Development of the Visible Light Photon Counter for Applications in Quantum Information Science

by

Kyle McKay

Department of Electrical and Computer Engineering
Duke University

Date: _____

Approved:

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Jungsang Kim, Supervisor

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April S. Brown

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Hissam Massoud

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Felix P. Lu

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Daniel J. Gauthier

Dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the Department of Electrical and Computer Engineering in the Graduate School of Duke University
2011

Abstract

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Abstract

The visible light photon counter (VLPC) is a high quantum efficiency (QE), Si-based, single-photon detector with high gain, low-noise multiplication, low timing jitter, and photon number resolution. While the VLPC has high QE in the visible wavelengths, the QE in the ultraviolet and infrared is low due to minimal absorption within the active layers of the device. In the ultraviolet, the absorption coefficient of Si is high and most of the incident photons are absorbed within the top contact of the device, whereas, in the infrared, Si is practically transparent. A number of applications in quantum information science would benefit from use of the VLPC if the QE was improved in the ultraviolet (e.g., state detection of trapped ions) and the infrared (e.g., long-distance quantum cryptography). This thesis describes the development of the ultraviolet photon counter (UVPC) and the infrared photon counter (IRPC), which are modified versions of the VLPC with increased QE in the ultraviolet and infrared wavelengths, respectively. The UVPC has a transparent metal Schottky contact to reduce absorption within the top contact of the VLPC, resulting in an increase in the QE in the ultraviolet by several orders of magnitude. The IRPC is a proposed device that has an InGaAs absorption layer that is wafer-fusion bonded to the VLPC. The band alignment of the resulting InGaAs/Si heterojunction is measured and shows a large discontinuity in the valence band that impedes carrier transport at the interface. A ultra-high vacuum wafer-bonding system was developed to understand the impact of the surface chemistry of the bonded wafers on the band

alignment of the InGaAs/Si heterojunction of the IRPC.

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List of Abbreviations and Symbols

Symbols

α	absorption coefficient
α_{D^+}	impact ionization coefficients for D+ charges
α_e	impact ionization coefficients for electrons
β	Poole-Frenkel parameter
χ	effective barrier height of interfacial layer
ΔE_C	conduction band discontinuity
ΔE_V	valence band discontinuity
δ	interfacial layer thickness
δ_1	energy differences between the Fermi level and valence band for InGaAs
δ_2	energy differences between the Fermi level and valence band for Si
ϵ	permittivity constant
ϵ_{si}	permittivity constant of Si
η	detector quantum efficiency
η_{abs}	absorption efficiency
η_{II}	impact ionization efficiency
λ	wavelength
μ	hole mobility
Φ_b	barrier height

ψ	surface potential
σ	conductivity
σ_e	impact ionization cross section
σ_r	RMS surface roughness
σ_{sb}	Stefan-Boltzmann constant
Θ	transmission coefficient
A	surface area
A^{**}	effective Richardson constant
C	capacitance
d	thickness of the absorption layer
$\mathcal{E}$	electrical field strength
e	emissivity of the material surface
$\mathcal{E}_{crit}$	characteristic field
E_{F0}	equilibrium Fermi level
E_{FP1}	quasi Fermi level for InGaAs
E_{FP2}	quasi Fermi level of Si
E_C	conduction band
E_F	Fermi level
E_V	valence band
G	gain
G_{II}	generation rate due to impact ionization
I	Current
J	current density
J_{D^+}	current density for D+ charges
J_e	current density for electrons
k_B	Boltzmann's constant

m^*	effective mass
N	number
n	ideality factor
N_a	acceptor concentration
N_C	effective density of states in the conduction band
N_d	donor concentration
PF	Poole-Frenkel enhancement factor
q	electron charge
R	reflectivity
R_0	spectral reflectance of an ideally flat surface
R_s	spectral reflectance of a real surface
R	reflectivity
T	temperature
t_c	thickness of top contact
T_c	temperature of cold surface
T_h	temperature of hot surface
t_i	thickness of intrinsic layer
v	drift velocity
V	voltage
V_{bi}	built-in voltage
V_{d1}	diffusion potential for InGaAs
V_{d2}	diffusion potential for Si
V_1	fractions of the applied voltage supported in InGaAs
V_2	fractions of the applied voltage supported in Si
V_a	applied bias voltage
V_D	diffusion potential

w	depletion width region

Abbreviations

AFM	atomic force microscopy
Al	aluminum
Sb	antimony
APD	avalanche photodiode
AR	anti-reflection
As	arsenic
Au	gold
BIB	blocked impurity band
B	boron
C	carbon
Cr	chromium
Cs	cesium
CTE	coefficient of thermal expansion
D+	D+ charges
DBS	dichroic beam splitter
DC	direct current
ENF	excess noise factor
F	fluorine
FWHM	full-width-at-half-maximum
H	hydrogen
HCl	hydrochloric acid
HF	hydrofluoric acid
Hf	hafnium

HTS	high thermal stress
IBC	impurity band conduction
InAlAs	indium aluminum arsenide
InGaAs	$\text{indium}_{0.53}\text{gallium}_{0.47}$arsenide
InP	indium phosphate
IPA	isopropanal
IR	infrared
IRPC	infrared photon counter
LOQC	linear optical quantum computation
LTS	low thermal stress
LWIR	long wavelength infrared radiation
Mg	magnesium
MgF_2	magnesium fluoride
Mo	molybdenum
N	nitrogen
NF	noise figure
O	oxygen
OFHC	oxygen-free, high-conductivity
PCF	photonic crystal fiber
PD	photodiode
PMT	photomultiplier tube
PNR	photon number resolution
QC	quantum cryptography
QDOGFET	quantum-dot, optically-gated, field-effect transistor
QE	quantum efficiency
QIP	quantum information processing

QIS	quantum information science
QKD	quantum key distribution
RCA	Radio Corporation of America
RF	radio frequency
RIE	reactive ion etching
RMS	root mean square
S	sulfur
SBP	Schottky barrier photodiode
Se	selenium
Si	silicon
SiO_2	silicon dioxide
SIMS	secondary ion mass spectrometry
SNR	signal-to-noise ratio
SNSPD	superconducting nanowire single-photon detector
SPAD	single-photon avalanche detector
SPD	single-photon detector
SSPM	solid-state photomultiplier
STJ	superconducting tunnel junction
TCSPC	time-correlated single-photon counting
TEM	transmission electron microscope
TES	transition edge sensor
Ti	titanium
TIA	time interval analyzer
UHV	ultra-high vacuum
UPS	ultraviolet photoelectron spectroscopy
UV	ultraviolet

UVPC	ultraviolet photon counter
VLPC	visible light photon counter
XPS	x-ray photoelectron spectroscopy

Acknowledgements

This thesis would not have been possible without the support of my advisor, Professor Jungsang Kim. Thank you for your leadership, guidance, and encouragement throughout the ups and downs of my thesis research. Your hard work and dedication has served as a model for me in my research career, and I owe much of my success and future successes to your efforts.

Thank you to Dr. Changsoon Kim and Dr. Felix Lu who, in my first few years at Duke, helped train me as a scientist. I am also grateful for the support and advice given to me by Dr. Scott Wolter over the years. A special thanks to my fellow graduate student, Dr. Caleb Knoernschild for his friendship and help throughout my graduate career.

I also want to thank Richard Nappi and Bernie Jelinek of the Physics Staff Machine Shop for their advice and willingness to teach me system fabrication and design. Thank you, Dr. Henry Hogue at DRS Sensors and Technologies for always being available to answer my questions about the visible light photon counter, as well as providing much of the material used to complete this thesis work.

I want to thank my parents for their love and encouragement. The lessons you have taught me and the example you set for me has shaped who I am today.

Finally, and most importantly, I want to thank my amazing wife and best friend, Becky. I wouldn't have made it this far without your love, patience, prayers, and encouragement.

1

Introduction

1.1 Single-Photon Detection

In a general detection process, the signal that an object of interest has been sensed needs to be transduced into an easily controllable form, e.g. an electrical signal. In a typical photodetector, radiation incident on the detector is absorbed and converted into electron-hole pairs. An applied bias creates an electric field that separates the carriers so they can be collected. The resulting current is an electrical signal proportional to the amount of input radiation absorbed. If the generated signal is greater than the background noise of the detection-circuit readout electronics, then the increase in the measured signal signifies the detection of input radiation. For a single-photon detector (SPD), the electrical signal generated by a single, electron-hole pair is typically much less than the intrinsic noise level of readout-circuit electronics. Significant gain is required to boost the detection signal above the background noise level so that the single photon can be detected.

Important figures of merits for SPDs include quantum efficiency (QE) and dark counts. The QE is defined as the ratio of the number of photons detected to the

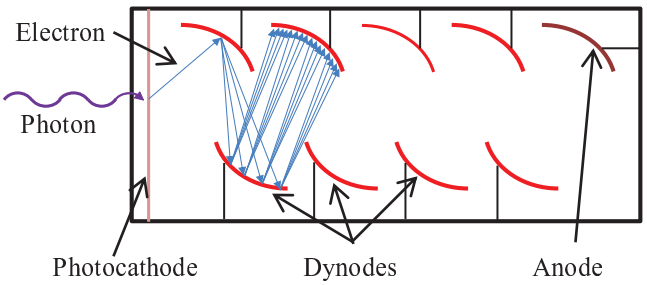

FIGURE 1.1: Schematic of a photomultiplier tube (PMT) operation. Absorption of a photon within the photocathode leads to emission of an electron. The electron is accelerated towards a series of dynodes and secondary emission from dynode surfaces leads to an exponential growth of electrons, which are collected at the anode. Typical gains for a PMT are $\sim 10^6$.

number of photons incident on the detector. In single-photon detection systems, a pre-set voltage threshold determines whether or not a photon has been detected. This threshold should be set above the background noise of the detection system but below the magnitude of the generated signal. Dark counts are detections that result from signals generated above the threshold when no photons are incident on the detector. An ideal SPD would have 100% QE and zero dark counts.

1.1.1 Brief History of Single-Photon Detection

Single-photon detection was first demonstrated using the photomultiplier tube (PMT) during the development of the television [1, 2, 3]. The PMT converts an incident photon into an electron via the photoelectric effect. The PMT then uses secondary emission from a series of positively-biased dynodes to achieve a gain of $\sim 10^6$ (see Fig. 1.1). The electrons are then collected at the anode resulting in a large current pulse that is easily detectable by subsequent electronics. This process requires high vacuum, so initial PMTs were fabricated using vacuum tubes. As a result, these initial fabrications were expensive and bulky.

The next breakthrough in single-photon detection came in the 1960s with the development of the avalanche photodiode (APD) [4, 5]. The APD is a solid-state

detector that operates by applying a large bias across a p-i-n junction. Photon absorption creates an electron-hole pair that, due to the large electric field, quickly gains enough energy to impact ionize additional carriers. Typical gains for APDs were around a factor of 100, too low for single-photon detection. However, by operating the APD in Geiger mode (typically referred to as single-photon avalanche detectors (SPAD)) above breakdown voltage, the gain of the APD could be increased by several orders of magnitude making single-photon detection possible [6, 7]. Due to their relative ease of use, availability, and performance, the SPAD and PMT are widely-used today.

While SPADs and PMTs were some of the first devices to exhibit single-photon detection, they are typically unable to distinguish between one and two or more photons events. The ability to determine the photon number is referred to as photon number resolution (PNR). The first device (to the author's knowledge) to exhibit PNR was the solid-state photomultiplier (SSPM), which had extremely broadband sensitivity between 400 nm and 28 μm [8]. The SSPM operates similar to the SPAD: it utilizes impact ionization to provide large gain. However, fluctuations in the gain were greatly suppressed compared to an APD resulting in an output pulse height proportional to the number of incident photons. Shortly after the development of the SSPM, the visible light photon counter (VLPC), a modified version of the SSPM with decreased sensitivity to long wavelength radiations, was demonstrated [9, 10].

Around the same time, interest in quantum information exploded and with it a desire for high-performance SPDs. Over the next two decades, numerous advances in fabrication technology led to the advancement of existing SPDs and the development of a number of new SPD technologies [11].

1.1.2 Quantum Information Science

Quantum information science (QIS) is an umbrella term that encompasses a number of topics, all of which exploit the properties of quantum mechanics and provide significant and novel benefits over classical approaches [12]. Information can be encoded into states of a quantum system (typically a well-controlled and understood system) and manipulated through experimental techniques to perform useful tasks. In order to maintain the quantum information, it is necessary to minimize interaction with the surrounding environment that causes decoherence, a loss of the quantum information.

A photon is a particularly useful quantum system for a number of reasons. First, due to its weak interaction with the environment, a photon has a long coherence time (the time it takes to decohere), relative to relevant quantum operations. Second, photons can transmit information quickly. And finally, they are readily accessible and easy to manipulate using commonly-available, off-the-shelf components. Single photons, and consequently SPDs, are particularly important to applications of quantum information processing (or quantum computing) and quantum cryptography.

Quantum Information Processing

In a classical computer, information is encoded in bits and represented as a 0 or a 1. Using N classical bits, any one number between 0 and $2^N - 1$ can be represented. In a quantum computer, information is encoded in quantum bits or qubits. Similar to a classical bit, they can be in either a 0 or 1 state. However, in contrast to a classical bit, a qubit can be placed into a superposition of 0 and 1 allowing it to occupy both states at the same time. As a result, a superposition of N bits can represent all of the numbers between 0 and $2^N - 1$ simultaneously, which enables massively parallel operations.

This scheme is referred to as quantum information processing (QIP) and has the

capability to efficiently solve some of classical computing's most difficult problems such as integer factorization and searching [12]. QIP-based algorithms that can solve these problems significantly faster than any classical algorithm have been developed [13, 14]; however, physical realization of a quantum computer has been difficult. For some physical implementations, such as linear optical quantum computation (LOQC) and quantum computation with trapped ions, the lack of SPDs that can meet the stringent demands imposed by QIP protocols has led to unwanted operational limitations. For an ion-trap quantum computer [15, 16], a SPD with high QE in the ultraviolet (UV) wavelengths is necessary for state detection [17, 18] and remote ion entanglement [19, 20]. For LOQC, high QE, photon number resolving detectors are needed for realizing two qubit gates and for error correction [21, 22, 23].

Quantum Cryptography

Quantum Key Distribution (QKD) is a fundamentally-secure communication protocol that can be used to create a set of private keys by transmitting information via public networks [12]. The key generation protocol is secure in the sense that the users can easily detect the presence of an eavesdropper and can determine what information has been compromised. The most common QKD scheme, BB84 [24], involves transmitting a polarized, weak (low power) laser pulse to the receiver. The receiver then measures the weak pulse in a particular polarization basis. Classical communication then can be used to select a subset of these measured bits and generate a secure key. For communication over long distances (tens of km), it is desirable to use an optical fiber in which photons with wavelength of 1.31 or 1.55 μm (referred to as the telecom wavelengths) can be transmitted over long distances with very little loss. The transmitted pulse should ideally be a single photon to prevent an eavesdropper from splitting the signal to extract information. Due to limitations on current single-photon sources, weak laser pulses are used to approximate a single pho-

ton. High-QE, high-speed, SPDs with low dark counts at the telecom wavelengths currently do not exist. Using currently available detectors, the key-generation rates of QKD protocols are low, making it difficult to communicate efficiently [11, 25, 26]. Other schemes for long-distance quantum cryptography include the use of quantum repeaters. Several proposals for implementations of a quantum repeater call for high-QE, photon-number-resolving detectors sensitive to the telecom wavelengths [11, 27, 28, 29].

Other applications in QIS that have need for high QE, SPDs over a wide spectral range include quantum metrology [30, 31] and quantum random number generators [32]. Additionally, a number of other fields outside of QIS, particularly in biological applications such as bioluminescence imaging [33, 34] and time-correlated single-photon counting (TCSPC) measurements [35, 36, 37], rely on high-performance SPDs.

The VLPC is one of the highest quantum efficiency SPDs available [11, 38]. It is also a photon-number-resolving detector [39] that can operate at high speeds [40]. However, the VLPC's use in QIS applications is limited because the high QE of the VLPC is bound to visible wavelengths. The QE drops rapidly in the ultraviolet wavelengths as well as near the telecom wavelengths [41]. The development of the VLPC towards improving the QE in the UV and at the telecom wavelengths is reported in this thesis.

1.2 Broadband Single-Photon Detection with Silicon

SPDs require a source of gain to increase the photoresponse generated by a single photon to a detectable level. For PMTs, the gain process is realized by secondary emission from dynodes. For solid-state detectors, such as APDs, SPADs, SSPMs,

and VLPCs, gain results from the impact-ionization process. Impact ionization is a scattering process in which the energy of a free carrier (such as an electron or hole) is transferred to a bound, electron-hole pair, resulting in the generation of an additional free electron and hole. By applying an electric field, the energy of free carriers can be increased rapidly and the impact ionization process leads to exponential growth in the number of carriers. The gain or multiplication noise associated with this process is minimized when only one type of carrier can trigger impact ionization events [42]. Low multiplication noise has a significant impact on the speed and QE of a SPD. Si has low multiplication noise compared to other materials, making it an attractive choice for use in SPDs.

Si has an indirect bandgap of 1.12 eV corresponding to a wavelength of ~ 1.1 μm, which makes it sensitive to the entire visible wavelength spectrum. Compared to direct-bandgap materials, the absorption coefficient of Si at visible wavelengths is much lower (see Fig. 1.2). However, due to the availability of high-quality, low-cost material and extensive Si fabrication capabilities, Si is the most commonly used photodetector material for visible wavelengths. Through the use of thick absorption layers, Si photodetectors are able to realize high QE despite a relatively low absorption coefficient.

At UV wavelengths, a direct bandgap transition in Si results in a increase in the absorption coefficient by almost two orders of magnitude. Si detectors, which are optimized for visible wavelengths, need to be redesigned to accommodate the increased absorption. A common problem for Si detectors in the UV is absorption within contact layers. The electric field in contact regions is almost zero, resulting in recombination rather than separation and collection of photogenerated carriers. Contact absorption can be minimized by the use of very thin contact layers (< 10 nm), which can be fabricated using methods such as Schottky metals [43, 44, 45], laser annealing [46, 47], and epitaxial growth [48]. UV-enhanced detectors using

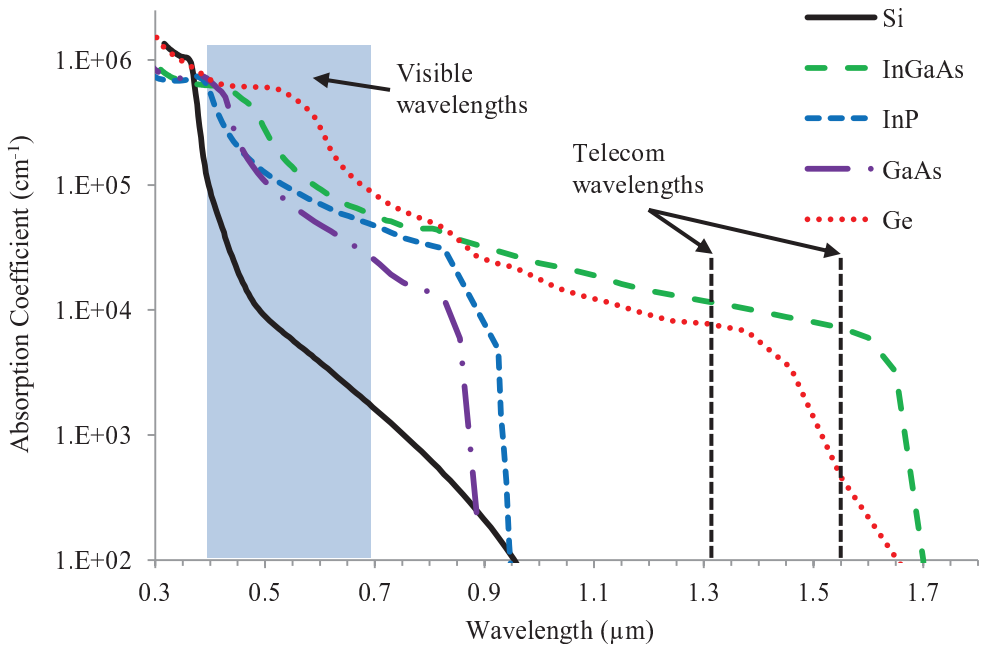

FIGURE 1.2: Absorption coefficients of several semiconductor materials typically used for photodetectors. Visible wavelengths range from $\sim 400 - 700$ nm. The telecom wavelengths are 1.31 and 1.55 μm and are referred to as such due to their low losses in silica optical fibers, which allows for long-distance communication.

these contact methods have resulted in tremendous performance gains compared to traditional contact devices. Using different materials for UV photodetectors is an option; however, the lack of high-quality materials with large bandgaps make these efforts challenging [49, 50]. Additionally, for SPDs high gain is required, and the gain noise associated with other materials is higher than that of Si. This makes it difficult to realize high-QE, solid-state, single-photon detection in the UV using materials other than Si.

The VLPC is a Si-based SPD with a separate absorption and gain layer (see Fig. 1.3) and is one of the highest QE SPDs in the visible but the QE in the UV is almost zero due to absorption within the top contact. The top contact, which is practically transparent for visible wavelengths, becomes opaque in the UV resulting in a decrease in the QE by several orders of magnitude. This thesis reports on the

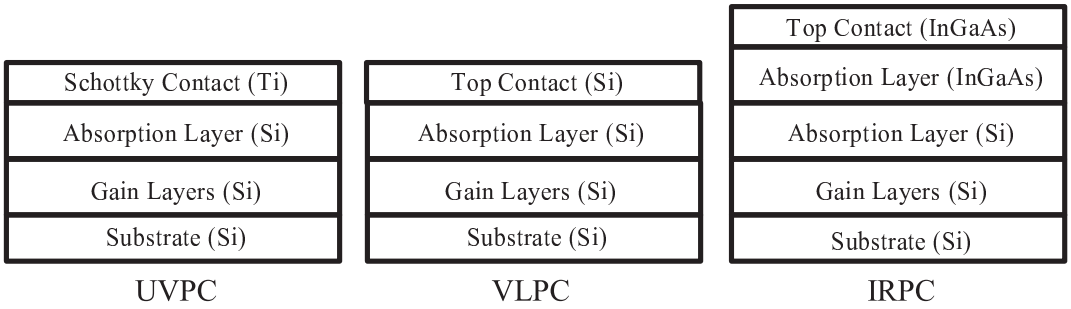

FIGURE 1.3: Schematic of the VLPC, UVPC, and IRPC. The UVPC and IRPC are modified versions of the VLPC designed for increased QE in the UV and IR, respectively.

use of alternative contact technologies to reduce UV photon absorption within the top contact and increase the QE of the VLPC in the UV [41].

At telecom wavelengths, the absorption coefficient of Si approaches zero making it practically impossible to utilize Si detectors at these wavelengths. Alternatively, $In_{0.53}Ga_{0.47}As$ (InGaAs), which is lattice-matched to InP, has a direct bandgap of ~ 0.74 eV at room temperature, corresponding to a photon wavelength of 1.68 μm. As shown in Fig. 1.2, InGaAs has strong absorption at the telecom wavelengths and is an ideal semiconductor material for realizing photodetectors at the telecom wavelengths. However, the use of InGaAs as a SPD is limited due to poor multiplication properties. Heterojunctions allow for the design of devices that use different materials to accomplish different tasks within the same device. This enables development of devices with significantly improved performance in comparison to homogeneous devices [51, 52, 53, 54, 55]. An ideal choice for a telecom wavelength SPD would be a heterojunction that uses InGaAs as an absorption layer and Si as a gain layer. InGaAs/Si heterojunction based APDs and SPADs have been demonstrated and exhibit significantly improved performance compared to homogeneous Si or InGaAs devices [52, 56, 57].

Heterojunctions are typically fabricated through epitaxial-growth techniques. A

requirement for epitaxial growth is that the different materials are lattice-matched to each other. InGaAs and Si have a lattice mismatch of $\sim$ 7.7%, which makes low-defect, epitaxial growth of InGaAs on Si very difficult using current techniques. An alternative means of combining the lattice-mismatched materials is to use wafer fusion bonding (or wafer bonding) [58, 59]. When two materials are smooth, flat, and clean, they can be permanently bonded together using wafer bonding. Wafer bonding has been used in the development of a number of high-performance, electronic devices [52, 53, 57, 60, 61]. An important consideration when designing heterojunction devices is the band alignment of the materials. How the conduction and valence bands of each material line up with respect to each other plays a critical role on the electrical properties of the heterojunction. A major goal in this thesis work is to investigate the wafer-bonded InGaAs/Si heterojunction and its role in the development of a VLPC sensitive to the infrared (IR) wavelengths.

1.3 Thesis Structure

The goal of this thesis is to further the development of the VLPC for use in QIS applications. The high QE and PNR capability of the VLPC make it an attractive detector choice for QIS applications, but the VLPC's response is limited to visible wavelengths. The work in this thesis is divided into three main parts: the VLPC, the ultraviolet photon counter (UVPC), and the infrared photon counter (IRPC). In the first part, the impact of the design and operation of the VLPC on the operating performance of the VLPC is presented. Chapter 2 provides background information on the VLPC and details the design and theory of the VLPC that enables the unique properties of the VLPC. In Chapter 3, the measurement and characterization of the timing jitter of the VLPC is presented. In the second part of this thesis, the ultraviolet photon counter (UVPC, see Fig. 1.3) is introduced. The design, fabrication, and performance of the UVPC is presented in Chapter 4 along with a description

of the measurement system used to test the VLPC and the UVPC. Work towards the development of the infrared photon counter (IRPC) is presented in the last part of this thesis. The IRPC is a proposed device that uses a wafer-bonded InGaAs absorption layer to improve the response of the VLPC to IR photons, particularly at the telecom wavelengths of 1.31 and 1.55 μm (see Fig. 1.3). Chapter 5 starts with an introduction to the wafer bonding process. The InGaAs/Si wafer bonding process is presented along with a measurement of the band alignment of the InGaAs/Si heterojunction. An ultra-high vacuum (UHV) system designed for understanding the impact of interface chemistry on the band alignment of wafer bonded heterojunctions is presented in Chapter 6. A discussion of future research directions and the impact of this thesis work is discussed in Chapter 7, and the thesis is concluded in Chapter 8.

2

Visible Light Photon Counter

The output of a single-photon detector (SPD) and its accompanying readout electronics is typically a narrow voltage pulse. When this voltage pulse is larger than the voltage threshold set by the discriminator circuit, the event is recorded as a single-photon detection. If a single-photon-induced voltage pulse is smaller than the voltage threshold, it will not be recorded, and the photon will not be detected. In general, the quantum efficiency of a detector is the ratio of the number of detected photons to the actual number of photons. However, the actual number of photons depends on where they are measured. Internal QE, external QE, and system QE are more specific terms that provide information on how the actual number of photons is quantified.

Internal QE is the ratio of the number of detected photons to the number of photons absorbed by the detector. External QE is the ratio of the number of detected photons to the number of photons incident on the detector (which includes photons reflected at the detector surface). For the remainder of this thesis, the term QE will refer to the external QE of the detector. The system QE is the ratio of the number of

detected photons to the number of photons inputted into the entire detection system. For example, a detector might use fiber coupling to guide light to the detector surface. Photons absorbed within the fiber would result in a decrease of the system QE but not in the internal or external QE. Dark counts are undesired detection events that occur even when the input photon source is shut off. They typically result from internal noise mechanisms and produce pulses that are indistinguishable from true photon events. Additionally, improper shielding of the detector from background radiation can lead to increased dark counts.

Another important figure of merit for SPDs is the excess noise factor (ENF). The ENF is a measure of the gain dispersion of the impact ionization or avalanche gain process. Ideally, a detector with gain, G, would produce G carriers for every absorbed photon (ENF = 1). However, fluctuations in the gain process lead to a distribution of gain values. The nature of that distribution is characterized by the ENF, which is defined by $\langle G^2 \rangle / \langle G \rangle^2$. The effect of increased ENF on the gain distribution is shown in Fig. 2.1. The ENF has a significant impact on the QE, the dark counts, and the ability to resolve photon number for a SPD. For a SPD with low ENF such as 1.025, it is easy to set a voltage threshold that distinguishes between background electronics noise and detection events. As the ENF increases, the pulse-height distribution (PHD) for detected photons merges with the background noise, and it is impossible to set a voltage threshold that fully distinguishes between the noise and the signal pulse. Thus, a compromise between increased dark counts and high quantum efficiency must be made. Additionally, for low ENF, the magnitude of the resulting voltage pulse is proportional to the number of incident photons. This makes it possible to discriminate between single-photon and multi-photon events (referred to as photon number resolution (PNR)). A practical requirement for PNR is high QE, as the probability of detecting a two-photon event is given by the square of the QE of a single event. As the number of photons increases, the efficiency for

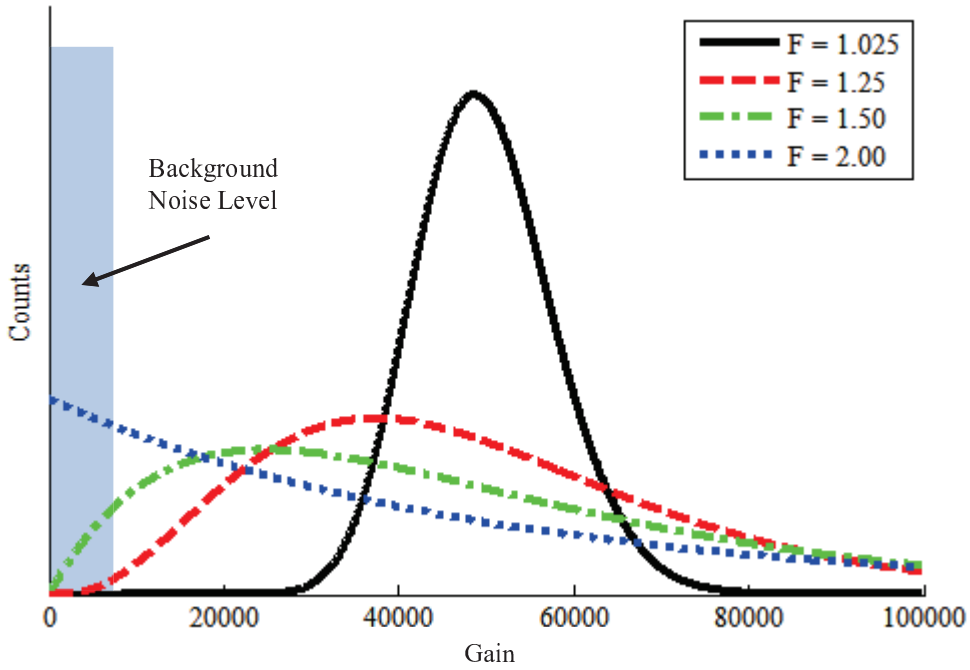

FIGURE 2.1: Plot of the gain distribution for a detector with average gain of 50,000 for different values of the ENF. As the ENF increases, the gain distribution broadens and increases the difficulty between distinguishing the detection signal from the background noise. Increased ENF also decreases the accuracy of PNR.

detecting the photon number decreases exponentially with the QE.

Other important figures of merit include timing jitter, spectral sensitivity, and maximum count rate. The timing jitter is a measure of the timing distribution of the arrival times of a detection pulse relative to photon arrival at the detector. Variations in absorption, transit times, or gain can cause uncertainty in the timing of the detection process leading to an increase in the timing jitter. Timing jitter is particularly important to high-clock-rate applications, such as quantum key distribution (QKD) [26] and linear optical quantum computation (LOQC) [21, 22, 23], and to time-correlated single-photon counting (TCSPC) measurements [35, 36, 37]. The spectral sensitivity is used to describe what wavelengths a detector is sensitive to. Most Si detectors have a spectral sensitivity range of 400 nm to 1 μm, but other detector properties, such as anti-reflection (AR) coatings, can adjust this range. The

spectral sensitivity is important for determining what types of SPDs are available for different applications. The maximum count rate of a detector is typically limited by dead times or afterpulsing of a detector. Dead time is a period of time after a detection event (or dark count) when the detector is insensitive to input photons. Afterpulsing is when there is an echo shortly after a detection, which is indistinguishable from the initial detection event. To minimize the effect of afterpulsing on the measured counts, the dead time of a detector can be increased electronically through the use of gating mode operation.

2.1 Single-Photon Detectors

There are a number of SPDs available today. In this section, some of the more common and high-performance detectors will be introduced.

2.1.1 Photomultiplier Tube

The photomultiplier tube (PMT) primarily consists of a photocathode, a series of dynodes, and an anode, which are configured in a vacuum tube. When a single photon with sufficient energy is incident on the photocathode, it will cause emission of an electron via the photoelectric effect. The emitted electron is then accelerated towards a series of dynodes that are biased at increasingly positive voltages. The accelerated electron will strike the dynode and eject additional electrons that are then accelerated towards the next dynode. Gains of $\sim 10^6$ are easily achievable by incorporating several dynodes. The emitted electrons are then collected by an anode, resulting in a large current pulse that is easily detectable by subsequent electronics. The performance of the PMT is governed by the photocathode material. In order to emit an electron, the incident photon needs to have energy greater than the work function of the photocathode material. PMTs are typically most useful in the UV wavelengths where the energy of UV photons is high compared to photocathode ma-

terials. The development of very low work function materials ($\sim$ 1 eV) and coatings have enabled PMTs to achieve quantum efficiencies of 40% at UV wavelengths; at longer wavelengths, the QE is lower [62]. PMTs have low dark counts ($\sim$ 100/sec), low timing jitter (300 ps), and high maximum count rates (10 MHz). The ENF of the PMT is relatively low ($\sim$ 1.25), which allows for some PNR, but the QE of the PMT makes PNR difficult to achieve practically.

2.1.2 Single-Photon Avalanche Photodiode

Avalanche photodiodes (APDs) are semiconductor-based detectors that utilize impact ionization of carriers across the bandgap of the material to achieve gain. When operated in Geiger mode, APDs have single-photon sensitivity and are referred to as single photon avalanche diodes (SPAD). In Geiger mode, the SPAD is biased above the breakdown voltage. A single carrier generated in the gain region causes rapid impact ionization of additional carriers. The rapid impact ionization leads to exponential growth in the number of carriers, eventual breakdown of the diode, and a large current pulse. After breakdown, the avalanche must be quenched to allow for detection of additional photons. Typically, the avalanche is quenched actively by sensing the avalanche and then reducing the bias voltage below breakdown to stop the avalanche. Si-based SPADs have a high QE of $\sim$ 70% with low dark counts ($\sim$ 50 Hz), low timing jitter (400 ps), and high max count rates (10 MHz) [63]. The ENF of SPADs is greater than 2, which makes PNR using traditional SPADs only possible through multiplexing techniques. SPADs fabricated using other materials, such as InGaAs/InP, are able to operate in the IR but at much lower QE. They also have much higher dark counts and longer dead times than traditional SPADs, which limits their max count rates [64].

2.1.3 Superconducting Tunnel Junction

The superconducting tunnel junction (STJ) uses a thin, superconducting layer as an absorption material. Absorption of a photon generates a large number of quasi-particles (Cooper pairs) that can tunnel across a thin, insulative layer and induce a voltage pulse. The size of the voltage pulse depends on the number of quasi-particles, which is proportional to both the number of photons absorbed and the energy of each photon. The STJ consequently has both PNR and energy resolution, though both are rather limited. The STJ has a QE as high as 45% in the UV with very low dark counts (< 10 Hz). However, the maximum count rate is very low (10 kHz), and the STJ must be operated at a very low temperature (~ 50 mK) [65].

2.1.4 Superconducting Transition-Edge Sensor

The superconducting transition-edge sensor (TES) is a type of bolometer that uses a superconducting layer as the absorption region. The superconductor is operated in the superconducting regime just below the critical temperature. When a photon is absorbed, the absorbed energy raises the temperature of the TES out of the superconducting regime leading to a large increase in the resistance. This change in resistance can be measured, and a voltage pulse proportional to the energy of the absorbed photon (or photons) is produced. The TES has a long dead time (~ 10 μs), which limits the maximum counting rate, and it must be operated at a very low temperature(< 1 K). However, the TES has demonstrated a system QE as high as 98% at 850 nm [66] and 95% at 1550 nm [67]. The sensitivity and high QE of the TES lead to efficient PNR and energy resolution [67].

2.1.5 Superconducting Nanowire Single-Photon Detector

The superconducting, nanowire, single-photon detector (SNSPD) operates in a similar fashion to the TES by taking advantage of the transition between superconduction

and normal conduction. The SNSPD is biased so that the current flow through a nanowire is below the critical current density threshold. When a photon is absorbed within the nanowire, it creates a hotspot where the resistance of the wire increases. This resistive region causes increased current flow in the remaining portion of the superconducting wire. This drives the current density above the superconducting threshold and causes a voltage pulse that can be detected by subsequent electronics circuit. The SNSPD quickly cools down ($\sim$ 30 ps) and returns to its original state. The SNSPD has very low timing jitter (50 ps) and is able to sustain very high count rates (1 GHz). Due to limited absorption in the nanowire, the QE is low [68]. However, by incorporating AR coatings and optical cavities or waveguides, QE as high as 94% at 1550 nm has been demonstrated, but at higher dark count rates ($\sim$ 10 kHz) [69, 70].

2.1.6 Quantum-Dot, Optically-Gated, Field-Effect Transistor

The quantum-dot, optically-gated, field-effect transistor (QDOGFET) uses a layer of quantum dots and a field effect transistor to detect the absorption of photons. Photogenerated holes are trapped by the quantum dots. This results in a modulation of the current that flows through the transistor. The increase in current is proportional to the number of photogenerated carriers, so the QDOGFET offers some degree of PNR. The QE of QDOGFETs is low (2%), and the max count rate is limited to $\sim$ 50 kHz [71, 72].

2.1.7 Solid-State Photomultiplier and Visible Light Photon Counter

The solid state photomultiplier (SSPM) operates similarly to the visible light photon counter (VLPC), which is the subject of this thesis and will be explained in detail in the following sections. The SSPM is a Si-based, blocked-impurity-band detector in which a photogenerated electron impact ionizes carriers across a small impurity

bandgap ($\sim$ 54 meV) and generates a well-controlled avalanche. Due to the impurity bandgap, the SSPM is an extremely broadband detector that is sensitive from 400 nm to 28 μms [8]. Both the SSPM and the VLPC require operation at $\sim$ 7 K in order to freeze out the impurity band. The VLPC has a similar design to the SSPM, but the VLPC has a thicker blocking layer and a thinner gain layer to reduce sensitivity to the far infrared and increase the absorption of visible wavelengths [9, 10]. A system QE of 88% has been demonstrated at 694 nm with a dark count rate of 20 kHz [38]. Additionally, the low noise multiplication process (ENF = 1.025) [73], along with the high QE, enables PNR capability for the VLPC and SSPM [74, 75, 76].

2.2 Visible Light Photon Counter

2.2.1 VLPC Structure

The structure of the VLPC is shown in Fig. 2.2(a). Several Si epitaxial layers, grown using vapor phase epitaxy with a total layer thickness of $\sim$ 30 μms, are grown on a Si substrate degenerately doped with Sb. The contact and spacer layers are As-doped layers that are compensated relatively heavily with B. The primary function of these layers is to isolate the gain layer from the substrate. The gain layer is also doped with As and lightly compensated with B. This layer is typically further divided into the gain and drift regions, which are distinguished only by the electric field profile. The intrinsic layer is a high-purity, undoped Si layer in which most of the visible light absorption takes place. The last layers are a thin transparent contact that is fabricated using ion implantation and annealing, followed by a single layer SiO_2 AR coating optimized for transmission at 550 nm.

2.2.2 VLPC Operation

The VLPC is operated at a temperature of $\sim$ 7 K where carriers in Si do not have enough thermal energy to be excited into the conduction band. Conduction at this

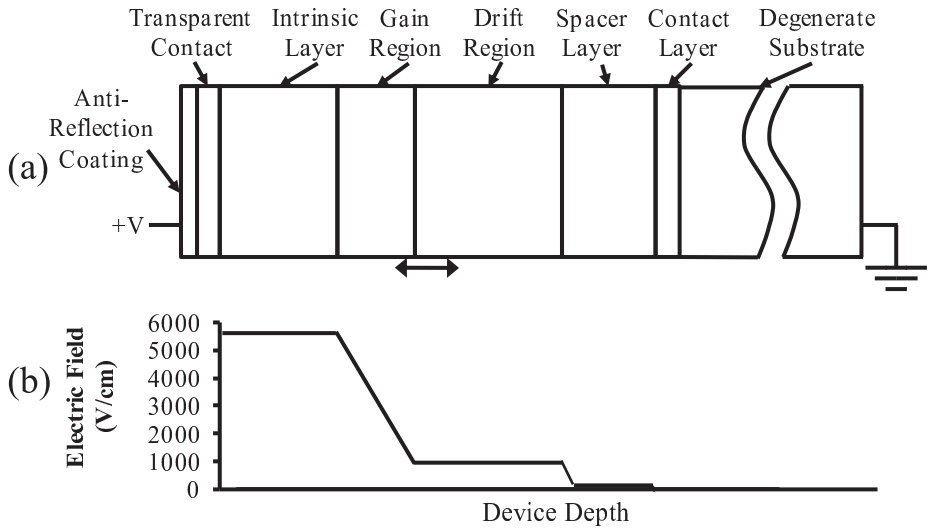

FIGURE 2.2: Schematic of the VLPC's (a) structure and (b) electric field profile. Total layer thickness of the epitaxial layers is ~ 30 μms.

temperature occurs via impurity band conduction (IBC) [77]. At sufficiently high impurity concentrations ($>\sim 10^{16}$ cm^{-3}), the impurities form a filled band where the wave functions of the impurities overlap. When compensating impurities are added, majority carriers in the impurity band will neutralize the compensating minority carriers resulting in empty states in the impurity band. Neighboring majority carriers can then tunnel into these empty states and charge will flow under the presence of an electric field. The conductivity of IBC depends strongly on the compensation levels [78]. IBC is the dominant conduction mechanism in the contact, spacer, drift, and gain layer. These layers are moderately doped with As, forming an impurity band ~ 54 meV below the conduction band and then compensated with B to control the conductivity. The empty states in the As impurity band are analogous to holes in the valence band and are referred to as D+ charges. At high donor concentrations, the impurity band merges with the conduction band and becomes metallic-like with high conductivity. This is the dominant conduction mechanism in the substrate and the top contact of the VLPC.

The VLPC is operated at a bias voltage of ~ 7 V, setting up an electric field in the device, which drives D+ charges in the gain layer away from the intrinsic layer. A depletion layer is formed at the gain layer to intrinsic layer interface as the intrinsic layer blocks IBC from the top contact to the gain layer. The large electric field enables electrons in the impurity band to tunnel into the conduction band through the Frenkel-Poole effect, resulting in the flow of a small bias current. This bias current sets up the regions of constant electric field in the drift region and spacer layer. The resulting electric field profile is shown in Fig. 2.2(b). Absorption of a single photon will generate an electron-hole pair (referred to as the primary electron and hole), which will quickly be separated by the applied field (see Fig. 2.3). The primary electron drifts towards the front contact and is collected while the primary hole drifts through the device. As the hole drifts through the gain and drift regions, it gains enough energy to impact ionize impurities in the impurity band, promoting an electron into the conduction band (referred to as the secondary electron). The secondary electron will then gain enough energy to impact ionize additional impurities and the successive impaction ionization events lead to an exponential growth of carriers referred to as an avalanche. A typical avalanche consists of several tens of thousands of electrons. The avalanche electrons will then be collected at the front contact, and the resulting large current pulse can be easily detected by subsequent electronics.

As the avalanche grows, D+ charges will accumulate in the impurity band. The conductivity of the D+ charges is several orders of magnitude less than that of electrons. On the timescale of an avalanche (< 1 ns), these D+ charges are practically immobile. The accumulation of these positive charges will reduce the local electric field and quench the avalanche. The electric field then drives these charges towards the substrate. Until they are driven away, the area local to the avalanche remains a type of dead zone where incident photons will not be detected. The low conductivity

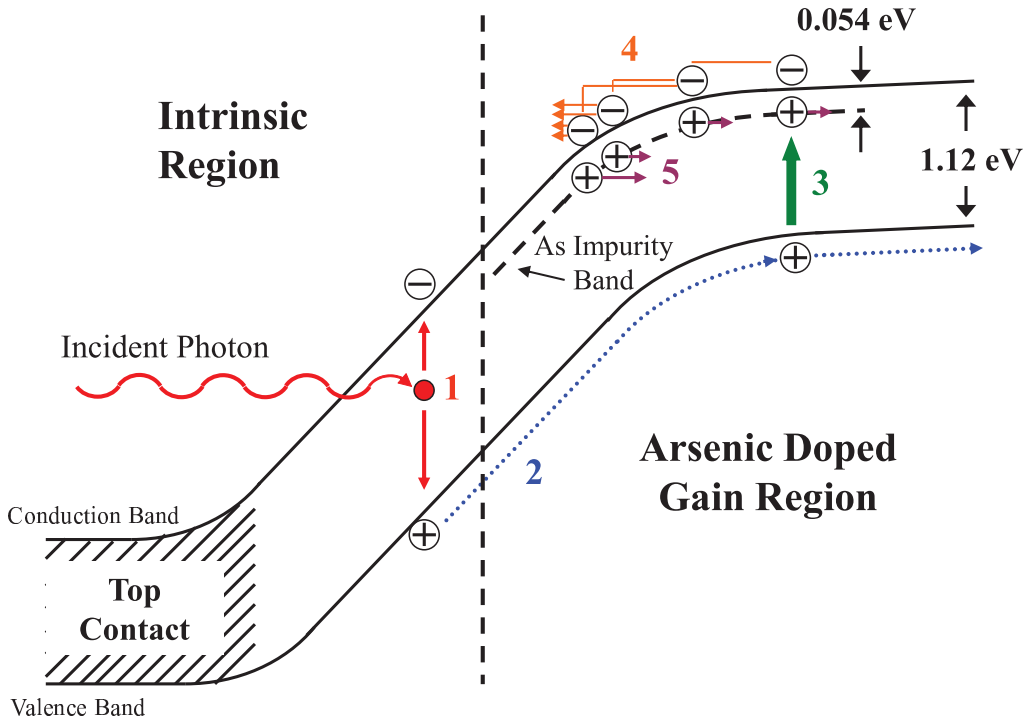

FIGURE 2.3: VLPC device operation. 1. An incident photon is absorbed generating an electron-hole pair. 2. The field in the device causes the hole to drift into the gain region. 3. The hole triggers an impact ionization event near the end of the gain region or within the drift region, which knocks an impurity electron into the conduction band. 4. The electron accelerates toward the front contact causing additional impact ionization events and starting an avalanche. 5. As the avalanche grows, D+ charges accumulate, which are slowly conducted away.

results in a local dead time $\sim$ 1 ms [79]. However, the active area of the VLPC is large ($\sim$ 1 mm^2), and the dead zone is only a small fraction of the active area (10^{-5} mm^2). The rest of the device remains sensitive to incident photons.

2.2.3 VLPC Performance

The VLPC features a demonstrated system QE of $\sim$ 88% at 694 nm and an estimated internal QE of $\sim$ 95% [38]. The QE of the VLPC can be modeled by

$$QE = (1 - R)\eta_{abs}\eta_{II}, \tag{2.1}$$

where R is the reflectivity, η_{abs} is the absorption efficiency, and η_{II} is the impact ionization efficiency. The reflectivity, R, of the VLPC is minimized by the use of a single-layer SiO_2 AR coating that reduces R to $\sim$ 10% at 550 nm. The use of refocusing mirrors to collect and redirect reflected photons back onto the device [80, 38], or the use of multilayer AR coatings can reduce R even further. The absorption efficiency is given by

$$\eta_{abs} = \exp\left(-\alpha t_c\right)\left\{1 - \exp\left[-\alpha\left(t_i + t_g\right)\right]\right\}, \tag{2.2}$$

where α is the absorption coefficent of Si, and t_c, t_i, and t_g are the thicknesses of the top contact, intrinsic layer and gain layer, respectively. Si is an indirect bandgap semiconductor for photon energies less than $\sim$ 3.4 eV; consequently, the absorption coefficient at visible wavelengths is relatively low compared to direct bandgap materials. The low absorption coefficient reduces absorption in the contact layer and the large combined thickness of the intrinsic and gain layer ($\sim$ 30 μm) results in a high absorption efficiency for visible wavelengths. The impact ionization efficiency, η_{II}, is the probability that the photogenerated hole will impact ionize an impurity band electron within the drift region, which is deep enough within the gain layer to trigger a full-size avalanche. Compared to a Si APD, where impact ionization occurs across the 1.12 eV bandgap, impact ionization in the VLPC requires significantly less energy to impact ionize impurities over the $\sim$ 54 meV impurity gap. The drift velocity of holes in the drift region is very high [81], and impact ionization is the dominant scattering mechanism in the gain and drift layers. For these reasons, the probability of impact ionization is high.

In addition to high QE, the VLPC features low gain dispersion, making the avalanche process practically noise free. The primary factors contributing to the low-noise multiplication are high impact ionization probability, single carrier multiplication, and localized field reduction [10]. The high impact ionization probability

reduces inelastic scattering and allows the avalanche to consistently grow to full size. In conventional Si APDs, the energy required to trigger impact ionization events is 1.12 eV. Before the carriers gain enough energy to trigger an impact ionization event across the 1.12 eV gap, there is a high probability that they will participate in inelastic scattering events, leading to a loss of energy. The randomness of these events makes the timescales and distances traveled by carriers between successive impact ionization events very random. This leads to a large variation in the gain of the device, and an increase in the gain dispersion. In contrast to APDs, the low, inelastic scattering rate of carriers in the VLPC gain process make the timescales and distances between impact ionization events more repeatable, helping to reduce noise in the gain process. After the photogenerated hole triggers one or more impact ionization events, the remainder of the avalanche is sustained by impact ionizations from electrons alone. The D+ charges that are left behind in the impurity band never gain sufficient energy to trigger impact ionization events, making the avalanche a single carrier multiplication process. Two-carrier multiplication is a dominant source of noise in conventional APDs. APDs are designed to maximize the ratio of the impact ionization probabilities of the two carriers in an attempt to minimize this source of noise [82]. A third contributor to the low noise associated with the VLPC gain is the effect of localized field reduction. As impact ionization occurs, D+ charges are left behind in the impurity band and relax slowly while the electrons are swept out of the gain region much faster (< 1 ns). The D+ charges act as space charge that attracts the electrons and reduces the field in the device. This effectively quenches the avalanche and limits the gain, helping to reduce multiplication noise.

The PNR of the VLPC is a result of the high QE, the low gain dispersion, and the large active area of the device. High quantum efficiency is necessary for reliable photon number discrimination as the efficiency for which N photons can be detected is given by η^N, where η is the quantum efficiency of the detector. The low gain

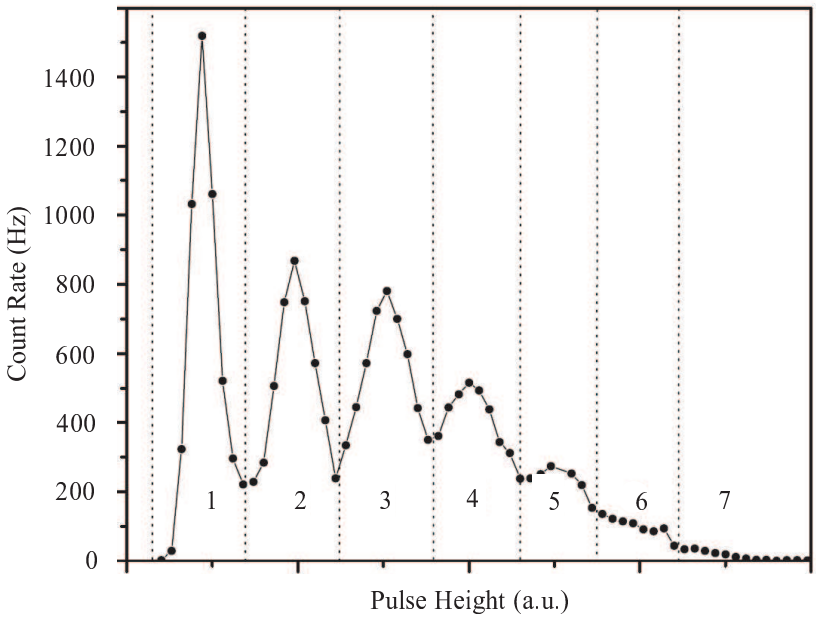

FIGURE 2.4: Pulse height distribution for the VLPC showing the size of the pulse depending on the number of photons detected. Dashed lines represent the voltage values at which thresholds would be set to determine photon number. Image reproduced with permission from [74].

dispersion and the high gain make it easy to discriminate the photon number from the pulse height [74, 39] (see Fig. 2.4). The large active area of the device ($\sim$ 1 mm^2) ensures that the local dead zone effect will leave most of the device sensitive to additional photons. Tight focusing of input radiation leads to degradation in the QE as a saturation effect due to the local dead zones but proper spot size design can minimize this effect [38].

Dark counts in the VLPC are the result of the tunneling of impurity-band electrons into the conduction band. At low temperatures, impurity-band electrons do not have sufficient thermal energy to be excited into the conduction band. However, because of the moderate field in the device, the energy required for electrons to tunnel from the impurity band into the conduction band is reduced by the Poole-Frenkel effect [9, 83]. The tunneling probability has a strong dependence on the field; therefore, tunneling is more likely to take place at the beginning of the gain region

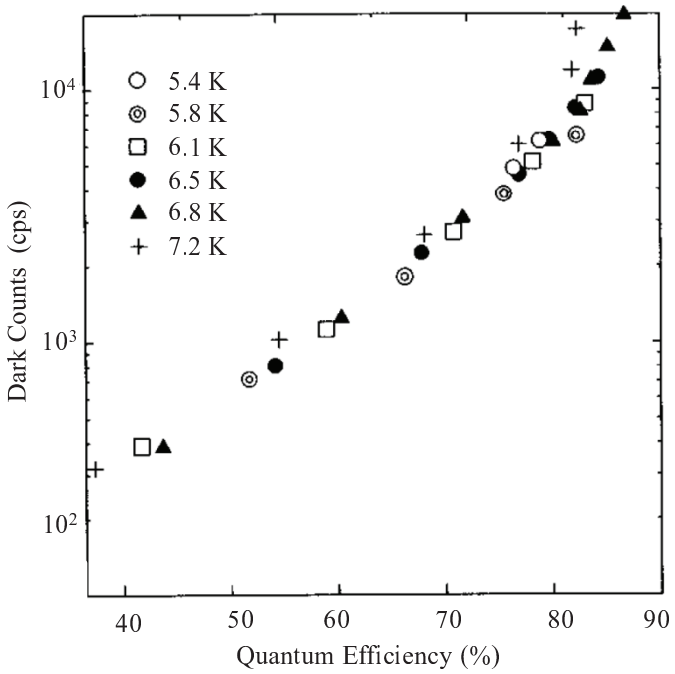

FIGURE 2.5: Dark counts vs. QE relation for the VLPC. Different symbols represent temperature at which measurement was taken while individual symbols represent data points taken at different dark count rates. The dark count rates are adjusted by changing the bias voltage. Image reproduced with permission from [38].

where the field is stronger (see Fig. 2.2(b)). Electrons that tunnel into the conduction band in this region will not have enough space to trigger full-size avalanches and will instead produce a steady DC bias current that flows through the device. The probability of tunneling near the end of the gain region is many orders of magnitude smaller than at the beginning of the gain region. However, an electron that tunnels from this region (approximately indicated by the arrow in Fig. 2.2(b))will produce a full-size pulse that is identical to the pulse created by a photogenerated hole. Fig. 2.5 shows the relationship between dark counts and the VLPC quantum efficiency. The quantum efficiency of the device improves at stronger fields, which leads to higher dark counts. Dark counts at the highest reported quantum efficiency ($\sim 88\%$) are $\sim 20,000$ counts per second [38].

2.2.4 VLPC Theory

The operation and performance of the VLPC are governed primarily by the electric field profile under bias. The VLPC gain layer is moderately doped ($\sim 5 \times 10^{17}$ cm^{-3}) with As, which at operating temperature results in a filled impurity band $\sim$ 54 meV beneath the conduction band. Donor electrons from this impurity band bind to compensating B acceptors resulting in empty states in the impurity band that behave similar to holes in the valence band and are referred to as D+ charges. When a positive bias is applied to the VLPC, the D+ charges will be driven towards the substrate by means of IBC. The intrinsic layer of the VLPC blocks IBC between the top contact and the gain layer, which prevents a bias current consisting of D+ charges from flowing through the device. Space charge consisting of immobile, negatively-charged acceptors remain and a depletion layer forms at the intrinsic/gain layer interface (see Fig. 2.6). The width of the depletion region, w, can be calculated using Poisson's equation and is given by [78]

$$w = \sqrt{\frac{2\epsilon_{si} V_a}{q N_a} + t_i^2} - t_i, \tag{2.3}$$

where ϵ_{si} is the permittivity constant of Si, V_a is the applied bias, q is the electron charge, N_a is the acceptor concentration, and t_i is the thickness of the intrinsic layer. The electric field is relatively constant within the intrinsic layer and the resulting initial electric field profile is shown in Fig. 2.6.

mathcalE

At the operating temperature of the VLPC, the thermal energy of electrons in the impurity band is insufficient to overcome the activation energy required to be excited into the conduction band. However, in the presence of a strong electric field, the activation energy is reduced by the Poole-Frenkel effect, and electron injection into the conduction band becomes possible. The Poole-Frenkel effect reduces the

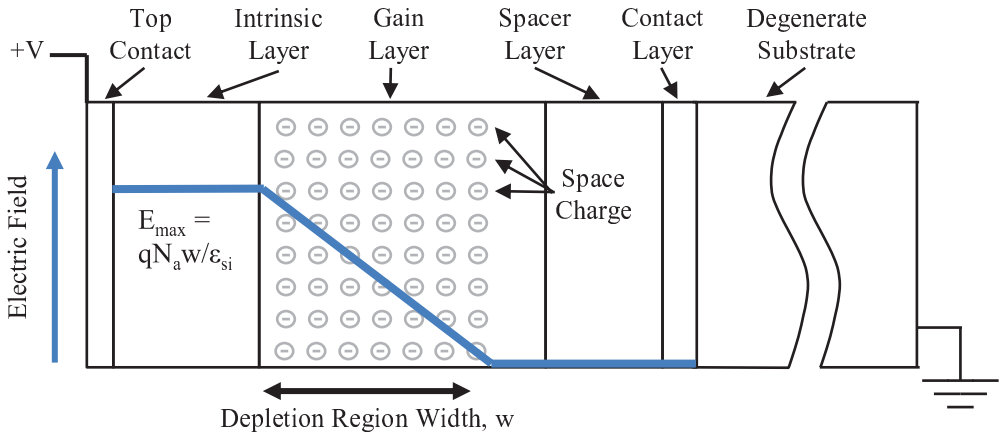

FIGURE 2.6: Initially, the applied bias drives away mobile D+ charges and a deletion region forms in the gain layer. The negative space charge consists of donor electrons bound to compensating B acceptor atoms. The initial field profile is constant within the high purity intrinsic layer with a value of $qN_a w/\epsilon_{si}$. The field decreases approximately linearly with a slope of qN_a/ϵ_{si}.

activation energy by $\beta\mathcal{E}^{1/2}$ where β is given by $\sqrt{q^3/\pi\epsilon_{si}}$, and for Si is 2×10^{-4} eVcm$^{1/2}$V$^{-1/2}$ and $\mathcal{E}$ is the electric field strength [84]. The increase in the generation rate of conduction band electrons due to the Poole-Frenkel effect is given by [9]

$$PF = \left(\frac{kT}{\beta\sqrt{\mathcal{E}}}\right)^2 \left[1 - \left(\frac{\beta\sqrt{\mathcal{E}}}{kT} - 1\right)\exp\left(\frac{\beta\sqrt{\mathcal{E}}}{kT}\right)\right] + \frac{1}{2} \tag{2.4}$$

Consequently, a small bias current flows through the device that consists of electrons in the conduction band and D+ charges in the impurity band. Electrons that tunnel into the gain region can then impact ionize additional carriers, which will increase the bias current. The generation rate of carriers due to impact ionization, G_{II} is given by

$$G_{II} = \alpha_e \frac{J_e}{q} + \alpha_{D^+} \frac{J_{D^+}}{q}, \tag{2.5}$$

where α_e and α_{D^+} represent the impact ionization coefficients for electrons and D+ charges, and J_e and J_{D^+} are the current density for electrons and D+ charges. The impact ionization coefficient is the inverse of the mean free path of carriers between

impact ionization events. The D+ charges move through IBC but never gain enough energy to impact ionize donor atoms and, consequently, α_{D^+} is zero. For electrons and holes, α_e is modeled by

$$\alpha = \sigma_e N_d \exp\left(-\frac{\mathcal{E}_{crit}}{\mathcal{E}(x)}\right), \tag{2.6}$$

where σ_e is the impact ionization cross section, N_d is the donor concentration, and $\mathcal{E}_{crit}$ is a characteristic field [85, 9]. The impact ionization cross section is determined by equating the ionization energy of the impurity to the coulomb energy and for Si is 1.6×10^{-13} cm^2. $\mathcal{E}_{crit}$ was experimentally determined by fitting data from blocked-impurity-band detectors and is estimated as 7000 V/cm.

Figure. 2.7 shows the Poole-Frenkel enhancement factor, the impact ionization coefficient, and the total gain as a function of position for a representative field profile of the VLPC. At the beginning of the gain region, where the electric field is strongest, the Poole-Frenkel and impact ionization coefficients are large. However, the total gain experienced by electrons generated in this region is small compared to a typical photodetection event (gain of 3×10^4 electrons). These carriers make up a persistent bias current that flows through the device. At a typical operating point of 7 K and 7 V, the bias current of the VLPC is $\sim$ 100 nA. Deeper in the gain region as the electric field strength decreases, the Poole-Frenkel coefficient drops rapidly, but carriers generated within this region can trigger a full-size avalanche, which is the source of dark counts in the VLPC.

The bias current leads to regions of constant electric field with a magnitude determined by Ohm's law,

$$J = \sigma \mathcal{E} \tag{2.7}$$

where J is the current density, and σ is the conductivity. In the drift region and spacer layer, the bias current consists of D^+ charges. The conductivity of D+ charges

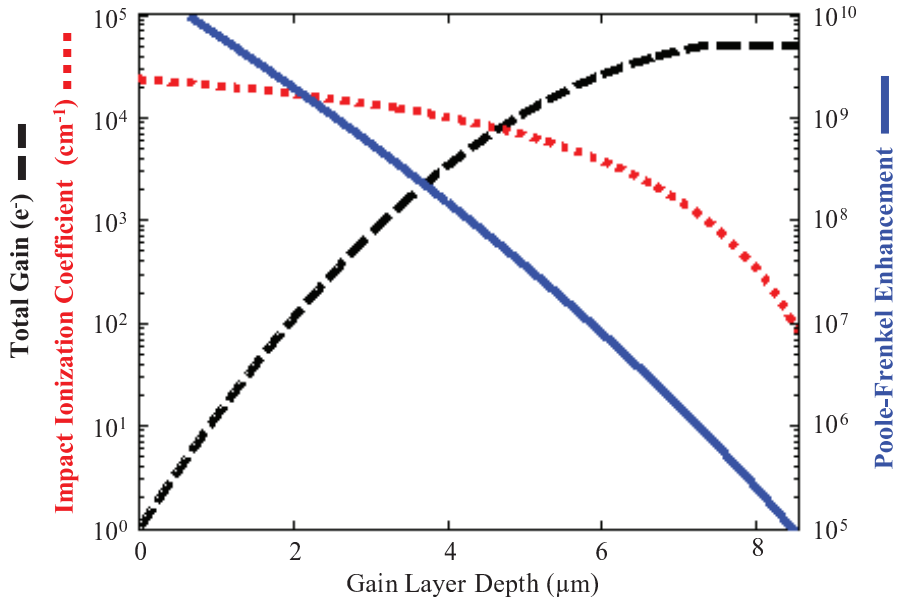

FIGURE 2.7: At the low operating temperature of the VLPC, impurity electrons have insufficient thermal energy to tunnel into the conduction band. At high electric fields, the Poole-Frenkel effect reduces the tunneling barrier and enhances the tunneling rate. The Poole-Frenkel enhancement factor is plotted as a function of position within the gain layer for a representative electric field profile. Conduction band electrons in the gain region will impact ionize additional carriers at a rate governed by the impact ionization coefficient. The total gain as a function of starting position is also plotted. At the beginning of the gain layer, the Poole-Frenkel enhancement and impact ionization coefficient are very high, but electrons generated in this region are swept out of the gain layer before they can trigger a full-size avalanche. These carriers contribute to the bias current which flows through the device. Deeper in the gain layer, the Poole-Frenkel enhancement factor is much lower, but electrons generated in this region have a large total gain and will generate full size pulses that are the source of dark counts in the VLPC.

is a product of the mobility and the concentration of free carriers, which are functions of the donor and acceptor concentrations [78]. The operating electric field profile of the VLPC can then be calculated for a given current density, doping structure, and applied bias.

3

Timing Jitter of the Visible Light Photon Counter

An ideal single photon detector (SPD) with zero timing jitter would produce a detection response exactly x time units after a photon was incident on the detector. This enables fast clock rates, which are critical for experiments such as quantum key distribution (QKD) [26] and linear optical quantum computation (LOQC) [21, 22, 23], and enable high timing accuracy for time-correlated single-photon counting (TCSPC) measurements [35, 36, 37]. A non-ideal detector has some uncertainties in the detection process: absorption location, transit times, and gain magnitude and growth rate. All of these uncertainties will lead to an increase in the timing jitter.

A general timing jitter measurement consists of a source with a narrow timing distribution (compared to the detector to be tested), a high-speed reference detector to define a start time for the measurement, a detector to be tested, and a discriminator that can record the timing of the detection pulse. The detection time minus the start time is recorded, and the experiment is repeated many times to generate a timing distribution for the detection process. The timing jitter is typically defined as the full-width-at-half-maximum (FWHM) of the timing distribution.

Many of the important properties of the visible light photon counter (VLPC), such as the quantum efficiency (QE), gain dispersion, photon-number-resolving (PNR) capabilities, and dark counts, are well characterized. However, the timing jitter of the VLPC is not fully understood. While several experiments have suggested that the timing jitter is relatively low, no thorough characterization has been done. In this chapter, a measurement for characterizing the wavelength, bias, and temperature dependence of the timing jitter of the VLPC, the results of those measurements, and a discussion of how the intrinsic properties of the VLPC led to those dependencies, is presented [40].

3.1 Timing-Jitter Measurement Setup

The timing jitter measurement was performed in collaboration with and at the National Institute of Science and Technology (NIST) at Boulder, CO. A schematic of the measurement setup is shown in Fig. 3.1. A Ti:Sapphire laser was used to generate 100-fs pulses at a repetition rate of 82 MHz. The pulses were then coupled into a 2-m-long photonic-crystal fiber. Nonlinear interactions within the photonic-crystal fiber (PCF) cause severe broadening of the ultrafast pulse, generating a supercontinuum with a very broad spectrum ranging from 470 nm to 1.3 μms. A dichroic beam splitter (DBS) was used to separate the pump signal from the supercontinuum, and the diverted pump pulse was detected by a fast Si photodiode (PD). The PD response was sent to the time interval analyzer (TIA) to start a timer. Filters and a grating monochromator were used to filter the supercontinuum down to pulses with a spectral bandwidth of 4 nm. The spectrally-filtered pulse was then coupled into a single-mode fiber connected to the cryostat.

The VLPC was cooled using a closed-cycle, cryogen-free, He-gas cryostat. The VLPC was mounted on a brass stage that included a thermometer and a heater, used to precisely control the temperature. A 4 K radiation shield was used to shield

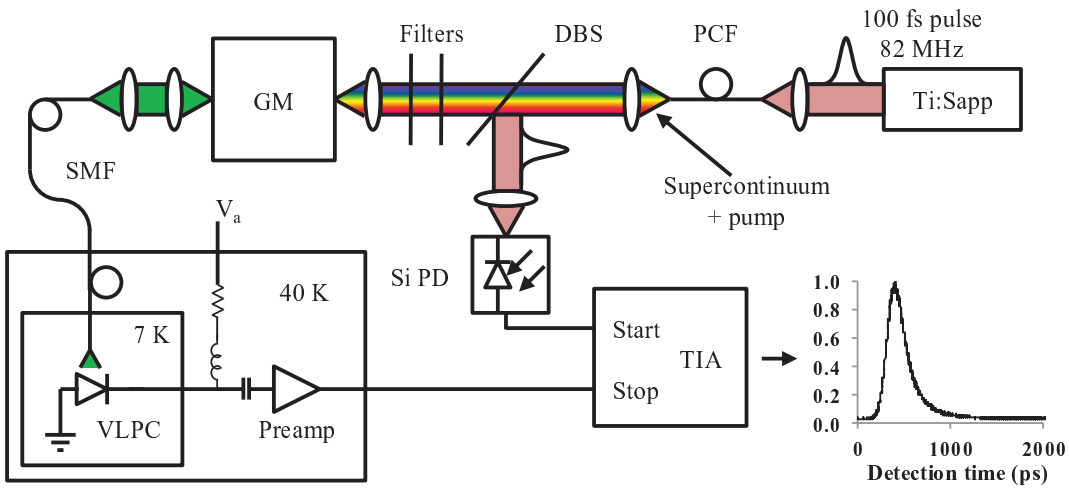

FIGURE 3.1: Schematic of the VLPC timing jitter measurement. PCF: photonic crystal fiber, DBS: dichroic beamsplitter, Filters: color and neutral density filters, GM: grating monochromator, SMF: single mode fiber, Si PD: fast Si photodiode, TIA: time interval analyzer. The setup is used to generate histograms of the timing distribution of the VLPC at variable wavelengths.

the VLPC from blackbody radiation. The fiber was aligned and mounted 1 mm from the VLPC with an expected spot size ($1/e^2$, 86.5%) ranging from 100 μm at 470 nm to 200 μm at 1 μm. The VLPC detection signal was amplified by a cryogenic preamplifier that was mounted on a 40 K stage and then by subsequent room-temperature amplifiers. The resulting detection signal was sent to the TIA. The TIA recorded the time difference between the start time generated by the pump and Si PD and the stop time generated by the VLPC detection pulse. The measurement was repeated to generate appropriate statistics, and a histogram of the VLPC timing distribution was recorded.

The timing jitter of the measurement setup was calibrated using a superconducting-nanowire single-photon detector(SNSPD), which has very low timing jitter ($\sim$ 40 ps). The timing jitter of the measurement setup was less than 100 ps at all wavelengths tested. The system QE of the VLPC in this setup was 40% at a bias of 7.2 V and a temperature of 7 K. The system QE was well below the intrinsic QE of the VLPC

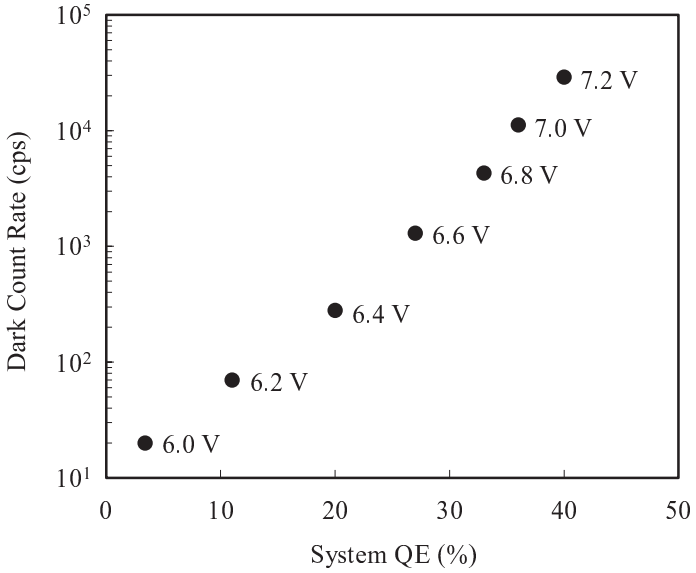

FIGURE 3.2: Plot of the dark counts of the VLPC as a function of the system QE. The system QE was measured at 633 nm at a temperature of 7 K.

($\sim 95\%$), but improvements in the fiber coupling, connector losses, and AR coatings could be used to increase the system QE of the measurement setup. The measured dark counts of the VLPC as a function of the system QE are shown in Fig. 3.2. The exponential relationship between the dark count rate and the system QE implies that the background count rate due to blackbody sources was negligible.

3.2 Timing-Jitter Results

The timing jitter of the VLPC was measured as a function of wavelength, bias, and temperature. The count rate of the VLPC was set to 5×10^4 counts per second, well below saturation levels, to avoid any associated performance degradations. The count rate was controlled by adjusting the optical attenuation at the desired wavelength by using a variable attenuator.

Normalized, background-subtracted histograms for the timing response of the VLPC at three different wavelengths and biases is shown in Fig. 3.3. The histograms

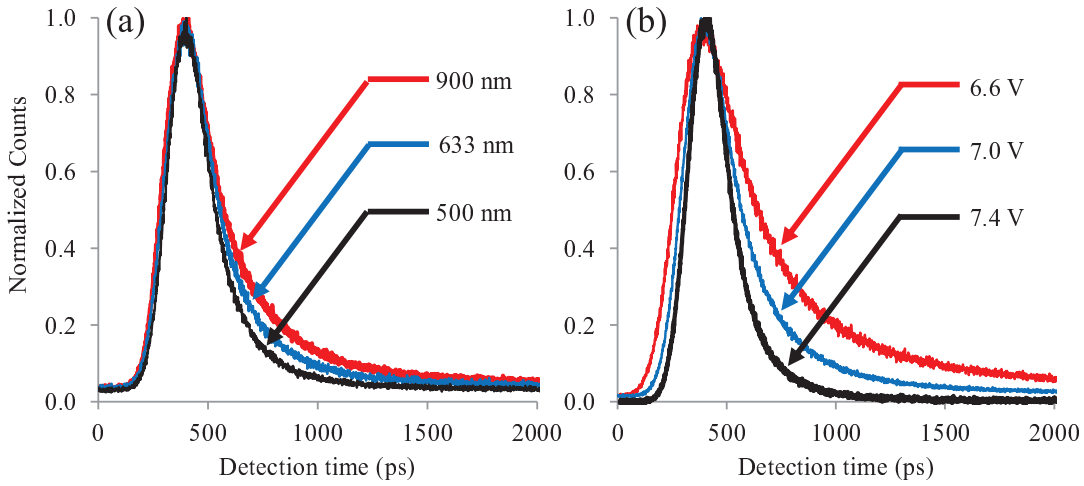

FIGURE 3.3: Photon detection time histograms of the VLPC at three different (a) wavelengths and (b) voltages.

show a timing distribution that has gaussian and exponential distribution components. For longer wavelengths and for decreasing bias voltages a long tail is also evident in the distribution. The timing jitter was extracted from the histograms by measuring the FWHM and the timing jitter as a function of wavelength and bias is shown in Fig. 3.4. As the wavelength is increased from 470 nm to 1 μm at a constant temperature of 7 K and bias of 7.2 V, the timing jitter of the VLPC increases from $\sim$ 240 ps to $\sim$ 310 ps. The timing jitter has a stronger dependence on the bias as the timing jitter increases from $\sim$ 210 ps to $\sim$ 470 ps as the bias decreases from 7.6 V to 6.4 V at a temperature of 7 K and a wavelength of 633 nm. Decreasing the temperature increases the timing jitter of the VLPC slightly ($\sim$ 70 ps/K).

3.3 Discussion of the VLPC Timing Jitter

The wavelength, bias, and temperature dependence of the VLPC timing jitter can be understood by considering the operation of the VLPC. Detailed descriptions of the VLPC operation can be found in Sec 2.2, but the relevant operating principles

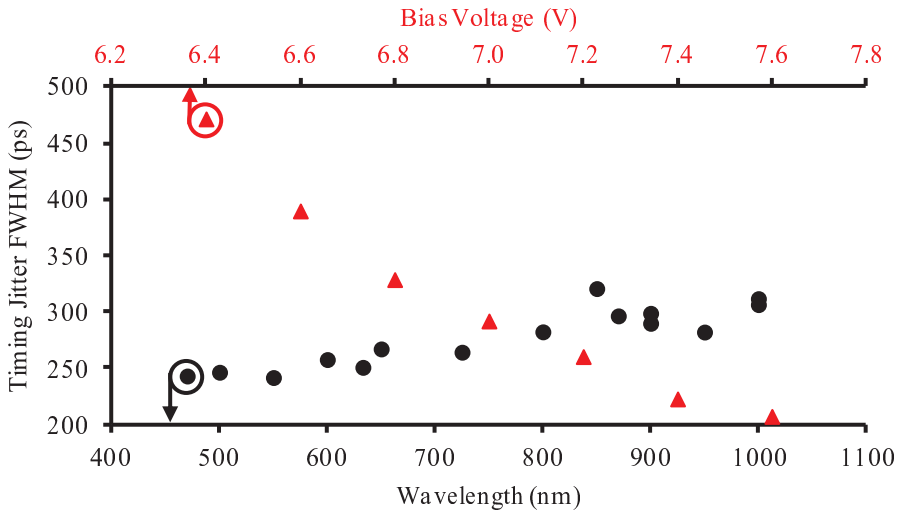

FIGURE 3.4: Plot of the timing jitter of the VLPC as a function of wavelength (circles) and bias voltage (triangles). The bias voltage dependence was measured at 633 nm and 7.0 K. The wavelength dependence was measured at a bias voltage of 7.2 V and a temperature of 7.0 K.

are briefly described below. The device structure is shown in Fig. 3.5(a) and consists of several epitaxial layers with a total layer thickness of ~ 30 μm. The electric-field profile of the device under bias is shown in Fig. 3.5(b). At the operating temperature of 7 K, impurities in the gain and drift region form a populated impurity band ~ 54 meV below the conduction band. The primary electron-hole pair generated by the absorption of a photon is separated by the field, and the hole accelerates into the drift region. The purpose of the drift region is to ensure that the photogenerated hole will impact ionize at least one neutral impurity-band atom to provide an electron (referred to as the secondary electron) in the conduction band. The secondary electron drifts towards the front contact, and successive impact-ionization events in the gain region cause a local avalanche of several tens of thousands of electrons. Long-wavelength-visible and infrared photons may propagate beyond the intrinsic layer and gain region before they are absorbed, in which case the primary electron will trigger the avalanche.

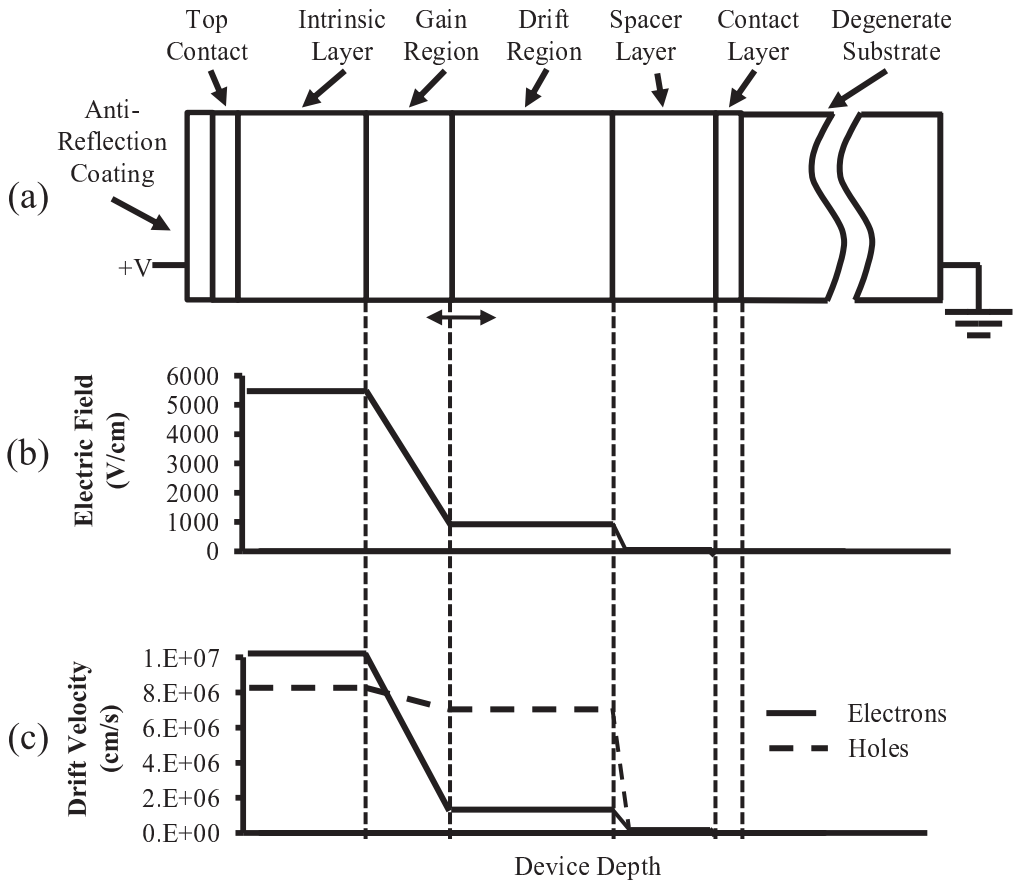

FIGURE 3.5: Schematic of the (a) VLPC Structure, (b) electric field profile, (c) associated drift velocity of electrons (solid line) and holes (dashed line). The schematic is drawn roughly to scale (lengthwise).

The electron drift velocity under voltage bias is shown schematically in Fig. 3.5(c). The drift velocity, v, for carriers in the ohmic regime is given by $v = \mu\mathcal{E}$, where μ is the mobility ($\mathrm{cm^2V^{-1}s^{-1}}$) and $\mathcal{E}$ is the electric-field strength ($\mathrm{Vcm^{-1}}$). The mobility of electrons in gain layer is limited by neutral-impurity scattering and can be estimated using Erginsoy's formula [86],

$$\mu = \frac{8\pi\epsilon E_d}{20 N_d \hbar q}, \tag{3.1}$$

where ϵ is the permitivity of the material, E_d is the donor energy level, N_d is the donor concentration, and for the VLPC gain layer the mobility is $\sim 1330\ \mathrm{cm^2V^{-1}s^{-1}}$.

Due to the low mobility and reduced field in the gain layer, the drift velocity of the secondary electron decreases rapidly in the gain layer. In the drift region, the electric field is on the order of 1000 V/cm resulting in a drift velocity of $\sim$ 13 nm/ps and a transit time of $\sim$ 75 ps/μm. As the generation of a secondary electron occurs deeper in the drift region, the delay between photon absorption and avalanche generation is prolonged. This leads to the asymmetric shape and long tail observed in the timing distribution. At optimum bias conditions (where the QE of the VLPC is highest, $\sim$ 7 K and $\sim$ 7.2 V), the impact ionization of the secondary electron occurs between the tail end of the gain layer and the top portion of the drift layer (hereafter referred to as the arrow region and marked by the arrow in Fig. 3.5(a)). Variations in secondary electron generation within the arrow region convolved with timing jitter in the avalanche process and the measurement-system jitter are the source of the measured timing jitter of $\sim$ 240 ps at 470 nm. Secondary electrons that are generated beyond the arrow region will have long transit times and contribute to the tail in the timing distribution.

The wavelength dependence of the VLPC timing jitter is a result of the distribution in transit times of the photogenerated hole (or electron) before it triggers an avalanche. The hole drift velocity in the VLPC is $\sim 1 \times 10^7$ cm/s (for electric fields in the range of $\sim 1 - 10$ kV/cm). At a photon wavelength of 500 nm, the absorption coefficient (absorption length) of Si at the operating temperatures is $\sim 5 \times 10^3$ cm^{-1} (2 μm), whereas at 1 μm, it is $\sim 1 \times 10^2$ cm^{-1} (100 μm). As a result of the change in absorption length with wavelength, the variation in the location of the primary hole generation results in a variation in transit times for the primary hole before it can generate a avalanche-inducing secondary electron. The timing jitter resulting from this variation in hole transit times is $\sim$ 20 ps at 500 nm to $\sim$ 200 ps at 1 μm. For wavelengths longer than $\sim$ 750 nm, a significant fraction of the incident photons are absorbed within the drift region. In this case, the secondary electron then triggers

the avalanche. Due to low drift velocity of electrons, the transit times for primary electrons deep in the drift region can be long ($\sim$ 1 ns), resulting in an increase in the size of the tail in the timing distribution.

The bias dependence of the VLPC timing jitter is due to increased variation in the location of secondary-electron generation and is closely related to the dependence of the VLPC QE on bias voltage (see Fig. 3.6. As the bias voltage is reduced, the magnitude of the electric field decreases. As a result, the impact ionization probability (see Eq. 2.6) and the Poole-Frenkel enhancement factor (see Eq. 2.4) are reduced resulting in a lower bias current. The electric field in the drift region is proportional to the current density (see Eq. 2.7). As the bias voltage is reduced by $\sim$ 1 V, the bias-current density, and consequently the electric field in the drift region, is reduced by a factor of $\sim$ 2 [10].

The reduced electric field in the drift region has several effects. First, it reduces the impact ionization probability for the hole to generate a secondary electron as the hole drifts through the drift region. As a result, a higher percentage of primary holes will drift through the drift layer without generating a secondary electron leading to a decrease in the QE of the VLPC. The reduced impact ionization probability also increases the size of the arrow region, which then increases the timing jitter resulting from transit time differences due to the spread in location of secondary electron generation in this arrow region. The reduced impact ionization probability also increases the probability of secondary electrons being generated deep in the drift region, which increases the size of the tail. The reduced electric field in the drift region also results in a lower drift velocity for electrons in this region. The lower drift velocity increases the secondary-electron transit-time timing jitter as well as the length of the tail in the timing distribution.

The temperature dependence of the timing jitter ($\sim$ 70 ps/K) results from similar effects as reducing the bias voltage. As the temperature is reduced, the thermal

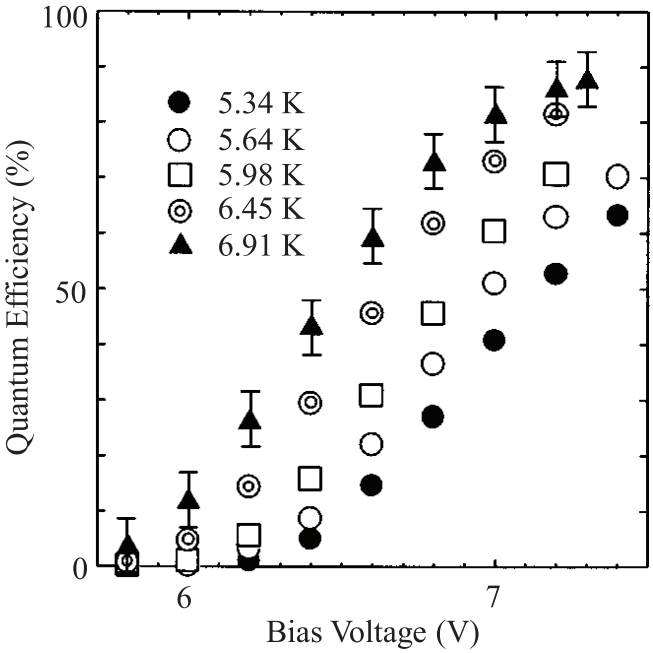

FIGURE 3.6: QE vs. bias voltage for the VLPC at several different temperatures. Image reproduced with permission from [38].

energy of impurity band electrons is reduced. This reduction decreases the thermal generation rate of carriers and decreases the bias current. The decreased bias current reduces the electric field in the drift region, and the decrease in temperature acts as a reduction in the applied bias of the device. As shown in Fig. 3.6, a change in temperature of ~ 1 K is consistent with a change in effective bias voltage of ~ 0.4 V, which is consistent with the observed change in the timing jitter.

4

Ultraviolet Photon Counter

The measured quantum efficiency (QE) of the visible light photon counter (VLPC) as a function of wavelength is shown in Fig. 4.1. Also plotted is the absorption coefficient,α, of Si at 10 K [87]. The QE is high in the $400-650$ nm wavelength range but drops sharply below 400 nm. The high QE of the VLPC in the visible wavelength range is attributed to the VLPC's near-unity absorption efficiency and the high probability for the impact-ionization process to occur and initiate an avalanche event. The absorption efficiency of the VLPC is given by Eq. 2.2. In the visible wavelengths, where α is $\sim 10^3 - 10^4$ cm^{-1}, absorption within the front contact layer($\sim$ 250 nm thick) is small and the contact is transparent. The combined thickness of the intrinsic and gain layers ($\sim$ 30 μm) leads to a near-unity probability of absorption. For wavelengths $<$ 400 nm, α rises rapidly due to a direct-bandgap transition of Si, and nearly all of the incident photons are absorbed within the front contact layer, reducing the absorption efficiency significantly and causing the QE of the VLPC to decrease dramatically. In this chapter, a modified version of the VLPC called the ultraviolet photon counter (UVPC), which has increased QE at UV wavelengths, is presented.

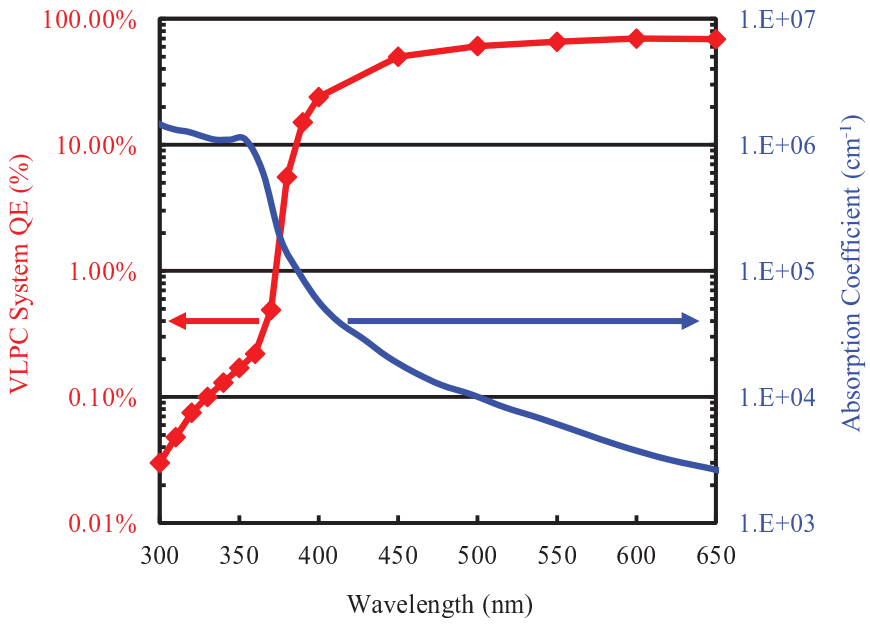

FIGURE 4.1: The measured system QE of the VLPC at 7 K and a bias of 7.2 V, and the Si absorption coefficient at 10 K in the wavelength range of $300 - 650$ nm is shown [87]. The QE drops sharply below 400 nm, which corresponds to a rapid increase in the absorption coefficient of Si.

To increase the QE of the VLPC in the UV, it is necessary to reduce absorption within the VLPC front contact layer. Potential methods for achieving this goal include Schottky metal contacts, laser-annealed contacts [46, 47], and ultra-thin contacts grown with molecular beam epitaxy [48]. The Schottky contact approach for increasing the QE of the VLPC in the UV is discussed in this chapter.

4.1 Design of the UVPC

The structure of the UVPC is shown in Fig. 4.2(b). The degenerately-doped Si front contact of the VLPC is removed and replaced with a thin, Ti contact layer ($\sim$ 10 nm thick) with a single-layer, MgF_2 AR coating that protects the Ti from oxidation and reduces the reflectance of the contact.

The design of the UVPC resembles the Schottky barrier photodiode (SBP), an ordinary *p-i-n* diode with *p* material replaced by metal. The QE of a photodiode

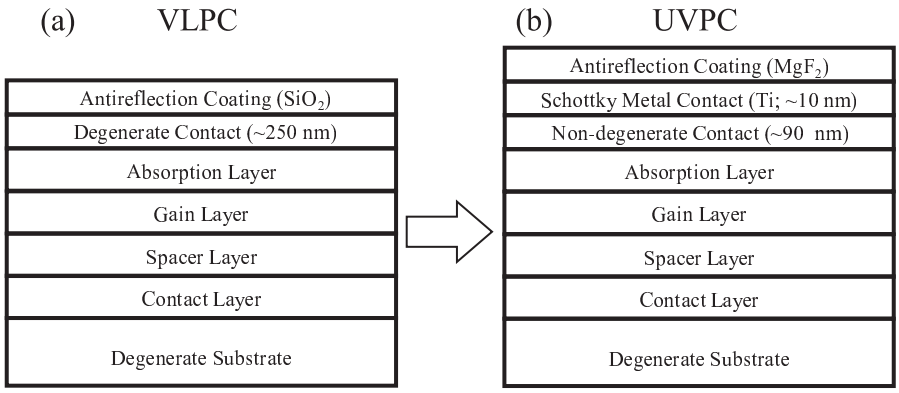

FIGURE 4.2: Schematic device structure of the (a) VLPC and (b) UVPC. The degenerately doped front contact of the VLPC is thinned and replaced with a Ti Schottky metal contact and a MgF_2 AR coating.

is maximized by ensuring that incident light is absorbed within the depletion region. For a SBP, the depletion region begins immediately after the metal. For this reason, SBPs are particularly useful in the UV wavelengths where the absorption coefficient of Si is high. For the same reason, a Schottky contact will increase the QE of the VLPC in the UV. Photons transmitted through the Schottky contact will be absorbed within the VLPC's intrinsic absorption layer where the field is strong enough to separate the carriers and drive the hole into the gain layer. Important design considerations for high QE SBPs are the transmission of the Schottky metal contact and the Schottky barrier height. These same considerations are important to the design of the UVPC.

Maximizing the transmission of a Schottky metal contact involves minimizing the absorption and reflectance of the metal contact. To minimize the absorption in the contact, a metal with a small absorption coefficient should be selected and made as thin as possible. There is a tradeoff between the electrical and optical properties of the metal film: thinner metal decreases the conductivity while thicker metal increases the absorption. Reducing the reflectance of the metal contact can be achieved through the use of AR coatings.

The Schottky barrier height also plays a significant role on device performance. For the UVPC, we want to ensure that there is no barrier to electron collection and a high barrier to hole injection. Direct injection of holes from the metal to Si will result in an avalanche identical to that from a photogenerated hole, leading to increased dark counts. For an ideal Schottky barrier, the barrier height is determined by the difference between the electron affinity of the semiconductor and the work function of the metal. For a real Schottky barrier, interface states have a major impact on the barrier height and generally reduce the p-type barrier. For this reason, as well as to reduce recombination near the interface, it is important to keep the metal Si interface clean and minimize surface states.

Titanium was used as a thin Schottky metal contact in the UVPC due to its relatively low absorption in the near UV ($300 - 400$ nm) and its high p-type barrier. Calculated values for the transmission of a 10-nm-thick Ti film are greater than 40% with a single layer MgF_2 coating and can be made greater than 70% with multilayer coatings for wavelengths longer than 300 nm. High p-type barrier diodes have been fabricated on Si with Ti through careful control of the Ti/Si interface [88, 89]. Important features of these devices include a clean Si surface and removal of H from the interface. Native oxide removal, crucial in preventing any electrical barrier, is typically accomplished with the use of hydrofluoric acid (HF), which leaves the Si surface terminated with H. In-situ Ar-ion RF sputtering was used to remove any H from the interface and ensure a clean surface prior to Ti deposition. Using this technique, p-type Schottky diodes were fabricated with a high p-type barrier height of 0.60 ± 0.04 eV and an ideality factor of 1.10, indicating a high-quality interface. The p-type barrier was determined by measuring current-voltage relationships and applying thermionic-emission theory [83] (See Fig. 4.3).

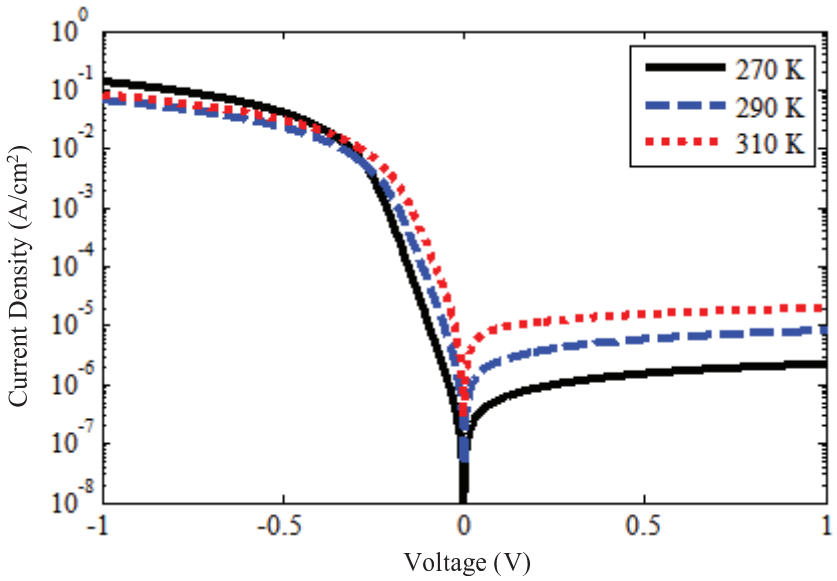

FIGURE 4.3: Current density-voltage (J-V) relationship of a 1000 μm diameter Ti Schottky diode with a MgF_2 coating. Thermionic emission-diffusion theory was used to determine the p type barrier height of 0.60 V. For clarity, data for all temperatures measured and used in the analysis are not shown.

4.2 UVPC Fabrication

The UVPC was fabricated by modifying a standard 8-pixel VLPC chip (see Fig. 4.4). The VLPC chip was patterned using S1813 (a positive resist) to expose a single pixel of the VLPC chip. A 90-second buffered-oxide etch (BOE, 10:1 NH_4:HF) was used to remove the single-layer, SiO_2, AR coating, which is $\sim$ 80 nm thick. The exposed, degenerate top contact was then dry etched using a Trion Technology Minilock II reactive-ion etcher (RIE). The RIE etch is a single-step, Cl_2-based process and is used to remove about 160 nm of Si with a 30-second etch (see Table 4.1). The etch rate of the RIE process is sensitive to the chamber conditions and the amount of exposed Si. Prior to the VLPC contact etch, the etch rate of the RIE process is calibrated using a test sample. After the RIE etch, the S1813 mask layer is removed in acetone.

The etched VLPC sample is next patterned using S1813 to expose the same pixel

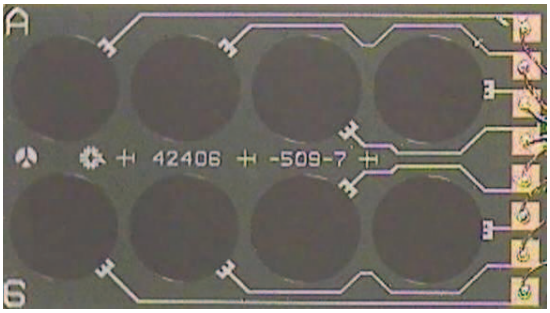

FIGURE 4.4: Picture of a standard 8-pixel VLPC chip. Each pixel has a circular aperture with a diameter of 1 mm. Aluminum traces connect each device to a gold wire-bond pad.

Table 4.1: Process parameters and recipes for the etching and deposition processes used to fabricate the Ti/MgF_2 Schottky contact of the UVPC

Process	Tool	Power	Pressure	Gas	Rate
Si dry etch	Trion Tech. Minilock II	180 W (ICP) 125 W (RIE)	10 mTorr	Cl_2	5 nm/s
RF sputter etch	Kurt Lesker PVD 75	70 W (RF)	5 mTorr	Ar	2 nm/min
Ti deposition	Kurt Lesker PVD 75	250 W (RF)	5 mTorr	Ar	5 nm/min
MgF_2 deposition	Kurt Lesker PVD 75	140 W (RF)	5 mTorr	Ar	1 nm/min

that was etched but with a slight overlap of the metal traces (see Fig. 4.4) to ensure that the deposited metal contact is connected to the Al metal trace. A 10-second BOE etch is used to remove any native oxide on the Si surface and the chip is loaded into a Kurt Lesker PVD 75 RF sputter system and pumped to a base pressure of 2×10^{-7} Torr. The exposed contact area is then cleaned using an RF sputter etch (see Table 4.1) for 5 minutes that etches an additional 10 nm of the VLPC Si contact. This etch is the critical step to the formation of a high p-type barrier for several reasons. First it produces in a clean surface by removing any surface contaminants that form interface states and reduce the barrier [89]. The etch also removes the H passivation layer from the surface, which reduces the p-type barrier for the Ti/Si

system [88]. Finally, the Ar etching process can lead to a buildup of positive charge at the interface that increases the p-type barrier [90].

After the 5-minute RF-sputter etch, the RF power of the Ti target is ramped to 250 W over a 3-minute time period during which the RF-sputter etch continues to etch the Si surface. A 10 nm thick Ti layer is then sputtered immediately after shutting off the RF-sputter etch to reduce any reaction with the reactive Si surface and the ambient Ar environment. A thickness of 10 nm was chosen to balance the transmissive properties of the Ti film while maintaining a uniform, high-conductivity contact layer. Following the Ti sputter deposition, ~ 56 nm of MgF_2 was sputtered at an RF power of 140 W. The deposition rate of the MgF_2 coating was monitored by measuring the reflectivity of a Si monitor sample during the deposition. A 10 nm color filter centered at 365 nm was used to spectrally filter a broadband source, which was reflected off the Si monitor sample and focused onto a optical power meter. Following the deposition of the Ti/MgF_2 contact layer, the S1813 resist mask was removed by an ultrasonic clean in acetone. The device was then packaged and wire bonded for testing.

The use of a MgF_2 AR coating was critical to preserving the quality of the thin Ti contact layer. Ti oxidizes rapidly when exposed to air. Because the Ti film is thin, any oxidation of the Ti significantly reduces the conductivity of the film. Decreased conductivity leads to a lateral gradient in the effective applied bias to the device. The QE and dark counts of the VLPC have a strong dependence on the applied bias and associated electric field. To prevent exposure of the Ti film to oxygen, the MgF_2 coating was deposited in situ with the Ti coating. Additionally, the use of O-containing, AR-coating materials such as SiO_2 and HfO_2 caused a reaction with the Ti film and reduced the effective thickness and conductivity of the Ti film.

4.3 UVPC Testing

For any high-precision, high-sensitivity measurement, such as single-photon detection, the measurement setup and testing methodology have a major impact on the quality of results. For testing of the UVPC, a cryostat is necessary to reach the low operating temperature of 7 K. Additionally, the sensitivity of single-photon detection measurements requires the use of low-noise electronics and low-noise measurement techniques. The design and operation of the cryostat, the design of the readout circuits and associated electronics used to test the UVPC, and the optical system used for characterizing the optical coatings of the VLPC and measuring the QE of the UVPC is detailed in this section.

4.3.1 The Cryostat

The cryostat was designed to fulfill several requirements: low-cost and stable, low-temperature operation; low-noise electrical measurement; fiber-based optical access from 300 nm to 800 nm; and shielding of blackbody radiation sources. Operation at 7 K typically requires the use of liquid helium, which has a boiling point of 4.2 K and is expensive ($\sim$ \$8/liter) compared to liquid nitrogen (boiling point 77 K, $\sim$ \$0.05/liter). Cryostem-type cryostats consume much less liquid helium during operation and allow for weeks of VLPC operation compared to days or less for flow-type cryostats [91]. Coaxial cables can be used to transmit signal into the cryostat, and a combination of multi-mode and single-mode fibers can be used to provide optical access.

Mechanical Design

A schematic of the cryostat is shown in Fig. 4.5. The top box contains the electrical and fiber feedthroughs used to transmit electrical and optical signals to the VLPC and associated electronics. Six coaxial cables are used for low-noise connections, such

as bias and signal lines. The coaxial cables have stainless-steel shields and conductors to minimize the low-temperature heat load. Two 25-pin d-sub connectors are used for electrical connections to less sensitive electronic components, such as heaters and temperature sensors. A 1.5-in.-outer-diameter, stainless steel tube is used to provide structural support for the stem. Similar to the smaller 0.5 in. tube, this tube is made from stainless steel to reduce any heat transfer from the room-temperature side to the cold side. The outer diameter of the tube is reduced to minimize the thermal conductance. The cold end of the cryostem is made from oxygen-free, high-conductivity (OFHC) copper, which has excellent thermal conductance and minimizes any temperature gradient within the cold section. The cryostat is designed to operate under vacuum to minimize thermal conductance and to prevent condensation of room air on sensitive electronics. A pumping port is located near the top box so that the cryostat can be connected to a pumping system. The vacuum seal on the cold end is provided by the brass can that covers it. Two matching, conical surfaces and a thin layer of vacuum grease provide a leak-free, room-temperature seal. When the cryostem is cooled down, the difference in the coefficient of thermal expansion for brass and copper results in a reliable, low-temperature, vacuum seal.

The VLPC is mounted on a subassembly, which is thermally isolated from the cryostem by two Delrin rods. The subassembly has a support for holding a temperature sensor and a 28-pin, chip-carrier socket. The use of a 28-pin chip carrier offers a standardized packaging solution and allows for significant flexibility on what types of samples can be mounted in the system. A fiber is secured in the base of the chip socket, which is aligned to a specific location on the chip carrier. When optical measurements are made, the chip carrier has a weak thermal link to the stage and temperature sensor. To improve the temperature uniformity, the cryostat is typically operated with a small background of helium exchange gas (< 1 torr). The stage can be reconfigured to accept different fiber inputs or different carrier designs. The fiber

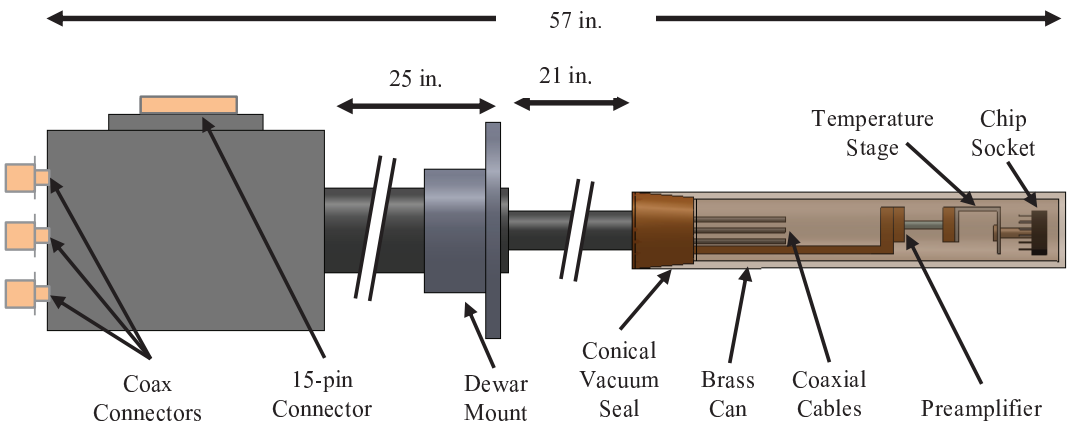

FIGURE 4.5: Schematic of the UVPC cryostat. The cryostat is designed for long term operation at low temperatures. It is typically operated under vacuum or with a small amount of exchange gas with a low temperature vacuum seal provided by a conical seal. The bulk of the cryostat is made from stainless steel to reduce the thermal conductance of the cryostat. The cold end is made from copper and brass to improve temperature uniformity. The UVPC is mounted on a chip carrier which is held by the chip socket.

used for testing the UVPC is a 200 μm core, high-OH, Silica/Silica multimode fiber that has relatively low attenuation levels ($<$ 0.2 db/m in range of $300 - 800$ nm), which do not change significantly at low temperatures and can guide radiation from 300 nm to 1.1 μm.

Blackbody Radiation

The VLPC is especially sensitive to infrared radiation from $\sim$ 3 μms to 30 μms. Blackbody radiation from all sources must be effectively shielded to ensure high-QE and low-dark-count operation for the VLPC. A blackbody source at 20 K emits about 10^6 photons/sec-cm^2 in the $4-30$ μm spectral range, which is easily enough to flood the detector and prevent reliable operation. In comparison, a blackbody source at 12 K emits fewer than 1 photons/sec$\cdot$cm^{-2}. The cold zone of the cryostem is made with OFHC copper and enclosed in a brass can, which keeps the entire cold zone cold enough to prevent significant blackbody radiation. Additionally, radiation shields are mounted at different points along the cryostem tube to block radiation from warmer

parts of the cryostem. All of the wires, cables, and electrical components are heat sunk to minimize the amount of blackbody radiation that could be absorbed by the VLPC. Another important source of blackbody radiation to consider is the fiber. If the fiber is not properly heat sunk or is able to guide any blackbody radiation, the radiation will be directed onto the VLPC surface. The multimode fiber used is heat sunk and cooled by the exchange gas. Additionally, this multimode fiber has increased absorption at long wavelengths leading to effective radiation shielding of the VLPC.

4.3.2 Readout Circuits

The readout circuit is a critical part of any single-photon detector. The circuit is responsible for amplifying the low-level signal output by the detector and converting it to a signal that is reliably discriminated against the background noise. The readout circuit for the UVPC consists of a low-temperature amplifier and room-temperature electronics, including additional amplifiers and filters (see Fig. 4.6).

Low-Temperature Amplifiers

A low-temperature preamplifier was used because the stainless-steel coaxial cables used to transmit signals from the cold end to the room-temperature connectors are very lossy (5 dB loss at 500 MHz). To correct for this loss, a low-power, GaAs-based RF amplifier (Avago Technologies MGA-81563), which provides about 10 dB gain with a 500 MHz bandwidth, was used as a preamplifier. The amplifier is designed for operation within the $0.1 - 6$ GHz range. At those frequencies, the amplifier has a gain of about 13 dB and a low noise figure. However, the response at low frequency is poor due to limitations of the internal feedback circuit. To extend the bandwidth to low frequency, an external feedback circuit was added, which flattened the gain response and resulted in a relatively flat 10 dB gain over a $5 - 500$ MHz bandwidth

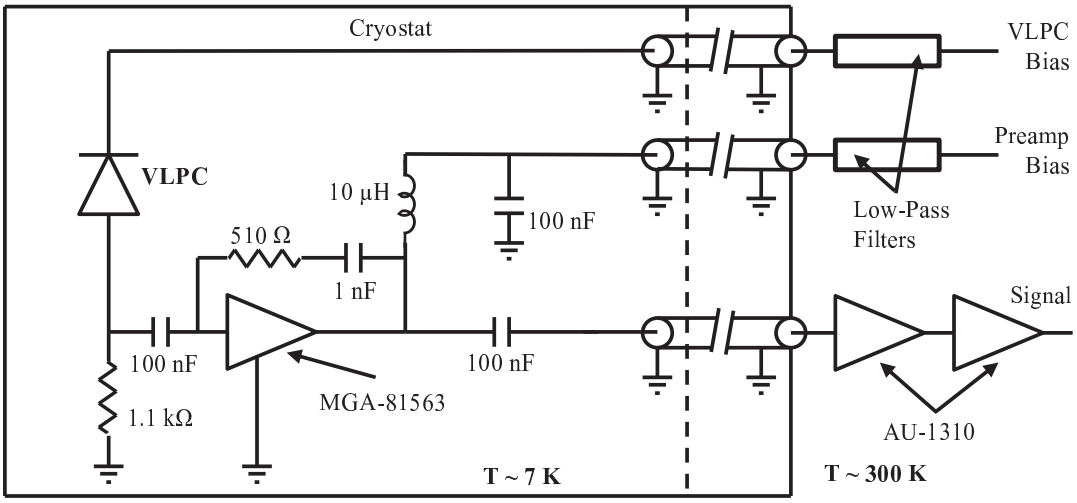

FIGURE 4.6: Readout electronic circuit for the VLPC. A low temperature preamplifier (MGA-81563) is used to compensate for lossy coaxial cables. Using an external feedback circuit the preamplifier provides 10 dB of low noise gain from 5 to 500 MHz. The VLPC signal is further amplified by two Miteq AU-1310 amplifiers which have 27 dB of broadband gain and a low NF. Low pass filters are used on the VLPC and preamplifier bias lines to remove any power supply noise.

(see Fig. 4.7). A GaAs-based amplifier was used because Si amplifiers freeze out at temperatures below 40 K. GaAs-based amplifiers are still able to operate at the low temperature of 7 K with minimal degradation in the gain response. Additionally, at low temperatures, the necessary bias voltage was reduced from 3 V to $0.3 - 0.6$ V with a current of 20 mA resulting in a low-power, low-noise preamplifier with about 10 dB gain.

Room-Temperature Electronics

Two Miteq AU1310 amplifiers were used to amplify the VLPC signal pulse at the output of the cryostat. The Miteq amplifiers are low-noise (noise figure (NF) = 1.4), broadband ($0.01 - 500$ MHz), high-gain (27 dB) amplifier modules that are well filtered. The resulting pulses show good signal-to-noise ratio (SNR, see Fig. 4.8) and fast time response (see Fig. 4.9). The Miteq amplifiers are relatively expensive. For multi-channel operation, a lower cost option is preferable. An alternative option

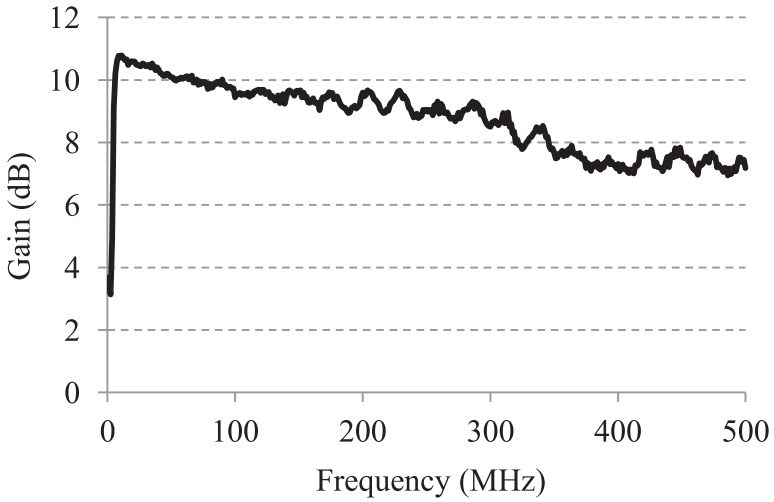

FIGURE 4.7: Gain of the MGA-81563 low temperature preamplifier as a function of frequency. The ripple in the gain response is due to a slight impedance mismatch.

for room-temperature amplifiers are California Eastern Laboratories UPC3215TB amplifiers, which have 20 dB gain over a 3 GHz bandwidth at a slightly higher NF of 2.3. These amplifiers can be cascaded to achieve similar gain, and the cost of these amplifiers is several orders of magnitude less ($2 each).

In addition to using high-quality cryogenic cables and low-noise amplifiers, it is necessary to use appropriate filters and practices to minimize noise in the measurement. A spectrum analyzer is used to monitor the noise spectrum of the VLPC and the amplifiers to ensure that the background noise is white and has no defined peaks. Peaks in the spectrum are generally a result of pickup or coupling of some noise source into the circuit and can completely wash out the actual signal. For the VLPC system, the largest sources of noise were the bias lines for the low-temperature amplifier and the VLPC, and the temperature sensor and heater. By using simple, low-pass filters, noise was removed from the bias lines resulting in a clean noise spectrum and signal pulses that were easy to discriminate. A Stanford Research System SR400 photon counter was used for discriminating and counting detection pulses for the QE measurements.

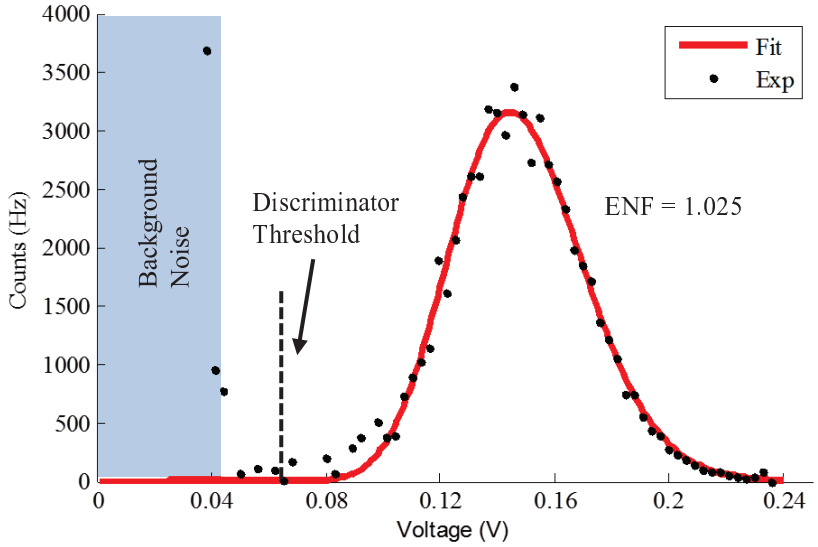

FIGURE 4.8: Histogram of UVPC pulse heights. The pulse height distribution shows an excellent fit to an ENF of 1.025 which shows that the gain properties of the UVPC were not affected by the modified contact. The pulse height distribution is clearly seperated from the background noise and the discriminator level is set to 55 mV.

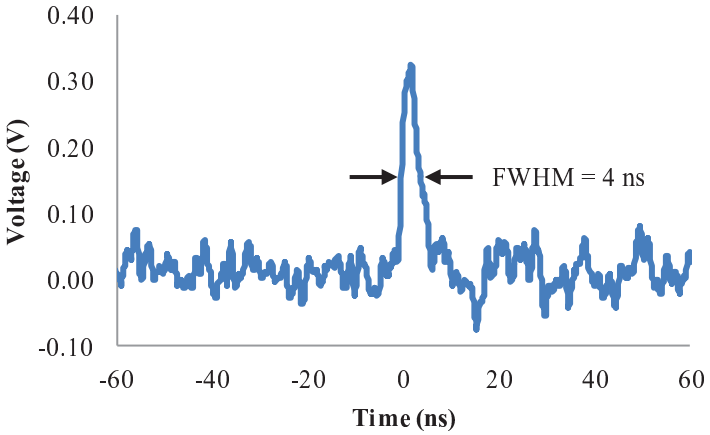

FIGURE 4.9: Single photon detection pulse of the UVPC. The pulse shows a good signal-to-noise ratio with a fast time response (FWHM = 4ns).

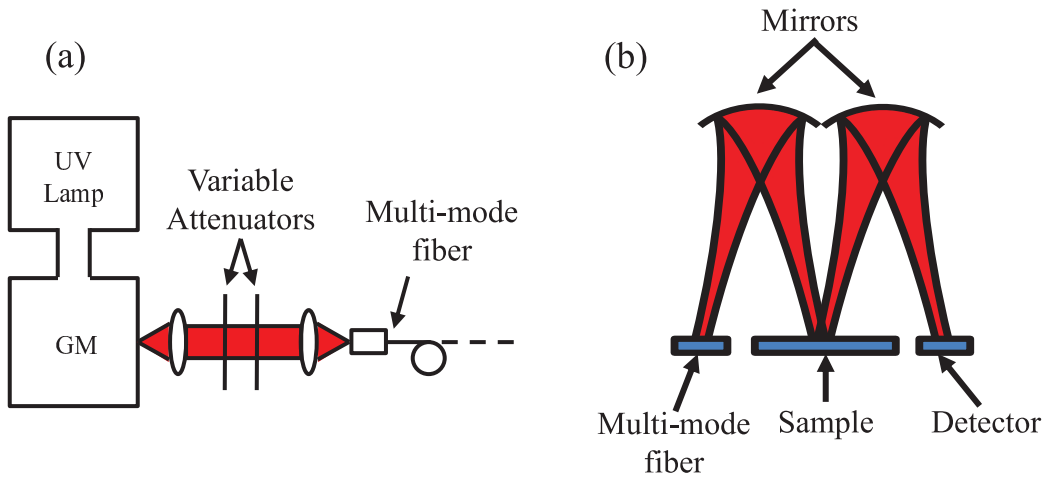

FIGURE 4.10: (a) A broadband, UV-enhanced lamp is spectrally filtered using a grating monochromator, attenuated to the desired photon flux using a series of variable attenuators, and coupled into a multi-mode fiber. (b) A set of curved mirrors are used to focus the output of a multi-mode fiber onto a sample and then the reflected power onto a detector.

4.3.3 Optical Setup

A 500-W, UV lamp, which has a broad spectral distribution, was filtered with a grating monochromator to provide a continuous wave source of photons with a ~ 2 nm spectral bandwidth over a wavelength range of $270 - 650$ nm (see Fig. 4.10(a)). A series of variable attenuators was used to attenuate the photon flux to the desired level, and the resulting photon flux was coupled into a multi-mode fiber. The multimode fiber was a 200 μm core, multi-mode fiber with a silica cladding and a silica core with high OH^- concentration to reduce attenuation at UV wavelengths. The multi-mode fiber could then be connected to a cryostat for measuring the QE of a VLPC or UVPC device, or to a reflectivity-measurement setup.

The reflectivity-measurement setup is shown in Fig. 4.10(b). The output of the multi-mode fiber is focused by a concave mirror onto the sample to be measured, and the reflected beam is then refocused onto a Si detector. The output of the detector is connected to a lock-in amplifier, which, in combination with an optical

chopper on the input, reduces the impact of background radiation on the reflectivity measurement. Curved mirrors were used instead of lenses to eliminate chromatic aberrations and allow for measurement over a broad spectral range ($270 - 650$ nm). The reflectivity was measured at an angle of 10° from normal. The reflectivity of the sample is calibrated by comparing the measured reflected power of the sample to the measured reflected power of a Si sample. The actual reflectivity of the sample, R_{sample}, as a function of the wavelength is then calculated using

$$R_{sample} = \frac{\text{sample reflected power}}{\text{Si reflected power}} R_{Si}, \tag{4.1}$$

where R_{Si} is the theoretical reflectivity of Si at the desired wavelength.

4.4 QE of the UVPC

The system QE of the UVPC in the $300 - 400$ nm wavelength range is shown in Fig. 4.11. The system QE is defined as the ratio of the number of photons detected (resulting in an electrical pulse) to the number of photons incident on the system. The input point of our system is defined to be the UV-enhanced, multi-mode fiber connector at the room-temperature end of our cryostat. The system QE of the UVPC, which had a single-layer, MgF_2, AR coating optimized for ~ 370 nm, was $5.3\% \pm 0.5\%$ at 300 nm and $11\% \pm 1\%$ at 370 nm. The UVPC was operated at a device temperature of 7.1 K and a device bias of 7.25 V. The dark counts at these operating conditions were $\sim 16,000$ counts per second. The incident photon flux at each wavelength was set to 2×10^5 photons per second with an uncertainty of ± 0.4 dB, which was dominated by fiber connector loss uncertainty at the system input.

The internal QE of the UVPC was estimated by accounting for several sources of loss in the system. The internal QE is defined as the ratio of the number of photons detected (resulting in an electrical pulse) to the number of photons transmitted through the front contact. The attenuation of the 1.7-m-long, UV-enhanced,

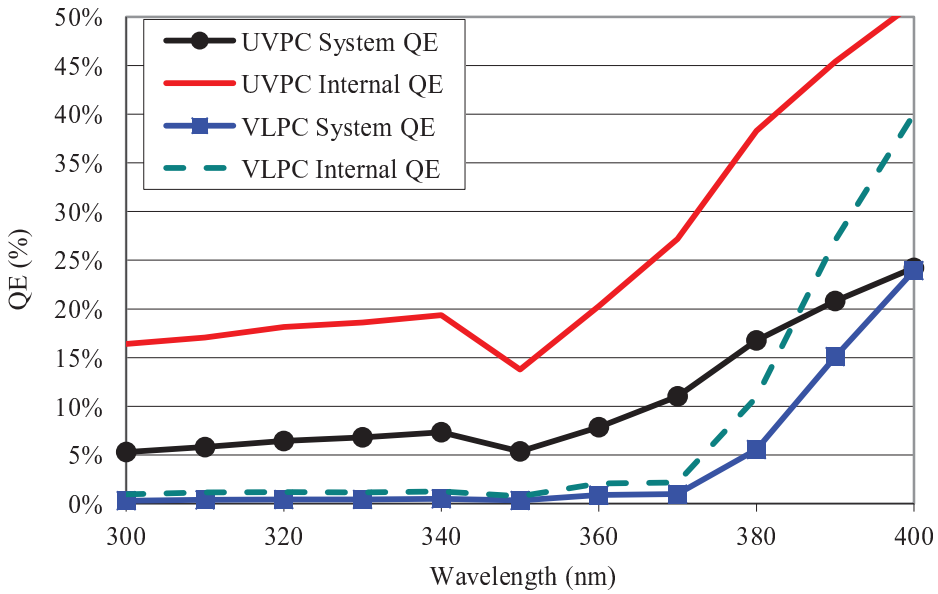

FIGURE 4.11: The system QE and estimated lower bound for the internal QE of the UVPC and VLPC from $300 - 400$ nm. The internal QE is estimated by accounting for losses in the fiber, output coupling efficiency, and detector coatings.

multi-mode fiber that runs down the cryostat has wavelength-dependent attenuation ranging from 0.2 dB/m to 0.05 dB/m in the $300 - 400$ nm wavelength range. Misalignment of the fiber to the detector reduces the output coupling efficiency of the fiber to an estimated 90%. The transmissive, absorptive, and reflective characteristics of the Ti/MgF_2 contact were simulated using ideal index values for the real and imaginary parts of the refractive index of the materials involved. The transmission values used in estimating the internal QE were the simulated values. Therefore, the reported internal QE values shown in Fig. 4.11 provide a lower bound on the actual internal QE of the UVPC. With these corrections, an estimate of the lower bound of the actual internal QE of the UVPC is 16.5% at 300 nm and 27% at 370 nm.

The estimated internal QE of the UVPC is below the internal QE of the VLPC ($\sim$ 95% at 694 nm). The measured reflectivity of a single layer MgF_2 optimized for transmission at 370 nm in comparison to the simulated values of the reflectivity for bare Si and the same single layer MgF_2 coating is shown in Fig. 4.12. Over the entire

measured spectrum, and particularly in the UV part of the spectrum, the measured reflectivity is lower than the theoretical values. The lower reflectivity can be caused by increased scattering at different layer interfaces or higher absorption compared to an ideal film. The root-mean-square (RMS) surface roughness, σ_r, of a reflective surface decreases the normal incidence spectral reflectance, R_s, by [92]

$$R_s = R_0 \exp\left[-\frac{(4\pi\sigma_r)^2}{\lambda^2}\right], \tag{4.2}$$

where R_0 is the specular reflectance for the surface with no surface roughness, and λ is the wavelength of the incident light. The decreased spectral reflectance due to surface roughness results in increased diffuse reflections. An atomic force microscope (AFM) was used to measure R_a for the RIE etched and RF sputtered Si surface ($R_a < 2$ Å) and the MgF_2 AR coating surface ($R_a \approx 11$ Å), which over the wavelength range of $300 - 650$ nm should lead to a decrease in the measured reflectivity of less than $\sim 1\%$).

Increased absorption in the sputtered MgF_2 film due to high defect and impurity concentration in the MgF_2 film can increase loss in the reflectivity measurement and reduce the measured reflectivity of the AR coated UVPC surface. Multi-layer AR coatings ($MgF_2/HfO_2/MgF_2$) resulted in only marginal improvements to the QE of the UVPC, presumably due to the higher absorption in the sputtered MgF_2 and HfO_2 films, and the increased thickness of the multi-layer AR coating. Higher quality AR coatings should be able to increase the QE of the UVPC. The measured and simulated values of a single layer SiO_2 coating is also shown in Fig. 4.12. The measured reflectivity values support the theory, which helps to confirm the accuracy of the reflectivity setup and the simulation values. Reaction of the SiO_2 coating with the Ti prevented successful operation of Ti/SiO_2 UVPC devices.

The lower internal QE at UV wavelengths indicates that there is significant ab-

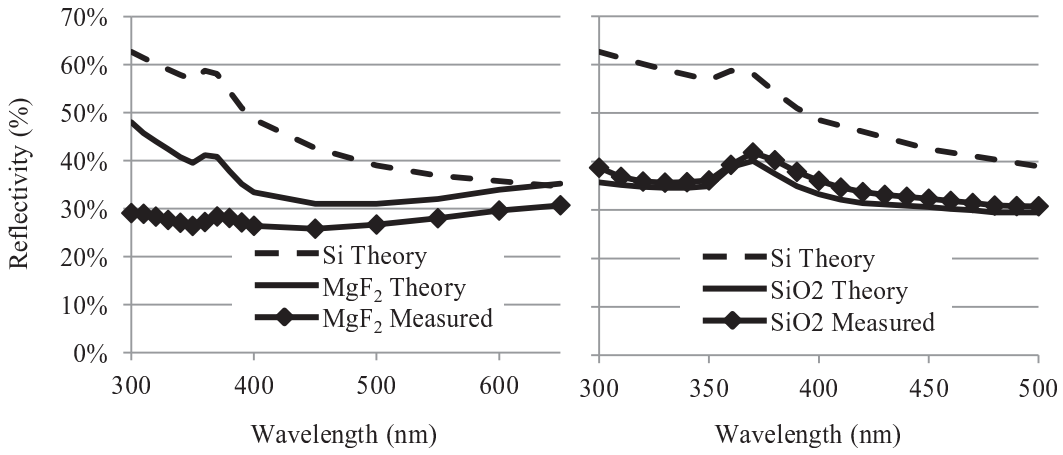

FIGURE 4.12: Plots of the reflectivity of single-layer, RF-sputtered, MgF_2 and SiO_2 coatings on Si. The measured value of the MgF_2 AR coating is significantly lower than the simulated values indicating that the film is significantly more absorptive than the ideal film. In contrast to the MgF_2 film, the measured reflectivity of the SiO_2 film agrees well with the simulated values.

sorption within the contact area of the UVPC. The thickness of the original degenerate front contact of the VLPC is $\sim$ 250 nm. The highest QE for the UVPC was observed when $\sim$ 160 nm of the front contact was etched, leaving $\sim$ 90 nm of the original contact layer intact prior to deposition of the Ti/Mg_2 Schottky contact. Shallower etching ($<$ 160 nm) resulted in reduced QE due to increased absorption within the remaining contact. Deeper etching ($>$ 160 nm) also resulted in reduced QE. As more of the front contact is etched (resulting in fewer dopants), the impact of etch related defects becomes greater and results in reduced QE.

5

InGaAs/Si Wafer Bonding

The integration of different semiconductors to form heterojunctions is typically realized through epitaxial-growth techniques. A critical requirement for epitaxial growth is lattice-constant matching between the host substrate and the epitaxial material. Any mismatch in the lattice constants results in defects or dislocations. There are two major types of dislocations: edge dislocations and screw dislocations (or threading dislocations). Edge dislocations can be thought of as an extra row of atoms (see Fig. 5.1) and are typically confined to the interface. Screw dislocations are a slip in the crystal lattice resulting in a helical-like string of dislocations, which can propagate through the material. Both types of dislocations are undesirable and can act as carrier traps or emitters that degrade the operation of a device, particularly for photonic devices [93]. The lattice matching constraint severely limits the set of materials that can be grown together with relatively few defects.

An alternative means of realizing heterojunctions is through the use of wafer-fusion bonding [58, 59]. Wafer-fusion bonding (also called direct bonding and hereafter referred to simply as wafer bonding) is the process in which two materials are

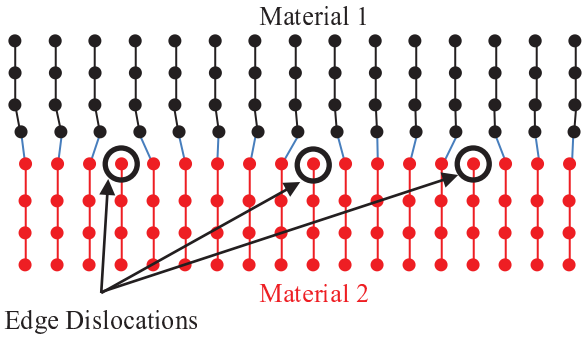

FIGURE 5.1: Schematic showing an example of edge dislocations. Material 1 has a larger lattice constant than material 2. Atoms near the surface will shift a little to accomodate the mismatch but dislocations will form at regular intervals.

brought into contact and permanently fused together. No "glue" layer is used to join the materials and covalent bonds are formed directly between the two materials. Wafer bonding supplants the lattice-matching restriction and allows practically any set of materials to be integrated. While the mismatch in lattice constants will still result in dislocations, these dislocations are typically confined to the interface plane and do not propagate through the crystal structure. Wafer-bonded interfaces have been used in a number of advanced heterojunction devices and have enabled a new generation of electronic and optoelectronic devices [93, 94, 60, 52, 53, 57, 61].

While wafer bonding can be used for bonding identical materials (such as Si/Si bonding), this thesis work focuses on the development of a heterojunction device. Thus, the discussion on wafer bonding will focus on bonding dissimilar materials, though for bonding similar materials many of the same principles apply. This chapter starts with an introduction to wafer bonding in Section 1. In Section 2, details of the InGaAs/Si wafer-bonding process, which is important for the development of the infrared photon counter, are described. The measurement and evaluation of the band alignment of the InGaAs/Si heterojunction is presented in Section 3.

5.1 Introduction to Wafer Bonding

5.1.1 Principles of Wafer Bonding

The wafer-bonding process can be broken down into three steps: surface preparation, room-temperature bonding, and a heat treatment. Polished wafers are physically and chemically cleaned of any surface particles and then brought into contact at room temperature. The wafers are then annealed to strengthen the interface bonds. The primary requirements for wafer bonding are that the wafers be smooth, flat, and clean [95]. If these requirements are met, when the wafers are brought into contact, intermolecular Van der Waals bonds will form and keep the wafers together. When the wafers are heat treated, strong covalent bonds will form between them.

Van der Waals bonds are weak, intermolecular bonds that form as a result of dipole-dipole attraction. This attraction can form between molecules that are polar or non-polar. Non-polar molecules will form temporary dipoles due to the movement of electrons within the molecule. Polar molecules have permanent dipoles, and the dipole attraction will be stronger than that of non-polar molecules. These temporary or permanent dipoles will attract other dipoles and form Van der Waals bonds.

The first requirement for wafer bonding is that the wafers be smooth. Smoothness of wafers is a measure of microscopic variations of the surface in contrast to flatness, which is a measure of macroscopic variations. The strength of Van der Waals bonds has a power law decrease as the distance between molecules is increased [96], so it is important for the surfaces to be close together. Any roughness of the wafers limits the surface area of the wafer that can form Van der Waals bonds. A general rule is that the spacing between the wafers should be on the order of the lattice constants of the wafers, which translates to a root mean square (RMS) roughness of less than 1 Å [97]. If the surfaces of the wafers are terminated with polar molecules, such as H, F, O, or N, stronger forces will exist between the wafers, relaxing the roughness

constraints. Generally, wafers under these conditions can be bonded with an RMS roughness of less than 5 Å.

The second requirement is that the surfaces of the wafers should be flat. If the surfaces are excessively bowed or wavy, there will be gaps between the surfaces when the wafers are brought into contact. Depending on the strength of the bond between the two surfaces, the wafers will elastically deform and conform to each other to close the gaps [59]. This elastic deformation becomes easier with thinner wafers. Consequently, when bonding wafers with large thickness variations, thinning one or both of the wafers can help increase the success rate of the process.

The third requirement is that the wafers be free of particles and surface contaminants. The existence of small particles on a surface can lead to bubbles or failed bonding for areas many orders of magnitude greater than the size of the particle. For example, a 1 μm particle on the surface of one of two 4-inch Si wafers will lead to an unbonded area of 0.5 cm^2 [97]. Surface contaminations, such as organics, can outgas during the high-temperature anneal. That gas, without means of escape, will be trapped at the interface forming bubbles (see Fig. 5.2).

In general, there are two classes of wafer bonding: hydrophylic bonding and hydrophobic bonding [59]. For hydrophylic bonding, the wafer surfaces are covered in an oxide before bonding (referred to as a hydrophylic surface due to its interaction with water). The oxide can either be chemically grown prior to bonding or simply be the native oxide that grows on most surfaces. Surfaces coated in oxide tend to be easier to bond due to the polar nature of such surfaces. Activation methods can result in strong bonding at lower temperatures compared to hydrophobic bonding [98, 99, 100, 97]. For hydrophobic bonding, surface oxides are removed prior to bonding and formation of any oxides at the interface degrades the properties of the junction. For devices where ohmic conduction across the interface is important, any oxide should be eliminated, as oxide acts as a barrier to carrier transport.

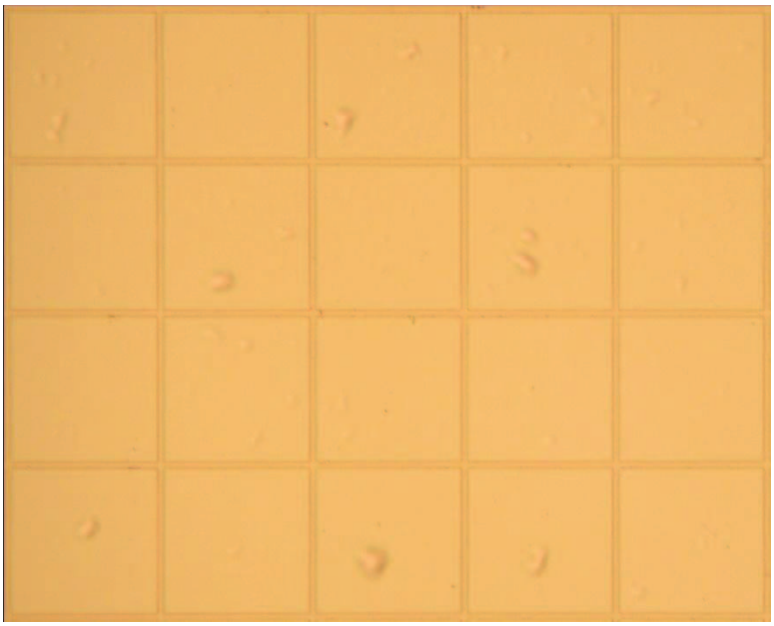

FIGURE 5.2: Picture showing an example of bubbles at the interface of a wafer bonded heterojunction. The wafer bonded InGaAs layers are thin so any interface bubbles are easy to observe under an optical microscope. Bubble formation at the interface can be avoided with the use of the high thermal stress method, intermediate annealing steps to allow for outgassing, and the use of etched channels to allow trapped gas to escape the interface.

5.1.2 The Bonding Process

A general process flow for wafer bonding starts with cleaning polished wafers. Typically, a mix of solvent- and acid-based cleaning processes is used to remove metallic and organic contaminants as well as any particulates from the wafer surfaces. The two surfaces are then put into contact and, typically, a small amount of pressure is applied to trigger the bonding process. The wafers should then be held together by Van der Waals bonds. Heat treatment is then necessary to break the initial bonding configuration of the individual surfaces and form covalent bonds between the wafer surfaces. When bonding dissimilar materials, differences in the coefficient of thermal expansion (CTE) cause significant build-up of stress at the bonding interface. This thermal stress causes deformation of the wafers and typically bond failure and signif-

icantly reduces the yield of the bonding process. One technique for bonding wafers with different CTE is the high-thermal-stress (HTS) method [94, 101, 58].

High-Thermal-Stress Method

The HTS method involves applying a large, uniaxial pressure to the bonded wafer pair during the heat treatment. The applied pressure forces the bonded wafers to remain in intimate contact during the anneal and prevents any peeling or bowing of the wafers. At high temperatures, the surface bonds will break and covalent bonds will form between the wafers. In addition to the applied pressure, the thermal stress will result in significant strain at the bonded interface. As the wafers are cooled, the wafers will need to relax or slip to accommodate the interface strain, which results in formation of dislocations at the interface [58]. In addition to accommodating for the thermal stress at the interface, the applied pressure also helps to force intimate contact between the surfaces to prevent the formation of bubbles and voids at the interface. Any gas trapped at the interface is forced to diffuse out of the interface by the applied pressure. An additional means of reducing interface bubbles is to use etched channels or grooves in one or both of the wafers surfaces to allow a means for trapped gas to escape the interface without having to diffuse through the entire interface [94, 102]. The HTS process is the most commonly used method for bonding dissimilar materials and high-yield, low-bubble-density bonding has been reported for a number of different material systems [94, 103, 104, 101, 58, 97].

After the heat treatment, one of the substrates is typically thinned or removed. For transfer of epitaxial layers, selective etches and etch stops can be used to remove one of the substrates without damaging the epitaxial layers and result in the transfer of epitaxial layers to the new host substrate. In the case of bulk wafer bonding, mechanical thinning can be used to thin one or both of the wafers [93]. Due to the strong bond energy of covalent bonds, the wafer-bonded interface will remain intact

during this process.

Low-Thermal-Stress Method

The low-thermal-stress (LTS) process is a bonding technique that can significantly reduce the thermal stress at the bonding interface and, consequently, reduce the dislocation density at the interface [102, 58]. The thermal stress at the bonding interface is proportional to both the bonding temperature and the thickness of the wafers. Since reducing the temperature is not an attractive option as it leads to non-covalent, lower-strength bonds, the best option is to reduce the thickness of one of the wafers (several micrometer). The thinner wafer can then more easily accommodate the thermal stress through elastic deformation, which doesn't result in the generation of dislocations. Handling and bonding very thin wafers is difficult to achieve practically. Preferably, the wafer is thinned after room-temperature bonding. Selective etch techniques are the best way to achieve this as the weak, room-temperature bonds are unlikely to survive mechanical thinning processes. After the wafer is thinned, the bonded wafer can then be annealed at high temperatures without any applied pressure.

Interface bubbles are much more likely to occur during the LTS process due to the thinner wafer and the lack of applied pressure. The use of etch channels or grooves is particularly important for LTS processes in helping to remove trapped gases from the interface. Another option is to anneal the bonded pair at low temperatures before thinning the substrate [58]. Pressure can be applied during this low temperature annealing step and trapped gases can diffuse from the interface. The substrate can then be thinned and the pair is annealed at high temperatures to complete the bonding process.

Ultra-High Vacuum Bonding

A third bonding method is ultra-high vacuum (UHV, $< 10^{-9}$ Torr) bonding. UHV bonding allows for complete control over the wafer surfaces prior to bonding. Impurities such as C, O, and H can be removed from the bonding interface [105, 106], enabling nearly ideal bonded interfaces [59]. Highly reactive surfaces can be prepared, which enables room temperature bonding [107, 108, 98], eliminating the problems associated with different CTE and opening up the possibility of bonding fully-processed devices that cannot be heat treated without degrading or destroying processed layers. The control of the bonding interface provided by the UHV environment is particularly useful as the bonding interface plays a critical role to the electrical properties of heterojunction devices.

5.1.3 Interface Characterization

The electrical properties of the wafer-bonded heterojunction are greatly influenced by several interface properties: the bubble and void density, the dislocation density, and the band alignment. Characterizing these properties is an important part of optimizing a particular wafer-bonding process and designing heterojunction devices. A variety of techniques, including microscopy, spectroscopy, and electrical measurements, are especially useful in characterizing these properties of wafer-bonded interfaces.

Interface Bubbles and Voids

Optical inspection is the fastest and easiest way to check the bonding interface for bubbles and voids. If one of the wafers is thin or transparent to visible or IR wavelengths, bubbles and voids can be visualized easily and characterized with the use of traditional microscopes or infrared cameras (see Fig. 5.2). Alternative non-destructive techniques include acoustic microscopes and X-ray topography [59].

Destructive measurements, such as interface etching and transmission electron microscopy (TEM), are useful in characterizing micro-sized bubbles and voids. However, these techniques are time consuming and, in the case of TEM, the measurement also has a small field of view and is expensive. The density of bubbles and voids typically can be reduced through increased mechanical pressure, etched channels to remove gases from the interface, outgassing stages in the annealing process, and better cleaning to remove organic contaminants and particulates.

Dislocations

Reducing the dislocation density of wafer-bonded interfaces is critical for the use of wafer-bonded heterojunctions in electronic or optoelectronic devices. An unavoidable source of dislocations results from a difference in the lattice constants. However, these dislocations are typically confined to the interface plane and do not propagate through the material. Thermal-stress-induced dislocations can be minimized with the use of LTS bonding or low-temperature bonding in UHV. An additional source of dislocations results from angular misalignment of the wafer-bonded interfaces [109, 110, 111]. If the crystal planes are not parallel, any misalignment induces networks of threaded dislocations. Characterizing dislocation densities is usually achieved through the use of TEM. TEMs are able to directly image the lattice structure of crystals by measuring the diffraction of transmitted electrons. The wavelength of high energy electrons is very small ($<<$ 1Å); consequently, TEMs are able to resolve features $<$ 1 Å and image individual lattice sites. Dislocations can be directly observed using TEM, and the densities of dislocations can be measured.

Band Alignment

The band alignment is a measure of how the conduction and valence bands of two materials align at the heterointerface. In most cases, the bands will not align due

to different bandgaps or interface dipoles [112, 113, 114]. Misalignment results in valence and conduction band discontinuities at the interface. The band discontinuities in the heterojunction dictate the transport of carriers across the junction, which makes it essential to understand the band alignment of a heterojunction device before designing a device. A number of theories have been proposed for predicting the band discontinuities, but at this point there is no theory that can reliably predict the band discontinuities [115, 116, 117, 114]. Additionally, the band discontinuities can be dependent on different parts of the bonding process. This makes experimental determination of the band discontinuities the only reliable way to determine the band alignment of the heterojunction. In general, there are two classes of band alignment measurement techniques: spectroscopic measurements and electrical measurements.

Measurements of the band discontinuities using optical spectroscopy rely on the absorption or emission of radiation. X-ray photoelectron spectroscopy (XPS) and ultraviolet photoelectron spectroscopy (UPS) use high-energy, incident radiation to eject electrons from core or valence levels of surface atoms. The kinetic energy of the emitted electrons can be measured to determine the initial binding energy of the electron. The binding energies of the electrons correspond to specific bonds. These energies can be used for identification of atomic concentration and bonding energy states and to directly measure the valence band energy levels [118, 113, 119, 120]. However, the probe depth of XPS and UPS is shallow, and these techniques are useful only when the interface is a few nm from the surface. The difficultly associated with bonding such thin layers limits the usefulness of these techniques for wafer-bonded heterojunctions. Other optical spectroscopy techniques are able to measure the band discontinuities by analyzing the emission or absorption spectra of quantum well structures [121, 122, 123]. Given accurate values for the carrier effective masses and well widths, the band discontinuities can be extracted. Quantum well structures are difficult to realize utilizing the wafer-bonding process and, in general,

are fabricated through epitaxial techniques. The primary means of characterizing the band alignment of wafer-bonded heterojunctions is through the use of electrical measurements.

One means of determining the band alignment of heterojunctions through electrical measurements is through the use of Capacitance-voltage (C-V) measurements [57, 124]. The capacitance of a heterojunction is given by

$$\frac{1}{C} = \sqrt{\frac{2\left(V_{bi} - V_a\right)}{q}\left(\frac{\epsilon_1 N_{c1} + \epsilon_2 N_{c2}}{\epsilon_1 N_{c1} \epsilon_2 N_{c2}}\right)}\,, \tag{5.1}$$

where V_{bi} is the built-in voltage, V_a is the applied voltage, ϵ is the relative permittivity of each side, and N_{c1} and N_{c2} are the majority carrier doping concentrations on each side of the junction [125]. When $1/C^2$ is plotted as a function of V_a, V_{bi} can be extracted by extrapolating the curve to find the intercept where $V_a = 0$. The built-in voltage of the junction is then used to extract the band discontinuities.

Current-voltage (I-V) measurements can be used to measure the band alignment of a heterojunction [126, 127] by utilizing thermionic-emission theory [128, 129, 83, 130]. Figure 5.3 shows a schematic of a semiconductor metal interface. One of the primary transport processes at the semiconductor to Schottky metal barrier is thermionic emission. Thermionic emission is the process in which carriers with energy greater than the barrier height are able to cross the barrier. The carrier density in the band is determined by the density of states and the Fermi-Dirac function. The current across the barrier due to thermionic emission is approximately given by the integral of the carrier density for energies above the barrier. The current density, J, due to carriers crossing from the semiconductor to metal, $J_{s\to m}$, is given by

$$J_{s\to m} = A^{**} T^2 \exp\left(-\frac{q\Phi_B}{k_B T}\right) \exp\left(\frac{qV_a}{k_B T}\right), \tag{5.2}$$

where A^{**} is the effective Richardson constant, T is the temperature, and k_B is

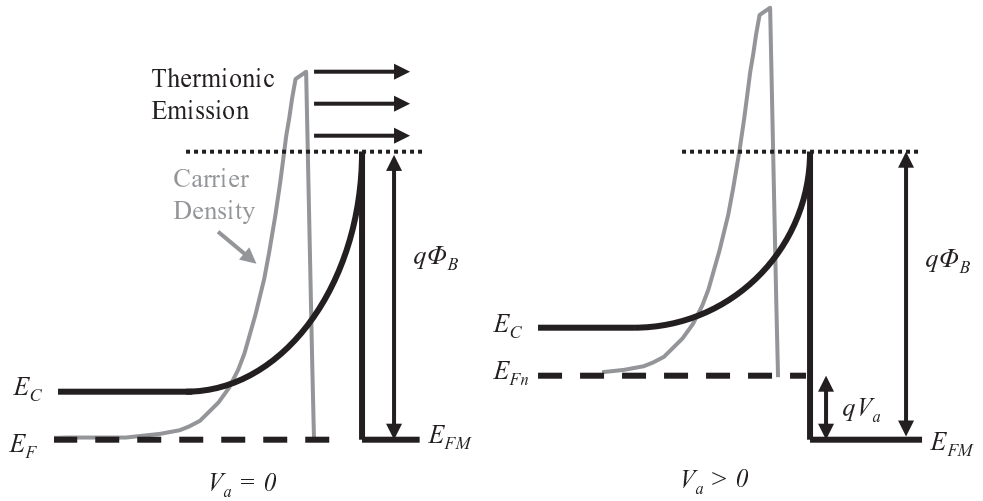

FIGURE 5.3: Schematic of a semiconductor to Schottky metal interface at equilibrium and under an applied bias. The barrier, Φ_b, between the semiconductor and the metal reduces the flow of current across the junction. Thermionic emission is a current transport process in which carriers with energy larger than the barrier are able to cross the junction. Under an applied forward bias the effective barrier is reduced and the current increases exponentially with the increasing carrier density. E_C is the conduction band, E_F is the Fermi level of the semiconductor, E_{FM} is the Fermi level of the metal, E_{Fn} is the quasi-Fermi level of the semiconductor under an applied bias, V_a.

Boltzmann's constant. As the applied voltage, V_a, increases, the effective barrier reduces and the carrier density above the barrier increases exponentially. Conversely, for the current density due to carriers crossing from the metal to the semiconductor, $J_{m\to s}$, the barrier is independent of the applied bias (to first order), and $J_{b\to s}$ is independent of the bias voltage. The total current density due to thermionic emission is the sum of $J_{s\to m}$ and $J_{m\to s}$, which at equilibrium must be zero and is

$$J = A^{**}T^2 \exp\left(-\frac{q\Phi_B}{k_B T}\right)\left[\exp\left(\frac{qV_a}{k_B T}\right) - 1\right]. \tag{5.3}$$

The barrier height, Φ_B can be extracted from the temperature and voltage dependence of the J-V measurements.

For a heterojunction, the analysis of the J-V measurements is similar. Any band

discontinuities act as a barrier to carrier transport and the barrier can be extracted from the temperature and voltage dependence of the J-V measurements. However, for a heterojunction, the applied voltage will be dropped over both sides of the heterojunction and both the forward and reverse currents will have a voltage dependence (see Sec. 1.3).

5.2 The InGaAs/Si Wafer-Bonded Heterojunction

This section will detail the specific wafer-bonding process, developed during the course of this thesis work, which was used to bond the InGaAs epitaxial layer to Si. The wafer-bonding process can be broken into three main steps: sample preparation, room-temperature bonding, and annealing. Due to the strict condition of wafer cleanliness, all stages of the bonding process take place in a cleanroom environment.

5.2.1 Sample Preparation

The sample preparation stage consists of cleaving, patterning, and cleaning the wafers. InGaAs epitaxial layers are grown on a lattice-matched InP substrate. InGaAs/InP wafers are expensive compared to Si wafers, so using entire wafers for individual experiments was prohibitively expensive. Instead, the Si and InGaAs/InP wafers are cleaved to a smaller size to increase the number of experiments that could be conducted per wafer. The cleaving process can be a major source of particle contamination for the surfaces. The first step in the cleaving process is to scribe the top surface of the wafer along the crystallographic axis with a diamond scribe. The wafer is then flipped over and slight pressure is applied in the same area as the scribe until the wafer cleaves. When the wafer is scribed on the top surface, particles can be sprayed onto the wafer surface. When the wafer is flipped over, there is a high probability that the surface will pick up additional contaminants. To reduce particulate contamination of the surface at this stage, the wafers are first covered

with photoresist [58]. Contaminants will then be deposited onto the photoresist layer rather than the wafer itself. Solvents can be used to remove the photoresist, greatly reducing the number of particles deposited onto the surface. This process is used to cleave the Si wafers into 8 mm $\times$ 8 mm pieces and the InGaAs wafers into 7 mm $\times$ 7 mm pieces.

The cleaved silicon pieces were then cleaned using the standard Radio Corporation of America (RCA) process (NH_4OH:H_2O_2:H_2O 1:1:5, RCA1; and HCl:H_2O_2:H_20 1:1:5, RCA2) for 10 minutes at 70 °C. The RCA1 solution is used to remove organic contaminants as well as particulate contaminants. The RCA2 step removes any metal contamination from the surface. The InGaAs pieces were patterned with a 300 μm $\times$ 300 μm square grid with 10 μm channels etched using an InGaAs selective etch (H_3PO_4:H_2O_2:H_2O 1:1:11). The channels were etched to allow any gas trapped at the interface to escape the bonding interface. The size of the grid and channels is not critical, and grids of up to 1 mm square were used with great success. The Si and InGaAs wafer pieces then underwent a final cleaning in acetone and isopropanol (IPA) until a microscope inspection revealed a clean surface, free of particulate contaminants. Frequently, cotton-tipped swabs are then used to gently clean the InGaAs wafer surfaces while constantly spraying the sample with acetone or IPA. The Si pieces were generally ready for bonding after the RCA clean. The clean wafer pieces were then transferred to an N_2 glove box for bonding.

5.2.2 Room-Temperature Bonding

The room-temperature bonding stage takes place inside a nitrogen glove box (in purge mode, to prevent saturation of purifiers by the HF solution) with an oxygen concentration of $<$ 1 ppm, and a moisture content of $<$ 10 ppm. To ensure that there is no oxide barrier at the wafer-bonded interface, the Si and InGaAs samples are dipped into a 5% hydrofluoric acid (HF) solution to remove any surface oxides.

After the HF dip, the Si sample should be hydrophobic, while the InGaAs sample should be wet with HF solution. Both samples are then blown dry with a filtered N_2 gun. The InGaAs piece is then pressed onto the Si and visually aligned to match crystallographic orientation. Once aligned, pressure is applied to the top of the InGaAs with a pair of plastic tweezers. The samples should be firmly stuck together due to Van der Waals forces. The samples are loaded into a graphite fixture designed to apply uniaxial pressure to the top of the bonded wafer pair. The fixture is then transported in nitrogen to an annealing furnace. The HF dip and low oxygen concentration of the glove box ensure that minimal oxides are present at the bonding interface. During transfer, the bonded samples are exposed to room air for about one minute before the furnace is pumped down and backfilled with nitrogen or hydrogen.

5.2.3 High-Temperature Annealing

The furnace chamber is a vacuum-tight (base pressure below 10^{-3} Torr) tube about 24 inches long with a 3-inch inner diameter. Prior to the heat treatment, the chamber is pumped and purged three times with N_2 to remove any oxygen or other contaminants. The chamber can then be backfilled with N_2 or H_2. The bonded pair is subjected to a two-stage anneal to convert the weak Van der Waals bonds into strong permanent covalent bonds. The first stage is an outgassing stage where the temperature is ramped slowly (2 °C/min) up to 300 °C and annealed for one hour. This stage allows any outgassing at the interface to escape through the channels etched in the InGaAs. In the second stage, the temperature is quickly ramped up (10 °C/min) to 650 °C and held for one hour during which covalent bonds are formed between Si and InGaAs. The maximum temperature of 650 °C was chosen as it is high enough for surface migration of the InGaAs but low enough that the InGaAs layer and InP substrate don't significantly decompose. After the anneal, the InP substrate was removed from the bonded sample by a long etch in an HCl solution (HCl:$H_2$0 3:1,

$\sim$ 1 hr). Through this process, the InGaAs layers were bonded and transferred to the Si surface for device processing.

5.2.4 Bonding Results

The bonding yield for the InGaAs/Si wafer-bonding process described previously was $\sim 80\%$ or higher as measured by the bubble-free, transferred area. During the substrate removal etch, any unbonded areas are separated from the Si surface by the HCl etch and only the covalently bonded InGaAs remains. The transferred layers are then subjected to device processing steps such as cleaning, patterning, etching, and wire bonding with no degradation in the transferred layers observed.

Thinning of the Si wafers was particularly important to successful bonding [131]. The initial Si wafers used had thicknesses of $400 - 550$ μm, and yields of the bonding were very low ($< 5\%$). By thinning the wafer to a thickness of 190 μm, the yields increased to over 80% while following the same bonding process. Additionally, bonding in a glove box environment helped reduce any oxide formation at the wafer-bonding interface. In previous InGaAs/Si wafer-bonding experiments, annealing in a H_2 environment was essential in reducing oxide at the interface [132]. For the process above, bonding in a glove box and maintaining a dry N_2 environment reduced formation of any oxide prior to bonding. No significant differences were observed when annealing bonded samples in N_2 compared to a H_2 environment. Finally, a thorough cleaning of the Si and InGaAs surfaces was essential for successful bonding.

5.3 Band Discontinuity Measurement

Using the bonding process described in the previous section, *p*-type heterojunctions were fabricated to investigate the hole transport properties across the InGaAs/Si interface. We used boron-doped, mirror-polished, *p*-type (100) Si wafers with a resistivity of ~ 4.5 Ω·cm (3×10^{15} cm^{-3}). The InGaAs structures were grown using

solid source molecular beam epitaxy on a semi-insulating (100) InP substrate with a highly-doped 1000 Å InGaAs contact layer ($> 10^{19}$ cm^{-3}), a 5000 Å moderately-doped InGaAs active layer (5×10^{16} cm^{-3}), and a 1000 Å InAlAs cap layer. The InAlAs cap layer is a sacrificial, protective layer that is removed prior to sample preparation using a selective HCl solution (HCl:$H_2$0 3:1). The cap layer helps protect the InGaAs surface between the time it is grown and the time is ready to use.

The valence band discontinuity of the heterojunction was characterized by measuring I-V characteristics and applying thermionic emission theory [83] to calculate the barrier height [126, 127]. Devices of different shapes and sizes were fabricated to measure the impact of surface and edge effects on the I-V measurements. Ohmic contacts (70 Å Cr/3000 Å Au) in square and circle shapes with characteristic sizes ranging from 100–250 μm were evaporated onto the transferred InGaAs. The Cr/Au contacts were used as self-aligned masks for the subsequent wet etch of the InGaAs layers that defined the size of the devices. Aluminum was evaporated on the backside of the Si to provide a substrate ohmic contact. I-V measurements were taken over a range of temperatures using a semiconductor parameter analyzer (Keithley 4200).

Carrier transport at the interface can be described by thermionic emission theory, and the total current density for a heterojunction is a function of voltage and temperature given by

$$J = A^{**}T^2 \exp\left(-\frac{q\Phi_B}{k_B T}\right)\left[\exp\left(-\frac{qV_1}{nk_B T}\right) - \exp\left(\frac{qV_2}{nk_B T}\right)\right] , \tag{5.4}$$

where n is the ideality factor, and V_1 and V_2 are the fractions of the applied voltage dropped on either side of the junction with $V_a = V_1 + V_2$ (see Fig. 5.4(a)). It is useful to redefine Eq. 5.4 as

$$J = J_{sat}\left[\exp\left(-\frac{qV_1}{nk_B T}\right) - \exp\left(\frac{qV_2}{nk_B T}\right)\right], \tag{5.5}$$

where J_{sat}, the saturation current density is

$$J_{sat} = A^{**}T^2 \exp\left(-\frac{q\Phi_B}{k_B T}\right). \tag{5.6}$$

The current density as a function of the applied voltage is shown in Fig. 5.5, where the InGaAs is biased with respect to the grounded Si substrate. The curve has three regions of interest. The first region, where series resistance effects dominate, extends from-2 V to 0.3 V. The second region is the region from -0.3 V to 0 V, where the current density is exponentially dependent on the applied voltage (second term in Eq. 5.4). The third region is the positively biased region where the dependence on the applied bias voltage is weak (first term in Eq. 5.4). In order to extract the valence band discontinuity E_V from the J-V measurement, the barrier height,Φ_B, must first be extracted.

The current density in region 2 was fit to the second term in Eq. 5.4, ignoring the first term in the limit of positive bias. By plotting the current density on a log-linear plot and extrapolating the curve to 0 V, the saturation current, J_{sat}, is extracted (see Fig. 5.6(a)). The barrier height, Φ_B, and the Richardson constant, A^{**}, can then be determined by fitting the exponential dependence of the saturation currents vs. the temperature (see Fig. 5.6(b)). The barrier height was determined to be 0.59 eV with a standard deviation of 0.04 eV as shown in Fig. 5.7. The reduced scatter in the data points at larger device area suggest that edge and surface effects could be responsible for some of the variations in the barrier height.

The valence band discontinuity, ΔE_V, can be deduced from the measurement of the barrier height using the relationship

$$\Delta E_V = qV_D - \delta_1 + \delta_2, \tag{5.7}$$

where V_D is the diffusion potential ($V_D = V_{D1} + V_{D2}$), and δ_1 and δ_2 are the distances from the valence band edge to the Fermi level for InGaAs and Si, respectively (see

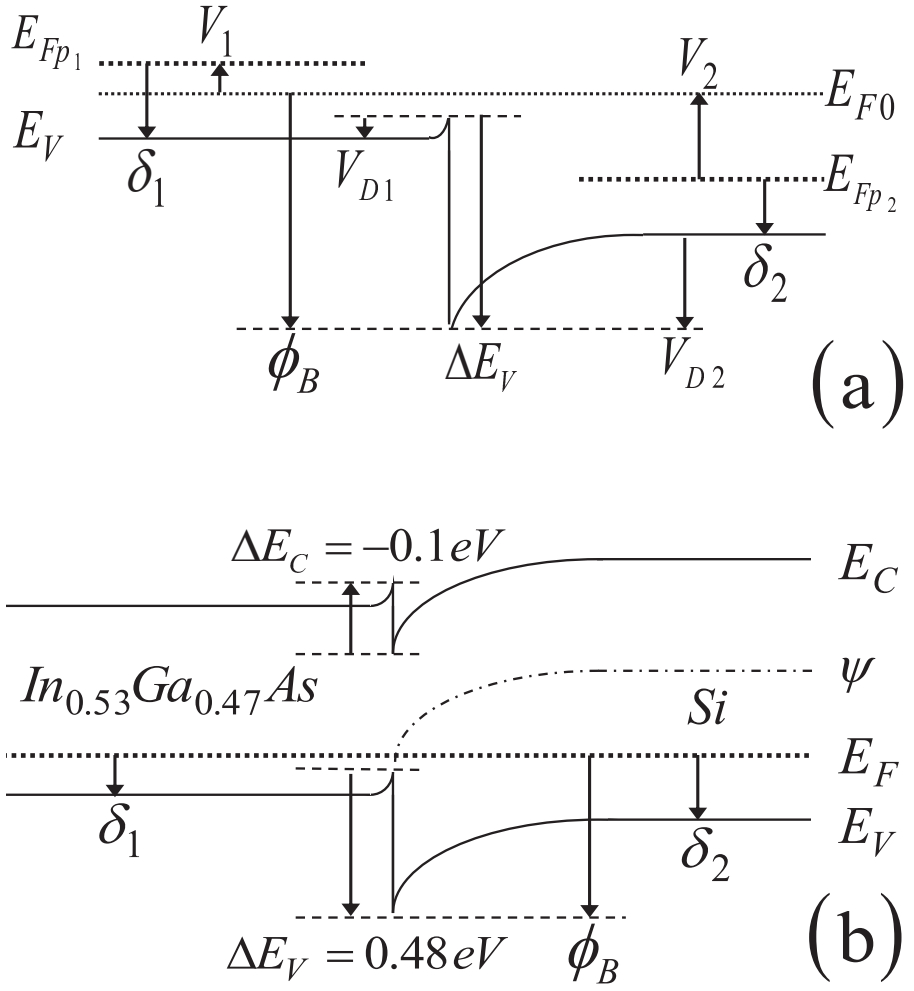

FIGURE 5.4: (a) Definitions of selected terms for the valence band. E_V is the valence band, E_{F0} is the equilibrium Fermi level, E_{FP1} and E_{FP2} are the quasi Fermi levels, δ_1 and δ_2 are the energy differences between the Fermi level and valence band, V_1 and V_2 are the fractions of the applied voltage supported in each semiconductor, V_{D1} and V_{D2} are the diffusion potentials, ΔE_V is the valence band discontinuity, and ϕ_b is the barrier height. (b) Band alignment of the p-type InGaAs/Si heterojunction. The valence band discontinuity is determined to be 0.48 eV, while the conduction band discontinuity is -0.1 eV. E_C and E_V are the conduction and valence bands, E_F is the Fermi level, and ΔE_C and ΔE_V are the conduction and valence band discontinuities. ψ is a measure of potential that is measured from the intrinsic fermi level of the bulk.

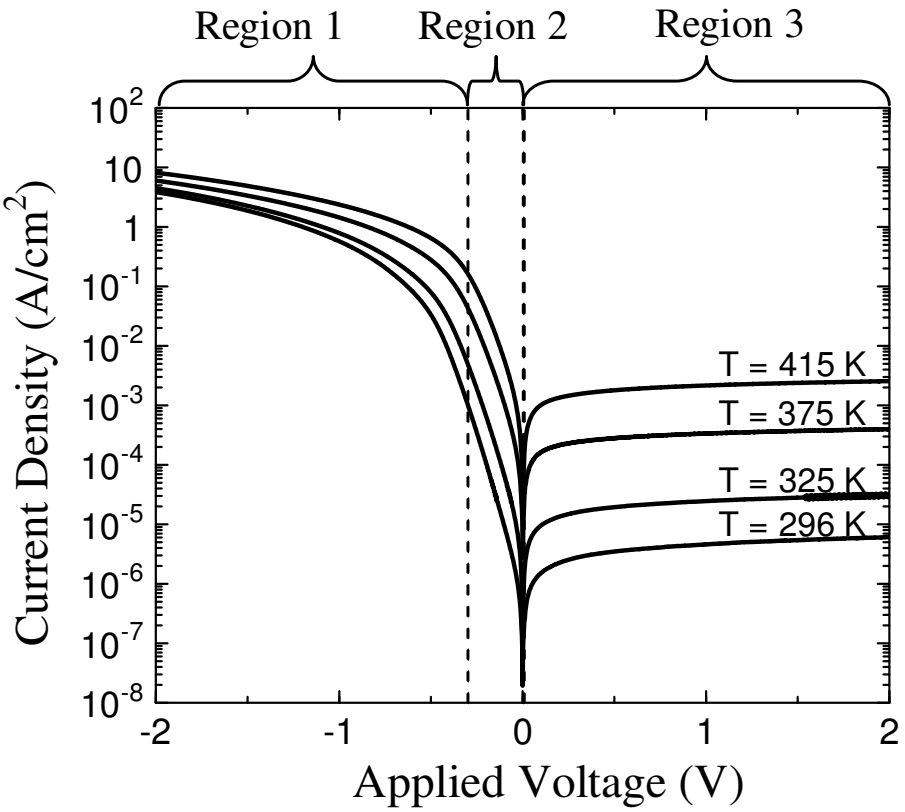

FIGURE 5.5: J-V Plot for a p type sample bonded and annealed in an N_2 environment. In region 1 (-2 V to -0.3 V), the current density is limited by series resistance effects. In region 2 (-0.3 V to 0 V), the current density has an exponential relation to the applied voltage. In region 3 (0 V to 2 V), the current density has a weak dependence on the applied voltage.

Fig. 5.4(a)) [127]. The parameters δ_1 and δ_2 are given by

$$\delta = k_B T \ln\left(\frac{N_V T^{3/2}}{N_a}\right), \tag{5.8}$$

where N_V is the materials valence band conduction band density of states.

Determination of the diffusion potential, V_D, can be accomplished due to the boundary condition imposed by the continuity of electric displacement field ($\mathcal{D}$, $\epsilon_1 E_1 = \epsilon_2 E_2$) at the interface. The barrier height of 0.59 eV and the reduced current for hole injection from InGaAs to Si suggests a band alignment similar to Fig. 5.4(b). The electric field on both sides of the interface is determined from the

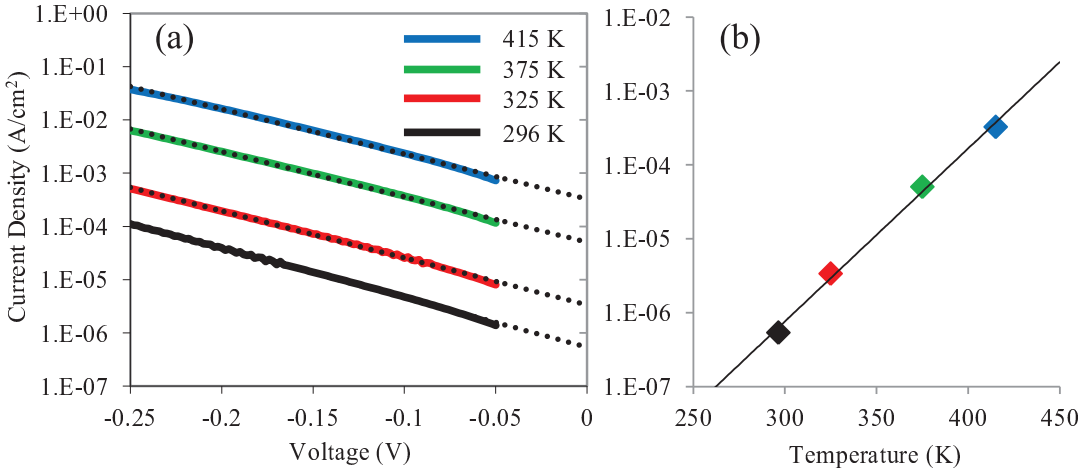

FIGURE 5.6: Plots of the (a) current density vs. voltage and the (b) saturation current vs. temperature characteristics of the fabricated p-type InGaAs/Si heterojunctions. The current density curves are extrapolated to find the saturation currents at 0 V. The saturation currents can then be plotted vs temperature to extract the barrier height from the exponential dependence.

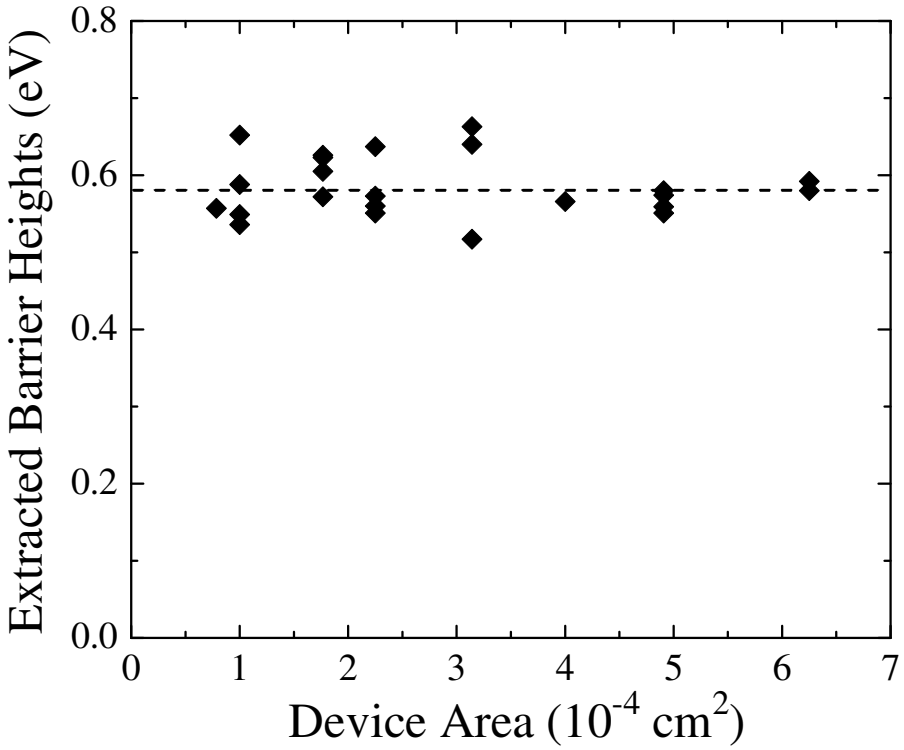

FIGURE 5.7: Extracted barrier heights for measured devices. Dashed line indicates the average barrier height of 0.59 eV.

one-dimensional Poisson equation,

$$\nabla \cdot \mathcal{D} = \epsilon \frac{\partial E}{\partial x} = \epsilon p\left(x\right) = \epsilon q\left(N_D^+ - N_A^- + p_p - n_p\right), \tag{5.9}$$

where N_D^+ and N_A^- are the ionized dopants and p_p and n_p are the majority hole and minority electrons for a p-type junction. Following the model of analysis used by Sze [83], it is useful to define a parameter for the potential, ψ, which is measured from the intrinsic Fermi level of the material in the bulk. In the bulk ψ is zero and near the interface it follows the curvature of the conduction and valence band (see Fig. 5.4(b)) and using ψ the majority and minority carrier concentrations can be redefined as

$$\begin{aligned} n_p &= n_{po} \exp\left(q\psi/k_B T\right) = n_{po} \exp\left(\beta\psi\right) \\ p_p &= n_{po} \exp\left(-q\psi/k_B T\right) = p_{po} \exp\left(-\beta\psi\right) \end{aligned} \tag{5.10}$$

where n_{po} and p_{po} are the equilibrium densities of minority electrons and majority holes, and $\beta \equiv q/k_B T$. Equation 5.9 can then be rewritten as

$$\frac{\partial E}{\partial x} = -\frac{q}{\epsilon}\left[p_{po}\left(\exp\left(-\beta\psi\right) - 1\right) - n_{po}\left(\exp\left(\beta\psi\right) - 1\right)\right]. \tag{5.11}$$

The displacement field on each side of the junction is then given by

$$\mathcal{D}_1 = \epsilon_1 E = \sqrt{2k_B T N_{a1}}\left[\exp\left(-\beta\psi_1\right) + \beta\psi_1 - 1 + \frac{n_{po1}}{p_{po1}}\left(\exp\left(\beta\psi_1\right) - \beta\psi_1 - 1\right)\right]^{1/2} \tag{5.12}$$

$$\mathcal{D}_2 = \epsilon_2 E = \sqrt{2k_B T N_{a2}}\left[\exp\left(-\beta\psi_2\right) + \beta\psi_2 - 1 + \frac{n_{po2}}{p_{po2}}\left(\exp\left(\beta\psi_2\right) - \beta\psi_2 - 1\right)\right]^{1/2}.$$

Assuming that the band alignment is similar to Fig. 5.4(b), ψ_1 is negative and ψ_2 is positive. For $\mathcal{D}_1$, the equilibrium carrier ratio, n_{po}/p_{po} is $<< 1$, so the last three terms can be ignored. Similarly, for $\mathcal{D}_2$, the first term and the last two terms can be ignored. The fourth term represents inversion and grows exponentially for large

values of ψ_2. However, at equilibrium and at negative voltages (forward current), this term is still $<< 1$ and can be ignored. Under these assumptions for forward bias conditions, equilibrating the fields results in

$$\epsilon_1 N_{a1} \left(\exp\left(-\beta\psi_1\right) + \beta\psi_1 - 1\right) = \epsilon_2 N_{a2} \left(\beta\psi_2 - 1\right). \tag{5.13}$$

Using the following helpful relationships,

$$\begin{aligned} \psi_1 &= V_{D1} - V_1 \\ \psi_2 &= -\left(V_{D2} - V_2\right) \\ \psi_2 &= \psi_1 - \left(V_D - V\right) \\ C &\equiv \frac{\epsilon_2 N_{a2}}{\epsilon_1 N_{a1}} \end{aligned} \tag{5.14}$$

Eq. 5.13 can be rewritten as

$$\exp\left(-\beta\psi_1\right) = \beta\left(C-1\right)\psi_1 - \beta C\left(V_D - V\right) - C + 1. \tag{5.15}$$

At zero bias, $V_{D2} = \delta_2 - \Phi_B$; therefore, V_{D2} is determined from the measured barrier height and evaluation of δ_2 using Eq. 5.8. Equation 5.15 can then be solved numerically at zero voltage to determine V_{D2} by replacing ψ_1 with V_{D1} (see Eq. 5.14 and using the calculated value of V_{D1}. For the p-type InGaAs/Si heterojunctions described above, the calculated value of V_D is 0.385 V. Using Eq. 5.7, the valence band discontinuity, ΔE_V is calculated to be 0.48 V. Equation 5.15 can then be used to solve for the V_1 and V_2 dependence on the total applied voltage. For low voltages ($|V| < 0.4$ V), V_1/V_2 is ~ 25. At higher voltages, the assumptions made to reduce Eq. 5.12 are no longer valid and the dependencies increase in complexity but can still be numberically solved using the calculated values.

The conduction band discontinuity, ΔE_C, is calculated using

$$\Delta E_C = E_{g2} - E_{g1} - \Delta E_V, \tag{5.16}$$

where E_{g1} and E_{g2} are the bandgaps of InGaAs and Si, respectively. Figure 5.4(b) shows the resulting type II band alignment at room temperature that results from the discontinuity values of $\Delta E_V = 0.48 \pm 0.04$ eV and $\Delta E_C = -0.1$ eV.

The Richardson constant, A^{**} for an ideal Schottky barrier is given by [83]

$$A^{**} = \left(\frac{4\pi q m^* k^2}{h^3} \right), \tag{5.17}$$

where m^* is the effective mass and h is Planck's constant. For a heterojunction structure where the semiconductors have different effective masses, the lower effective mass should be used [133]and for holes in the InGaAs/Si heterosystem the ideal Richardson constant is ~ 40 Acm^{-2}K^{-1}. Using Eq. 5.6, an average of 0.06 Acm^{-2}K^{-1} for the Richardson constant was extracted from the measured J-V data for the wafer-bonded, p-type, InGaAs/Si heterojunctions. The significant difference between the ideal value and the measured value for the Richardson constant indicates that there is a thin interfacial layer at the heterointerface that impedes carrier transport across the junction [134, 135, 136]. For thermionic emission at an interface with a thin tunnel barrier Eq. 5.6 is modified to

$$J_{sat} = \Theta A^{**} T^2 \exp\left(-\frac{q\Phi_B}{k_B T} \right), \tag{5.18}$$

which includes the transmission coefficient of the barrier, Θ. For a rectangular barrier the transmission coefficient, Θ, can be approximated using the WKB approximation to be [134]

$$\Theta = \exp\left(-2 \int_{x_1}^{x_2} |k| \, \mathrm{d}x \right), \tag{5.19}$$

where k is the component of the momentum in the direction perpendicular to the barrier and x_1 and x_2 are the positions of the interface barrier edges and the thickness of the interfacial layer, $\delta = x_1 - x_2$. The component of momentum, k, for a

rectangular barrier is given by

$$k = \sqrt{\frac{2m^*}{\hbar^2}(W - E)}, \tag{5.20}$$

where W is the potential height of the barrier and E is the energy of the carrier. An effective barrier, χ, is defined as $\chi \approx (W - E)$ assuming that the barrier is large compared to E and that there is no thermionic emission over the barrier, then Eq. 5.19 becomes [134]

$$\Theta \approx \exp\left(\sqrt{m^*\chi}\delta\right), \tag{5.21}$$

where χ is measured in eV and δ is measured in angstroms.

Figure 5.8 is a TEM image of the wafer-bonded InGaAs/Si interface. The bright patches at the interface result from a thin ($<\sim$ 1.5 nm) amorphous layer, which is most likely an oxide. Using Eq. 5.21 , the transmission probability of an interfacial layer with an average thickness of 10 Åand an effective barrier, χ, of 1 eV the transmission probability, Θ is $\sim 10^{-3}$. The valence band discontinuity between Si and SiO_2 is $\sim$ 4.4 eV [113]; however, as the interface layer only consists of several monolayers of amorphous oxide it is unlikely that the thin layer has the same properties as bulk SiO_2. In addition, the interfacial oxide layer probably consists of additional oxides with InGaAs making it difficult to determine the actual barrier.

Secondary ion mass spectrometry (SIMS) analysis was also done to the wafer-bonded InGaAs heterojunctions to measure the H, C, and O concentrations at the bonding interface. In a SIMS measurement, a high-energy ion beam ($\sim$ 1 kV) is used to sputter surface atoms. Any ions that are sputtered away from the surface are then collected, and a mass analyzer is used to measure the mass distribution of the sputtered material. A SIMS measurement result for a wafer-bonded InGaAs/Si sample is shown in Fig. 5.9. The wafer-bonded interface occurs at a depth of $\sim$ 0.9 μm, and at the interface the values of C, H, and O exhibit a sharp peak. The C and

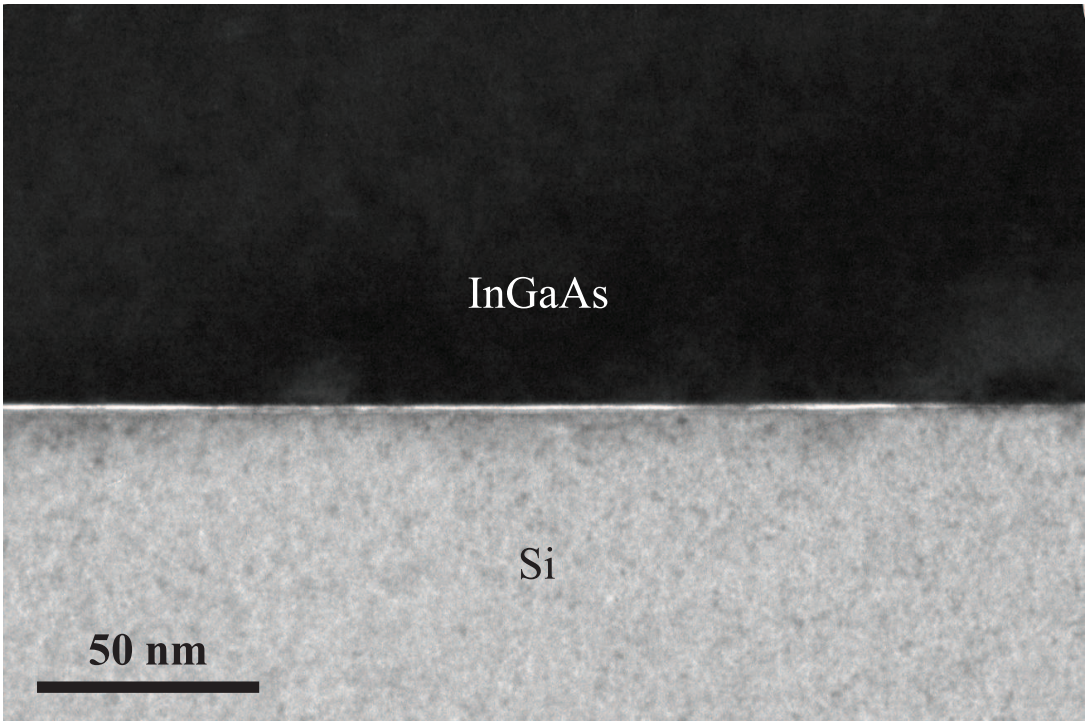

FIGURE 5.8: TEM image of the Si (bottom) and InGaAs (top) interface. A thin amorphous layer ($\sim 1-2$ nm) is visible in patches at the interface.

O curves in Fig. 5.9 are shifted to the right by 0.3 μm and 0.6 μm, respectively, to improve clarity of the peaks. The width of the peaks is due in part to uneven sputter rate over the sample area as the device is etched. The O peak reaches a maximum concentration of $\sim 8 \times 10^{20}$. For bulk SiO_2, the atomic density is $\sim 4.6 \times 10^{22}$ atoms/cm^3, and given a step size of ~ 20 nm, the maximum concentration of the O peak is consistent with a thin interface layer with an average thickness of 3 Å. This is only a rough estimate as the interface layer probably consists of several types of oxide, with a density different than the bulk approximation used [134]. The SIMS measurement provides some confirmation that the interface layer is some type of oxide.

The interfacial layer significantly reduces the transmission of carriers and reduces the effective area of the heterojunction. Annealing in a H ambient helps to

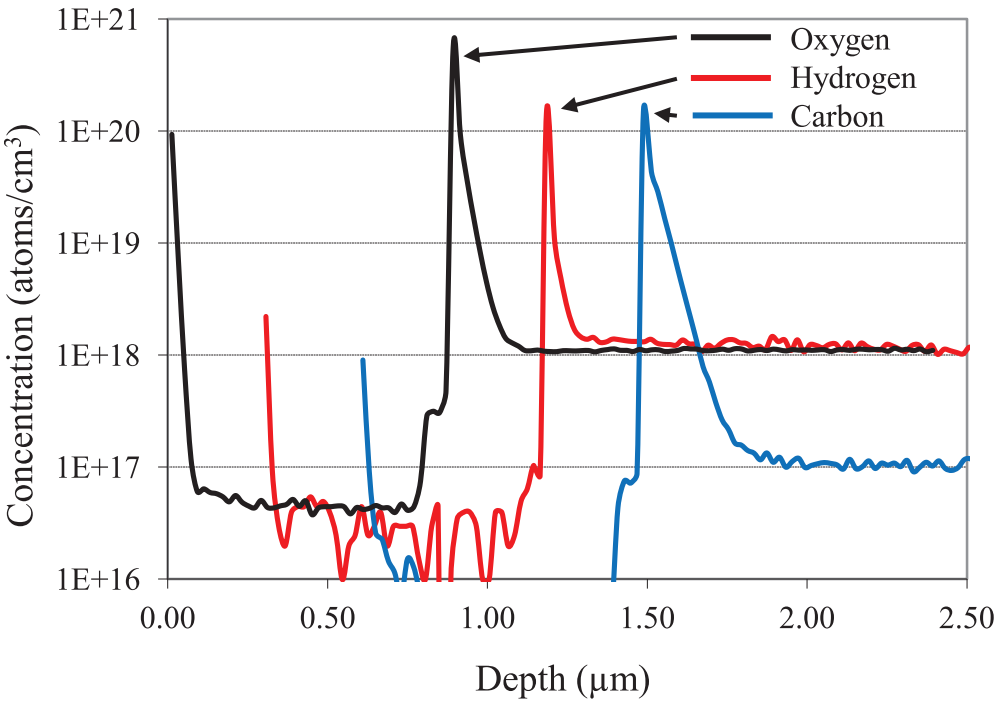

FIGURE 5.9: Secondary ion mass spectrometry (SIMS) measurement of the wafer-bonded InGaAs/Si interface. The H and C curves are shifted to the right by 0.3 and 0.6 μm, respectively to improve clarity of the peaks which occur at the bonding interface at about 0.9 μm. The high O concentration at the interface is consistent with a thin interfacial oxide layer at the bonding interface that creates a thin tunnel barrier at the interface.

reduce the formation of this oxide and InGaAs/Si heterojunctions annealed in a H environment have shown significantly improved I-V characteristics in comparison to samples annealed in non-H environments [132]. The influence of strain resulting from the thermal mismatch of InGaAs and Si is also expected to reduce the current from the ideal value [133, 137, 138].

Due to the 7.7% lattice mismatch between InGaAs and Si, a periodic array of dislocations are expected at the hetero-interface. The spacing between the edge dislocations is given by the ratio of the lattice constant and the lattice mismatch and for InGaAs/Si, the expected spacing is $\sim$ 13 lattice planes. The edge dislocations are visible in TEM images of regions of the InGaAs/Si interface where no interfacial

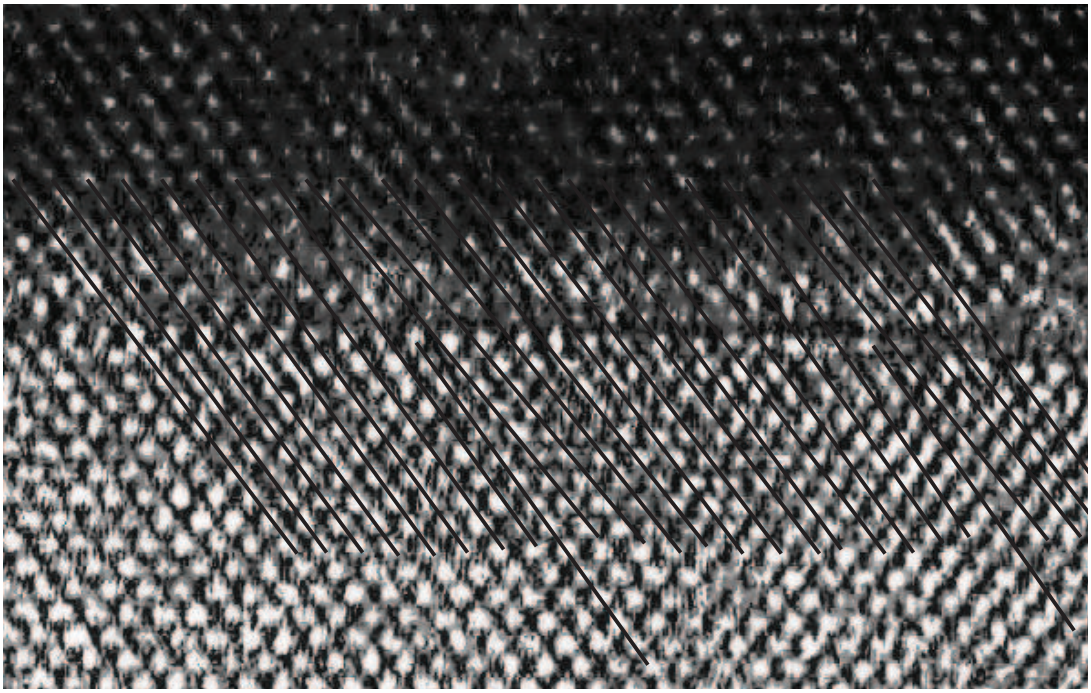

FIGURE 5.10: TEM image of the Si (bottom) and InGaAs (top) interface. The lattice mismatch of 7.7% results in edge dislocations at the interface which are spaced every $\sim$ 13 atomic planes in Si. Strain effects at the interface lead to some distortion in atom location at the interface.

layer is present (see Fig. 5.10. In the bonding process described in this chapter, it is expected that many of these dislocations are passivated by hydrogen from the HF treatment prior to bonding. Previous work has shown that a nearly ideal interface, free from significant charge trapping, can be fabricated between InGaAs and Si, even in the presence of these dislocations [57]. Any trapped charge at the interface modifies the continuity equation to include the addition of the interface charge. This can shield the applied voltage and will result in an increase in the ideality factor in Eq. 5.5 [134, 135, 136, 130]. Fitting of our data shows that the ideality factor is $\sim$ 1.5, which is greater than the ideal value of 1.

6

UHV bonding system

6.1 Introduction

The proposed infrared photon counter (IRPC) uses an InGaAs absorption layer to increase the sensitivity of the VLPC to infrared radiation, particularly at the telecom wavelengths of 1.31 and 1.55 μm (see Fig. 1.3. The photodetection response of the VLPC is generally triggered by the photogenerated hole. For the IRPC, the photon would be absorbed in the InGaAs absorption layer and the hole would need to drift across the heterointerface into the Si layers to trigger the gain process. For the photogenerated hole to transfer between InGaAs and Si with high efficiency, there should be no barrier to hole transport at the heterointerface. The band alignment of the InGaAs/Si wafer-bonded heterojunction was presented in Section 5.3 and shows that there is a large barrier to hole injection (0.48 eV) from InGaAs to Si.

The Anderson model predicts the band alignment of a heterojunction by neglecting interface effects and aligning the materials using the electron affinities of the bulk materials [115]. The predicted band alignment for the InGaAs/Si heterojunction using the Anderson model (ΔE_v = -0.07 eV) is significantly different than the observed

band alignment ($\Delta E_v = 0.48$ eV) [139]. The reason for this is that the Anderson model does not take into account any interactions at the interface. In reality, there is a transfer of charge at the interface, which generates a dipole (referred to as the interface dipole) [140, 113]. This interface dipole results in a modification of the band alignment from the model predicted by Anderson. This interface dipole is greatly influenced by the interface chemistry of the heterojunction. Modification of interface dipoles has the potential to induce large shifts in the band alignment of heterojunctions with shifts of 0.5 eV being experimentally demonstrated [112, 141, 113].

Control of interface dipoles requires precise control of the interface chemistry of the heterojunction. Control of the interface chemistry can be achieved by controlling the surface chemistry of the wafers prior to bonding, which requires bonding in a ultra-high-vacuum (UHV) environment. In a UHV environment ($< 10^{-9}$ mbar), the density of atoms and molecules is many orders of magnitude below atmospheric pressure, which significantly decreases the interaction of the surface with the environment. Reactive surfaces can be prepared and maintained in UHV environments. In this chapter the design of a UHV system that can be used to study the impact of the interface chemistry on wafer-bonded heterojunctions is described.

6.2 System Design

The UHV bonding system (see Fig. 6.1 and Fig. 6.2) consists of three main subsystems: a wafer-bonding subsystem, an X-ray photoelectron spectroscopy (XPS) subsystem, and a RF/DC sputtering subsystem. The systems are connected via a trolley subsystem for transportation of the samples from one subsystem to another while maintaining them in a UHV environment. A load lock permits samples to be loaded and unloaded quickly without compromising the vacuum integrity of the system.

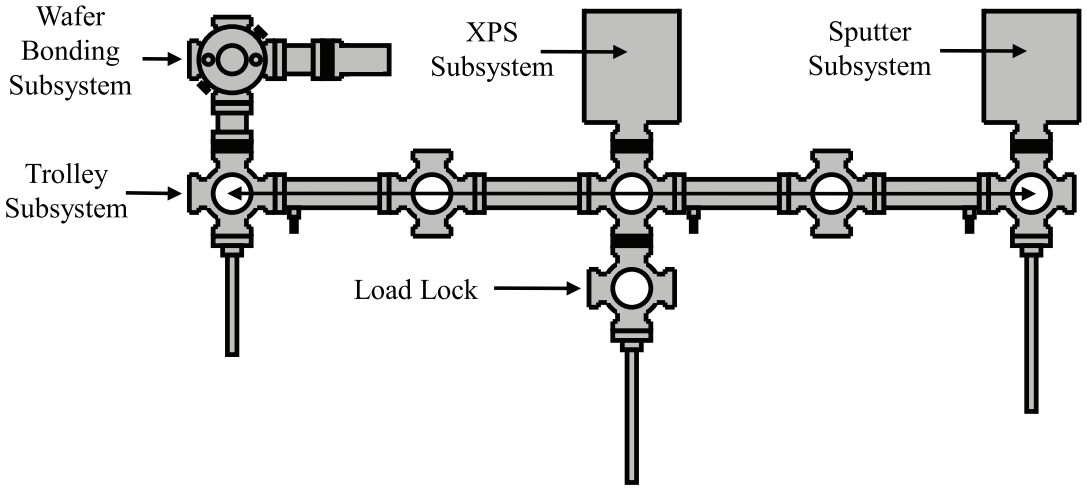

FIGURE 6.1: Schematic of the UHV system. The wafer-bonding subsystem, the XPS subsystem, and the sputtering subsystem are all connected by the trolley rail subsystem that enables sample transfer. A load lock is connected to the trolley subsystem for quick loading and unloading of samples into the system.

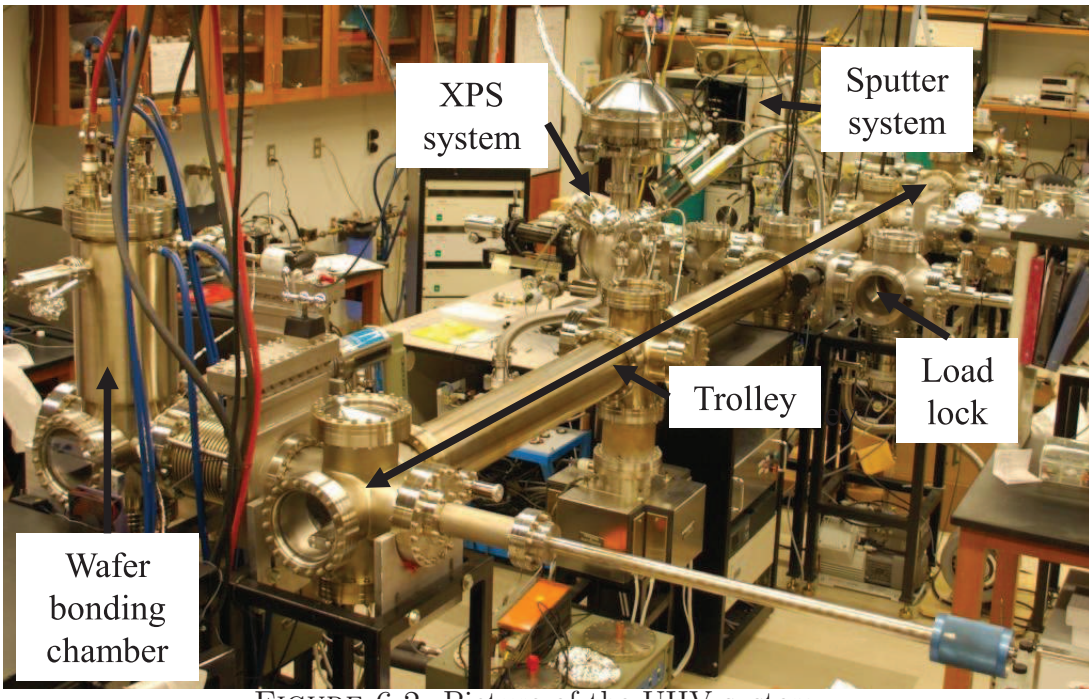

FIGURE 6.2: Picture of the UHV system.

6.2.1 Wafer-Bonding System Requirements

The wafer-bonding subsystem was custom-designed to satisfy a number of requirements necessary for serving two functions: sample annealing and wafer bonding. Annealing is necessary for certain pretreatment processes of the wafers prior to bonding [142, 143], as well as strengthening the bonds of the bonded pair. To make the system flexible for multiple material systems, the system was designed with the capability to anneal the samples at temperatures up to 1400 °C.

In addition to temperature control, other key parameters to control in the bonding process are the relative crystal orientation of the two wafers at the interface [109, 110, 111] and the mechanical pressure applied to the samples during the bonding process [101, 58]. Both of these parameters impact the quality and yield of the bonded interfaces. The subsystem includes the necessary mechanics to provide control over these parameters to successfully bond the wafer pair.

6.2.2 Heater Design

Annealing in the wafer-bonding system is accomplished through a graphite resistive heater that radiatively heats the sample. Graphite was selected due to its low cost, high melting point, and low vapor pressure at high temperatures and high vacuum. Radiative heating is an effective method for heating in high-temperature applications due to its non-contact nature, which enables uniform sample heating independent of the electrical or thermal properties of the sample material. A cylindrical, serpentine heater (see Fig. 6.3) was designed with a 3-in. inner diameter so that 2-in.-diameter sample holders fit within the heat zone. The main structure of the heater is 4 in. tall with a 3-in. inner diameter and a 3.5-in. outer diameter. Twenty-eight 3.5-in. long slits of width 0.125 in. are cut into the heater to form the serpentine shape. The number and width of the slits was chosen to match the resistance of the heater (0.16 ohms at 1400 °C) to the 10 kW 40 V power supply to achieve maximum power

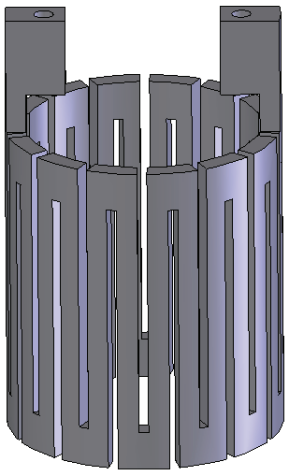

FIGURE 6.3: Model of the graphite heater used in the wafer-bonding system. The main structure of the heater is 4 in. tall with a 3 in. inner diameter and a 3.5 in. outer diameter. Twenty-eight 3.5 in. long slits of width 0.125 in. are cut into the heater to form the serpentine shape.

efficiency during high-temperature operation. The design was also constrained to ensure a structurally-sound heater element and the smallest cross-sectional area of the heater is 0.06 in^2. Two electrodes have a 1-in.-deep, $1/4 - 20$ tapped hole for electrical connection.

The heater is housed in the top half of an 8-in. inner-diameter, water-cooled, stainless-steel UHV chamber (see Fig. 6.4). The radiative heat transfer between two surfaces at different temperatures is given by

$$P = e\sigma_{sb}A\left(T_h^4 - T_c^4\right), \tag{6.1}$$

where e is the emissivity of the material surface, σ_{sb} is the Stefan-Boltzmann constant, A is the surface area, and T_h and T_c are the hot and cold surface temperatures, respectively. Equation 6.1 shows that if the heater was heated to 1400 °C inside a water-cooled chamber wall, ~ 6 kW of cooling power would be necessary to keep the walls at room temperature. To reduce both the power requirements of the heater and the cooling system, radiation shields are used (see Fig. 6.4). Molybdenum (Mo) is used for most of the furnace parts that need to operate at high temperatures

because of its high melting point, relatively good machinability, low cost (compared to other refractory metals), and high thermal conductivity. Very thin Mo foil (0.003 in.) was used to make four layers of cylindrical radiation shields of 4.0, 4.5, 5.0, and 5.5 in. in diameter. Four layers of radiation shields are also used on the top and the bottom of the heat zone. The shields are supported by two Mo plates that are each anchored to the chamber wall by four stainless-steel fixtures. The four stainless-steel fixtures at the bottom of the radiation shield assembly represent the most critical component with regard to the temperature control. The bottom Mo anchor plate supports the bottom shields as well as the radial shields, and all of the shields have a thermally conductive link to the cooled chamber wall through the stainless-steel fixtures. The conductive load on the fixtures is minimized by using the thinnest possible Mo foil. This ensures that most of the heat is dissipated through radiation over the entire chamber wall surface rather than conducted to the stainless-steel fixtures. Two K-type thermocouples (chromel–alumel) are used to monitor the temperature of one of the anchor fixtures from both the bottom shields and the top shields to ensure that the temperature of the stainless-steel fixtures does not exceed 600 °C. At temperatures above 600 °C, stainless steel begins to decompose under UHV conditions and can result in Ni contamination of wafer surfaces. The use of four layers of thin radiation shields reduces the heat load on the chamber wall and reduces the cooling requirements by an order of magnitude compared to a design with no shielding. The maximum tested temperature of $\sim$ 1400 °C was achieved at a current of 110 A (the temperature of the stainless-steel fixtures was 510 °C). The diameters of the through holes in the top and bottom radiation shields necessary for structural support and sample loading are minimized to reduce radiative losses from the heat zone.

Power is delivered to the heater via two water-cooled, copper, electrical feedthroughs. Two 0.25-in.-diameter, threaded, Mo rods suspend the heater and connect it to two

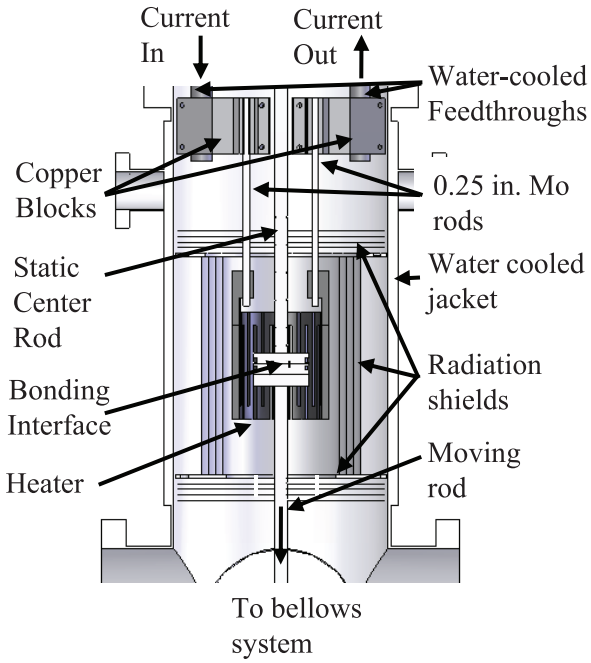

FIGURE 6.4: Internal cross section of the top portion of the wafer-bonding chamber. A graphite heater is surrounded by four layers of Mo radiation shields. The heater is supported by two Mo rods connected to a water-cooled copper feedthrough. The bonding interface is located at the center of the heat zone. Pressure can be applied by squeezing the sample between the static center rod and the moving rod connected to the bellows system.

copper blocks attached to the water-cooled feedthroughs (see Fig. 6.5).

6.2.3 Wafer-bonding Mechanics

The wafer-bonding mechanics are provided by a static center rod and a bellows system (see Fig. 6.6) for moving the sample holders vertically. For the static center rod, a 0.5-in. Mo rod is set in the center of the chamber, attached to the top flange through a flexible bellows to adjust the center position of the rod (see Fig. 6.5). This static center rod is used to apply pressure to samples in the heat zone. Additionally, two C-type thermocouples (tungsten 5% rhenium–tungsten 26% rhenium) are attached to the center rod to measure the temperature of the sample just above the center of the heat zone. The C-type thermocouples are electrically isolated from

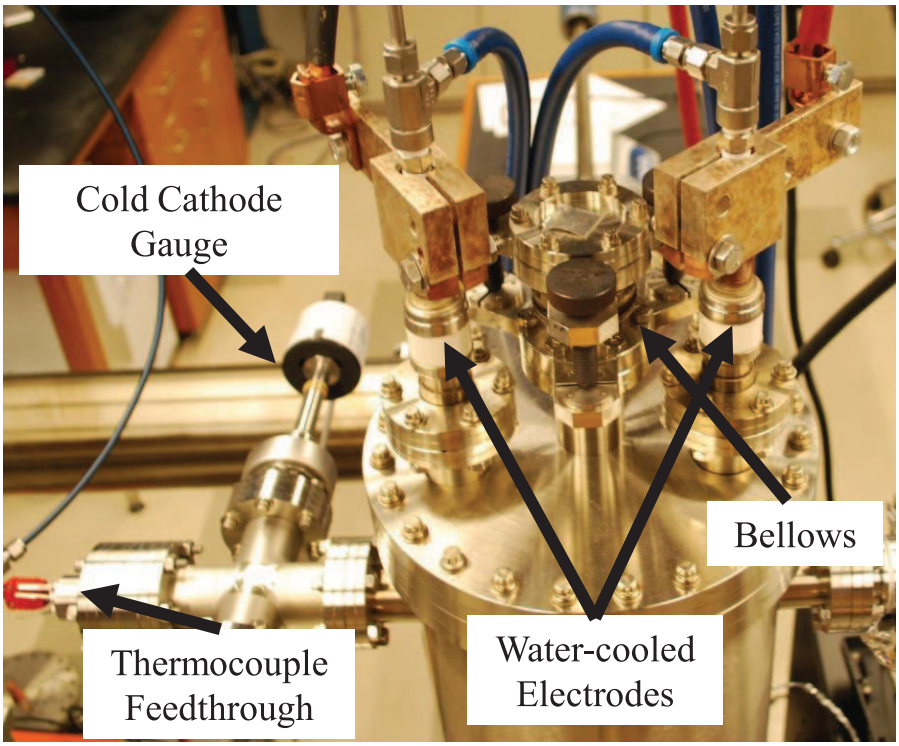

FIGURE 6.5: Picture of the top flange of the wafer bonding chamber. Two water-cooled electrical feedthroughs are used to supply power to the graphite resitive heater. The temperature of the heater is measured by two C-type thermocouples which are mounted at the end of a static center rod that drops down from the top bellows into the heat zone. The top bellows is used for adjusting the angular alignment of the static center rod to enable uniform pressure application during bonding. A cold-cathode gauge is used for measuring the pressure of the system.

system components through the use of ceramic tubing. Molybdenum wire is used to secure the ceramic tubing as well as the tip of thermocouple to the static center rod. The C-type thermocouple feedthroughs are attached to one of the side ports of the main chamber along with a cold-cathode gauge for monitoring the system pressure.

Figure 6.6 shows the schematic of the bellows system custom-designed to provide 18 in. of finely-controlled vertical travel for loading samples and applying pressure to the sample holders. While providing the necessary travel for sample loading, the bellows system must be rigid and remain vertically centered to withstand the pressure applied to the sample during the bonding process. A 22-in. bellow with an 18-in.

stroke is attached to the bottom flange and a flange connected to a moving plate. The moving plate is raised and lowered by three acme-threaded rods ($1/2-10$). The rods are connected to each other by a gear-and-sprocket set and rotated by a crank. The height can be controlled to within 0.012 in. (or 0.32 mm) by turning the handle in steps of 1/8 turns. To ensure vertical alignment during the travel of the bellows, three linear-bearing rods are used to maintain strict control of the position and angle of the moving plate.

A 28-in.-long, 0.5-in.-diameter Mo rod is attached to a flange mounted against the moving plate at the base of the bellows. The four radiation shields are attached to the rod to match up with the base radiation shields when fully raised to prevent thermal radiation leakage into the unheated portion of the chamber. A 2-in. platform is mounted atop the rod to hold the sample holders (see Fig. 6.6). Four beveled alignment pins (0.1875-in. diameter) fixed to the platform are used to fix the alignment of the sample holders.

Pressure can be applied to the samples through several different methods. The simplest way is to position the sample holders at a height that will allow thermal expansion of the rods during annealing to apply pressure between the sample holders and the static center rod in the chamber. Pressure can also be applied at room temperature by either rotating the bellows crank past the point at which the sample holders contact the vertical rod or by applying pressure through external means such as a hydraulic jack. In order to accommodate a means to apply external pressure, access to the bottom of the bellows was provided via 2.75-in.-diameter clearance holes in all of the bellows support plates.

Mo pucks (2-in. in diameter and 0.4-in. thick) are used for holding the InGaAs and Si samples (see Fig. 6.7). The base design includes four 0.204-in. diameter holes to match the alignment pins in the sample holder platform and a continuous slot around the outer edge for lifting the puck with a transfer fork. A notch is

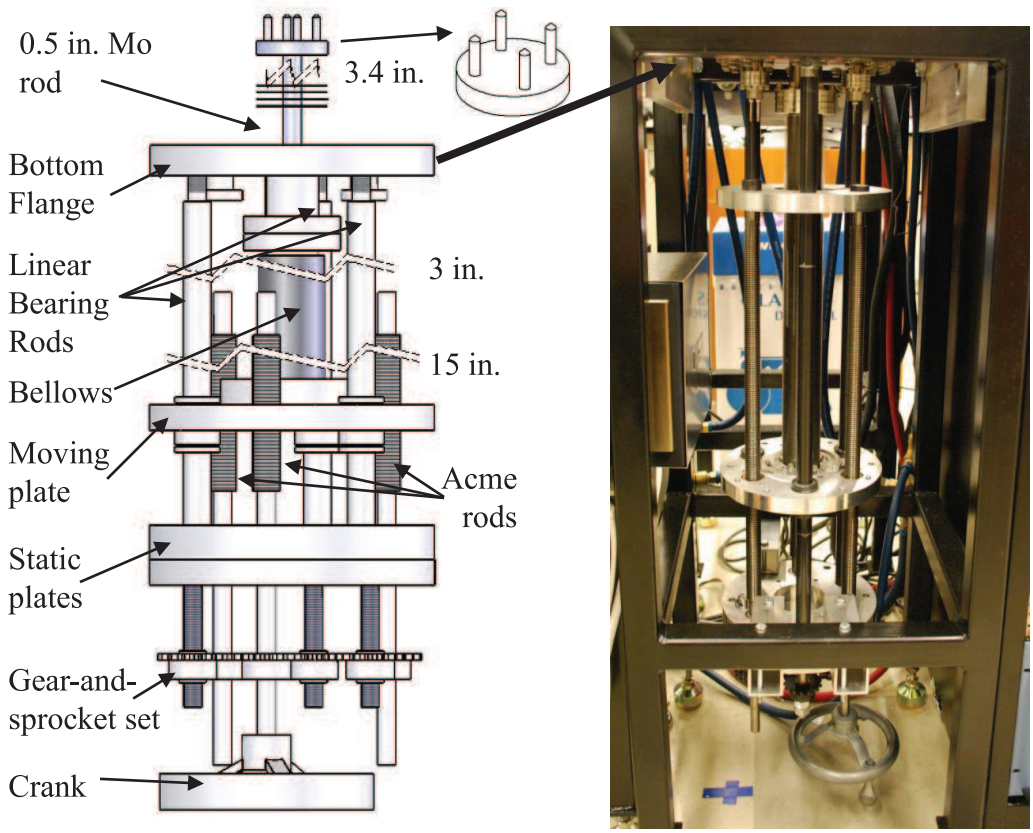

FIGURE 6.6: Schematic drawing and picture of the bellows system. The bellows system is mounted to the bottom flange of the wafer-bonding chamber. Three acme-threaded rods (1/2-10) are controlled by a chain and a gear-and-sprocket set, which, with the aid of a crank, rotates the acme rods to raise and lower the bellows (22 in. long with 18 in. stroke). The base of the bellows is attached to an Al moving plate. Linear-bearing rods are used to maintain vertical alignment of the bellows and the attached 0.5 in. diameter vertical Mo rod. The Mo rod has a sample holder platform (shown in top center of figure) at the end along with four radiation shields that match with the radiation shields of the heater system. Breaks (labeled with distance) added for clarity.

used to match with the transfer fork and prevent radial-rotation of the sample pucks during sample transfers. This base design was modified to fit the requirements for each sample used in the bonding process. For the InGaAs/Si bonding system, a 12.5 $\times$ 10 mm Si sample is bonded to an 8 mm square InGaAs/InP sample. The top surface of the puck used for attaching Si substrates (termed the Si puck) is polished to ensure uniform pressure application and reduce cracking of the samples

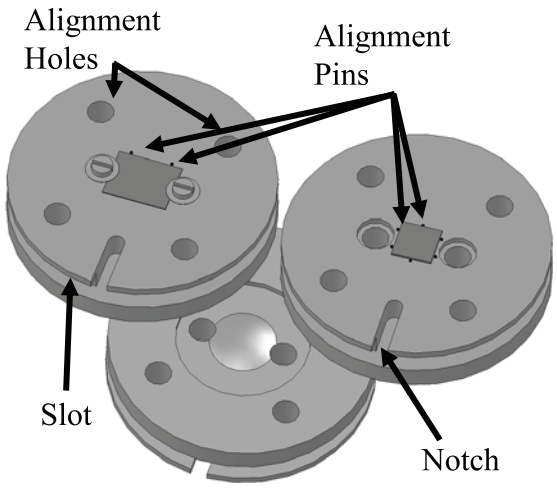

FIGURE 6.7: Models of the Mo pucks used for bonding InGaAs and Si samples. The left puck uses two screws to hold a 12.5 mm x 10 mm Si sample. The Si puck is flipped upside-down during the bonding process. Two removable alignment pins are used to align the crystal axes of the Si. The right puck holds an 8 mm square InGaAs sample. Six alignment pins are used to align the crystal planes. The pucks have four holes for alignment, a slot for a transfer fork, and a notch that matches the transfer fork to prevent rotation of the puck during sample transfer. The top surfaces of the holders are polished where the samples sit to prevent cracking of the samples due to surface roughness. The bottom puck is a model of the bottom of the Si puck. A dome feature is used to ensure uniaxial pressure between the pair of pucks, sitting on the sample platform, and the static center rod during the bonding process.

when applying pressure. The Si sample is thinned to $\sim$ 190 μm, which makes it particularly susceptible to cracking if uneven pressure is applied. A dome feature is machined on the back of the Si puck to ensure that a uniaxial pressure is applied by the static center rod during the bonding process. Two removable alignment pins (0.02-in. in diameter) are used to align the crystal axis to the holder. Two Mo screws are used with thin Mo washers to hold the Si sample in place. The Si puck is flipped upside-down during the bonding process; the screws are necessary to secure the sample during this process. For the puck used to hold the InGaAs (InGaAs puck), the top surface is also polished. Six alignment pins are used to control the crystal alignment and prevent the sample from moving or sliding during transfer. Clearance holes for the screws on the matching Si puck were machined into the InGaAs puck.

The wafer-bonding chamber is pumped by an ion pump and a cryopump. The cryopump is typically isolated except when running high-temperature anneals. A water-cooled, in-line shroud protects the cryopump from any thermal radiation that could raise the temperature of the cryo shields. The system was baked by external heater tapes at 200 °C, and the internal graphite heater (> 800 °C), which enabled the system to achieve a base pressure in the 10^{-11} mbar range. During moderate heating (< 800 °C), the pressure stays in the 10^{-9} mbar range. At the highest tested temperature of 1400 °C, the pressure rises to $\sim 1^{-6}$ mbar.

6.2.4 Surface Preparation and Analysis Capabilities

The XPS subsystem was built from components manufactured by Thermo Scientific and has a hemispherical analyzer and a dual-ion source (Mg and Al). The XPS was calibrated with a gold film to have a full-width-at-half-maximum (FWHM) of 1.3 eV for the $4f_{7/2}$ peak. The XPS subsystem is pumped with an ion pump and a Ti sublimation pump with a base pressure in the 10^{-10} mbar range.

The sputtering subsystem is made by Denton Vacuum and has two sputter guns that can be operated in either RF or DC sputter modes. The RF supply can be switched to provide RF sample biasing to the sample stage for plasma activation and cleaning. A halogen lamp is used to provide sample heating (< 250 °C). The system is pumped by a turbo pump, which results in a base pressure in the 10^{-7} mbar range. It also has a liquid-nitrogen pumping station, which can lower the base pressure if needed.

6.2.5 Trolley System

A 20-ft-long trolley subsystem from Kurt J Lesker Co. is used for transferring samples from one subsystem to the other. Figure 6.8 shows a picture of the trolley along with a 3.5-in.-diameter, stainless-steel, transfer puck; an InGaAs puck; and a fork used for

transferring the InGaAs puck into the wafer-bonding chamber. The fork is controlled by a rotary/linear-motion drive that is used to manipulate the InGaAs and Si pucks for sample transfer as well as wafer bonding. The trolley is controlled by three rotary feedthroughs connected with a stainless-steel, braided wire. The trolley system is housed in a 6-in.-inner-diameter tube pumped by two large ion pumps and a base pressure of $\sim 10^{-8}$ mbar. A two-stage parking station (see Fig. 6.9) is located in the trolley system between the load lock and the XPS system for storing sample holders during surface-preparation and wafer-bonding processes. The parking station was designed and fabricated to hold the stainless-steel pucks with Mo sample pucks within a 4.5-in.-inner-diameter, 5-way cross. The stainless-steel sample holders are compatible with the XPS, sputter, and load lock systems. The Mo sample holders are transferred along with a stainless-steel holder for use in these systems.

6.3 Initial Bonding Results

The wafer-bonding capabilities were tested by employing our standard InGaAs/Si bonding preparation process (described in Sec. 5.2). The samples were mounted onto their respective pucks, and loaded one at a time into the load lock to reach a pressure of $< 10^{-4}$ mbar within 10 min of the HF dip. The samples were transferred into the wafer-bonding chamber (InGaAs first and Si second) and brought into contact. Minimal pressure was applied to the pair by raising the sample into the heat zone and bringing the pucks into contact with the top rod. The sample puck height was then lowered by ~ 0.04 in. During the anneal, thermal expansion of the Mo rods will lead to a large applied pressure between the two pucks. The distance of 0.04 in. was carefully controlled to ensure that the applied pressure was large enough to ensure a high quality bond but small enough to prevent fracture of the Si or InGaAs sample during the bonding process. Any cracking or fracture in either sample generally results in a failed bond. The power supply for the heater was set to 300 W, which

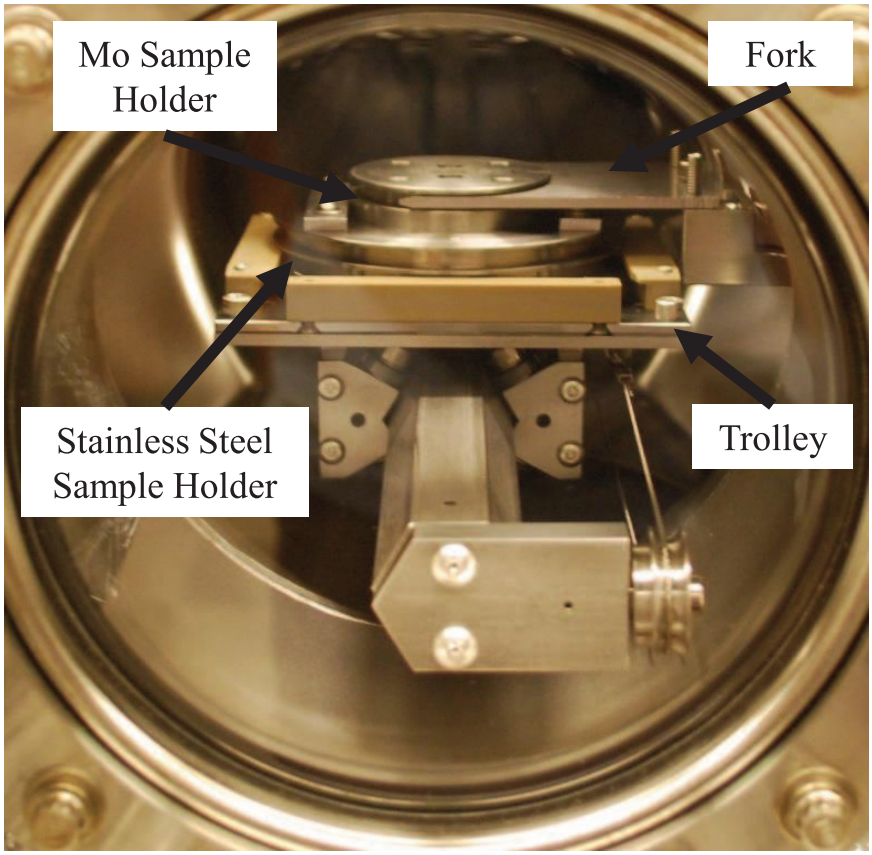

FIGURE 6.8: Picture of the UHV trolley subsystem. The trolley is controlled by three rotary motion feedthroughs (not shown) and a braided, stainless-steel-wire rope. The Mo sample holders used in the wafer bonding chamber are supported by a 3.5-in.-diameter, stainless-steel, sample holder which sits on the trolley. A fork, which matches the design of the Mo sample holders, is attached to linear rotary motion feedthrough and is used to manipulate the Mo sample holders in the trolley and wafer bonding subsystems.

leads to a ramp rate of 5 °C/min and a final temperature of 550 °C. The pair was annealed for two hours. Then, the heater was turned off to ramp the temperature down.

The bonded sample pair was unloaded from the chamber and the InP substrate was etched away using a 3:1 HCl:H_2O solution. Yields for the process are typically $\sim$ 80%, as measured by the number of patterned 300 μm InGaAs squares transferred. A result with 83% yield is shown in Fig 6.10. I-V measurements of wafer-bonded

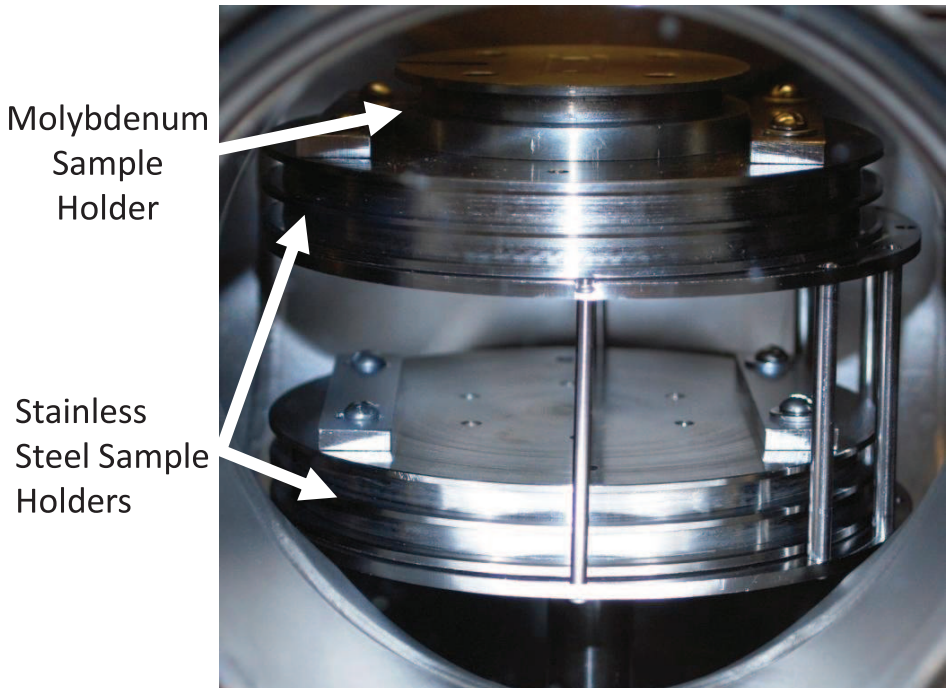

FIGURE 6.9: Picture of the UHV parking station. The parking station has two stages which can each hold a stainless-steel sample holder with a Mo sample holder on top.

devices exhibit behavior consistent with the samples bonded at atmosphere (see Sec 5.3). As the interface chemistry of the initial UHV bonded InGaAs/Si heterojunction is nominally the same as the samples bonded in the glove box environment, the band alignment of the heterojunction should be the same as reported in Sec 5.3. The main differences between the two processes were the time between the HF dip and the bonding, and the annealing profile. For the UHV bonded samples, the InGaAs and Si sample were dipped in an HF solution to remove the oxide and then had to be mounted, transferred to the UHV system, and loaded into the UHV system. During this time the samples were exposed to room air and could potentially have begun growth of an oxide. The HF process is known to passivate Si surfaces very well with the H-passivated surface stable for many hrs [144]. Similarly, the InGaAs surface is passivated by the HF dip, though this surface is not as stable for as long as Si

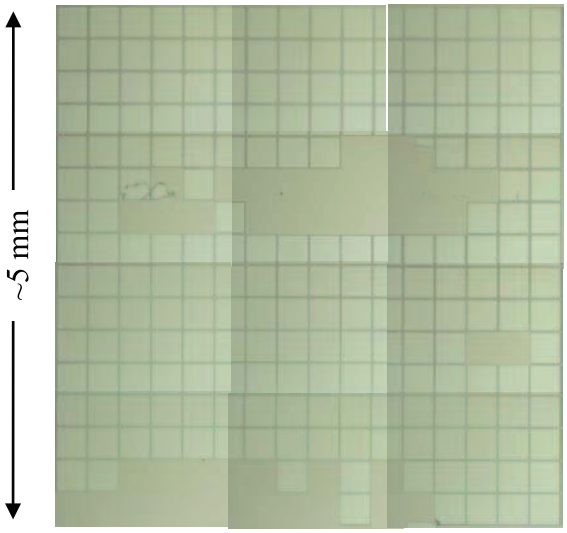

FIGURE 6.10: Picture of InGaAs squares wafer bonded to Si. 300 μm squares of InGaAs have been transferred to Si with no bubbles. Typical yields for the InGaAs/Si bonding process for our UHV system are $\sim$ 80% (as measured by the percentage of squares transferred) when bonded using our standard process.

surfaces [145].

The UHV bonding process used a single stage anneal at 550 °C in contrast to the two stage anneal at 300 °C and 650 °C for the non-UHV process. The primary purpose of the low-temperature annealing step was for outgassing of the sample surfaces. This was not necessary for the UHV process as the samples were outgassed efficiently by the UHV environment prior to bonding, and the resulting bond typically showed no or very little evidence of voids or bubbles (see Fig. 6.10). Additionally, the sample was annealed at a lower temperature of 550 °C. The melting point of the InP substrate is reduced at lower pressures, and higher temperature processing of the bonded pair resulted in decomposition of the InP substrate. No negative effects were observed due to the lower annealing temperature.

Prior to bonding, the Si and InGaAs samples are dipped in HF to remove any surface oxides, and the resulting surfaces are passivated mostly by H with some F. Hydrogen has a higher electronegativity compared to Si, so a dipole should form

between the Si and H with electrons being transferred to H. This dipole affects the band alignment of the InGaAs/Si interface. In Perfetti et al., the impact of H at the Si/SiO_2 interface was a shift in the band alignment of 0.5 eV compared to a H-free interface. By adding Cs, which has a very low electronegativity, to the interface, electrons were transferred from Cs to Si resulting in a dipole with opposite polarity that shifted the band alignment in the opposite direction by 0.25 eV [113]. To test the impact of interfacial H on the band alignment of the InGaAs/Si heterojunction, wafer bonding InGaAs and Si without H at the interface was attempted.

A H-passivated Si surface was produced by an HF dip and the sample was loaded into the UHV system. In situ XPS analysis of the sample shows a clean Si surface that is free from significant C and O contamination (see Fig. 6.11). The Si sample was then heated to 600 °C (the Si-H desorption temperature is 520 °C) for four hours to desorb the H from the surface [142]. Subsequent XPS measurements showed no increase in C or O contamination of the surface (H is not measurable with XPS). Atomic force microscopy (AFM) showed no increase in the surface roughness of annealed samples (measured RMS roughness $\sim$ 1 Å). The samples then went through our UHV bonding process, but no InGaAs was transferred to the Si. This process was repeated many times (with different samples) always resulting in unsuccessful bonding of InGaAs to Si.

A second test was to prepare an O-passivated Si surface through the growth of an RCA oxide layer ($HCl:H_2O_2:H_2O$, 1:1:5 for 1 min at 70 °C, see Fig. 6.11). The oxide was then desorbed by annealing the sample at 800 °C within the wafer bonding system [143]. XPS showed that the oxide was removed resulting in a clean Si surface free from significant C and O contamination. The sample was then used in the bonding process but InGaAs was not bonded to the Si over multiple bonding attempts.

When the Si surface was treated in UHV to prepare an O- and H-free surface

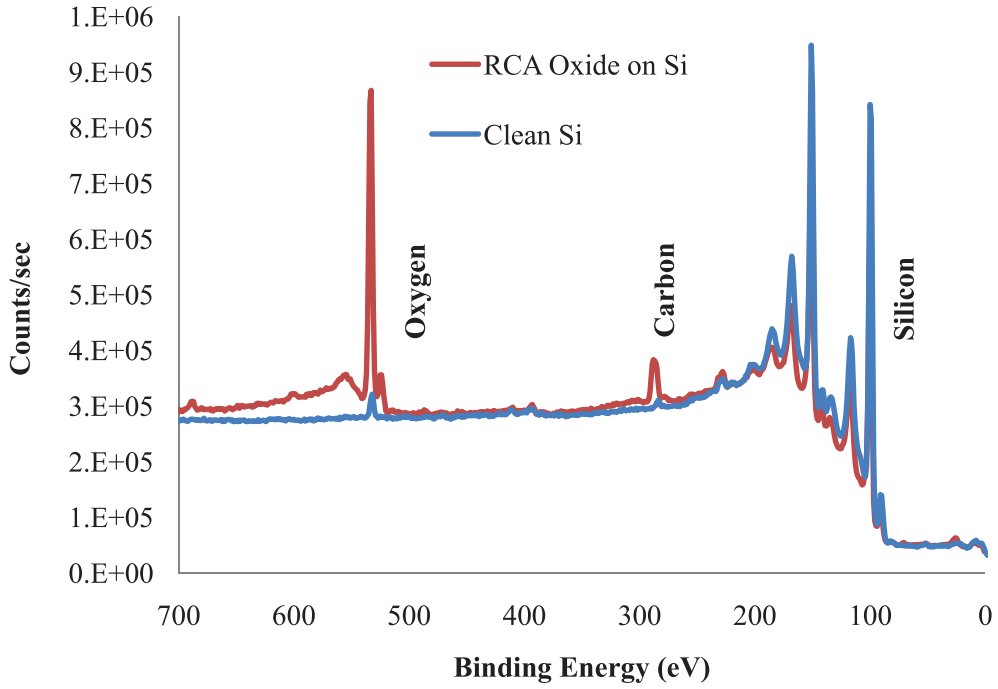

FIGURE 6.11: XPS measurements of a clean Si surface (black curve) and a RCA oxide passivated Si surface (gray curve). The clean Si data is a Si surface which is passivated by H as a result of an HF dip (ex situ) and shows no significant C or O contamination (H is not measurable with XPS). A Si sample was also prepared with an RCA oxide (to eliminate the H passivation layer from the interface). After annealing the RCA oxide coated Si surface at 750 °C for 30 min to desorb the O from the surface, XPS measurements show a clean Si surface free from significant C or O contamination.

(first by H desorption and second by O desorption), InGaAs no longer bonded to Si, indicating the importance of H to the wafer bonding process. Previous research has demonstrated that O-free wafers passivated by H can be bonded in UHV environment at low temperatures and mechanical pressures, while similar surfaces without H passivation do not bond [107, 59].

For the initial bond at room temperature, Van der Waals bonds form between InGaAs and Si. Van der Waals bonds are weak compared to covalent bonds and a

high temperature anneal is necessary to form strong covalent bonds between InGaAs and Si. The range of covalent bonds is on the order of an angstrom; thus, the surfaces must be flat and smooth to bring atoms from opposing surfaces close enough to each other to form covalent bonds over a large area. During the high temperature anneal, surface atoms can mobilize to help fill any gaps due to the flatness and roughness variations of the surface so that atoms are close enough to form covalent bonds, but this process only occurs when the surfaces are already weakly bonded [93]. A simple relation for the bondability of a wafer is given by [146]

$$\text{Bondability} \propto \frac{wL}{Eh^2}, \tag{6.2}$$

where w is the bond energy, E is a measure of the material stiffness, L and h are length and height parameters of the roughness or flatness of a wafer. For a set of wafer surfaces with a given L and h parameter that characterizes the flatness or roughness of the surface, it is evident from Eq. 6.2 that larger bond energy and a deformable material increases the bondability of the wafers. The deformability of a wafer can be increased by decreasing the thickness of one or both of the wafers. The bond energy is determined by the chemical nature of the surface and the bond. The Van der Waals bond energy of two non-polar surfaces is less than that of one non-polar and one polar surface or two polar surfaces, so the bond energy for surfaces passivated by strongly electronegative species, such as H, O, or F, will have stronger bond energies in comparison to non-passivated surfaces. For UHV bonding of InGaAs and Si, removing H from the interface decreases the bond energy and increases the requirements for the smoothness and flatness of the wafers.

An AFM is used to measure the surface roughness of a wafer, and the measured RMS roughness of the Si wafers used for the UHV bonding process was ~ 1 Å. The RMS roughness of the InGaAs wafers was ~ 2 Å, which is a factor of two rougher than the Si, but is still relatively smooth. However, the kurtosis of the InGaAs

surface is very high ($\sim$ 1000 nm) compared to Si ($\sim$ 3 nm), indicating that the increased RMS roughness of the InGaAs is primarily a result of a smaller number of taller features rather than the even distribution of shorter features that characterizes the Si surface. Increasing the bondability of the InGaAs surface requires smoother InGaAs surfaces or other passivation layers that can increase the bonding energy of the InGaAs/Si interface bonds.

7

Future Research Directions

7.1 VLPC Modeling

The visible light photon counter's (VLPC) combination of high quantum efficiency (QE, $\sim$ 88%)), low timing jitter ($\sim$ 240 ps), and photon number resolution (PNR) offers a combination of performance that is unmatched by other single photon detectors (SPDs) [11, 25]. However, the use of the VLPC in quantum information science (QIS) applications has been limited by several factors. A cryostat system is necessary to reach the low operating temperature ($\sim$ 7 K) of the VLPC. Historically, reaching low temperatures has required the use of liquid helium cryostats, which can be expensive to operate. However, a number of closed-cycle, cryogen-free, cryostats are now commercially available which make low-temperature operation more accessible for researchers [147]. Additionally, the fastest and highest-QE SPDs are realized through the use of superconducting materials that also require low temperature-cryostat operation.

Other factors that limit the use of VLPCs in QIS applications are their relatively high dark counts($\sim$ 20 kHz at the highest QE) and the limited maximum count

rates ($\sim$ 1 MHz). The dark counts of the VLPC are caused by field-assisted, thermal ionization of impurity band electrons (see Sec 2.2.4). The dark counts of the VLPC are closely related to the QE of the VLPC (see Fig. 2.5) and can be reduced by almost two orders of magnitude by reducing the QE by a factor of two. The dark counts of the VLPC can be reduced by decreasing the size of the detector. The VLPC has a large active area ($\sim$ 0.8 mm^2) and the dark count rate is proportional to the area of the VLPC. By reducing the area of the VLPC, the dark count rate can be significantly reduced; however, saturation effects are important to consider as the detector size is reduced. The detection process of the VLPC results in a small, local dead zone ($\sim 10^{-5}$ mm^2, see Sec. 2.2.2) of the detector that can take a few ms to recover [79]. As the incident photon flux increases, the probability of an incident photon being absorbed within a dead zone increases, which decreases the QE of the VLPC. Optimization of the incident photon flux spot size to reduce the saturation effects of the VLPC is critical for maintaining high QE operation at high count rates [38]. For applications in which the arrival times of photons is well known (for example, by using pulsed lasers), the effective dark count rate of the VLPC can be significantly reduced through gating operation. The low timing jitter of the VLPC allows for short gating-time windows, which decreases the probability of a dark count during the time window.

Development of a model for the VLPC is necessary for future optimization of the operating and performance characteristics of the VLPC. The device physics that explain the operation of the VLPC are detailed in Sec. 2.2.4. However, a VLPC model based on this theory fails to adequately predict the observed performance, indicating that the understanding of the VLPC is incomplete. Much of the model was derived from blocked-impurity-band (BIB) detectors, which are similar in many ways to the VLPC and precursors to the original solid state photomultiplier (SSPM) and VLPC devices [148, 85, 78, 149]. BIB detectors are long wavelength infrared radia-

tion (LWIR) detectors (not single-photon counting) that have an intrinsic blocking layer and a moderately-doped gain layer, similar to the VLPC and SSPM. They are cooled to low temperature, where an impurity band forms, and incident LWIR is detected through direct photo-ionization of the impurity band. The dark current in the device is greatly suppressed due to the intrinsic layer blocking the conduction of D+ charges through the device. Unlike the VLPC and SSPM, BIB detectors typically operate at low bias levels to minimize any impact ionization or gain. For a BIB detector, impact ionization or gain results in increased noise in the detection process [85]. As part of the BIB development, a number of models have been developed to charachterize the impact-ionization process, conductivity, and carrier-generation rates of BIB detectors. Due to the similarity of the BIB detectors to the VLPC and SSPM, parts of these BIB detector models have been used to explain the operation of the VLPC. Many of the VLPC's important operation parameters, such as the layer conductivities and impact-ionization coefficients, have been extrapolated from low-field BIB-detector data. Very limited data for VLPCs is available to understand these parameters at the higher fields of the VLPCs. A study of how different doping levels of the VLPC and SSPM layers affect the operating and gain characteristics of the device is currently underway at Duke University as part of a multi-team collaborative effort. A larger set of VLPC and SSPM data will help to create a better fit of VLPC modeling parameters and better understand the underlying device physics so that a better model can be developed.

Some of the opportunities for VLPC optimization with a better model include improvements in the timing jitter, increased maximum count rates, or reduced dark counts [150]. The timing jitter of the VLPC is dominated by uncertainty in location of secondary-electron generation (the electron that triggers the avalanche; see Sec. 3.2). As the photogenerated hole drifts through the gain and drift regions, the probability for impact ionization depends strongly on the electric field strength and the donor

density. The drift velocity of the electron in the drift region is low, so the deeper this electron is generated, the larger the transit time and resulting timing jitter. By increasing the electric field strength in the drift region or increasing the donor density, the impact-ionization probability can be increased, which would reduce the spread in the secondary-electron-generation location. Increasing the field in the drift region or increasing the donor densities will have a significant impact on other operating characteristics of the device such as the dark counts and the gain. A model of the VLPC is necessary for understanding these tradeoffs to ensure optimal design of future iterations of VLPC devices.

The maximum count rate of the VLPC is limited by saturation effects resulting from local dead-zone generation. The time scale over which these dead zones recover is determined by the conductivity of the D+ charge carriers. Until the impurity band is able to recover by sweeping out the D+ charges, the area will remain insensitive to absorbed photons. The conductivity of the D+ charges is dependent on the donor and acceptor densities in the gain and spacer layer [78]. The recovery time can be reduced by increasing the conductivity of these layers by adjusting the doping and compensation levels or by reducing the thickness of the gain and spacer layers. A VLPC model is necessary in understanding the tradeoffs in QE and dark counts associated with these changes. The inclusion of additional structural layers or graded donor density layers could balance some of these conditions and lead to new VLPC devices with improved performance.

The high QE and low-noise multiplication of the VLPC contribute to the VLPC's abilty to determine the photon number of an incident photon state [74, 39]. Photon number resolution is important to a number of applications in QIS such as linear optical quantum computation (LOQC) [22] and quantum metrology [151, 30, 152]. In the absence of circuit noise and saturation effects of the detector, an intrinsic limit on the number of photons a SPD can resolve is given by $1/(F-1)$, where F is the

excess noise factor of the multiplication process in the SPD [153]. For the VLPC, the excess noise factor is ~ 1.025 (see Fig. 2.1), resulting in an intrinsic limit of ~ 40 photons. The QE of detecting N photons scales exponentially with the QE, so high QE is necessary for large photon number states. In quantum metrology applications such as quantum lithography [154] and quantum imaging [152], special photon states referred to as NOON states can be used to increase the resolution of measurements [151]. A NOON state is a photon state which can be mathematically described by

$$|\text{NOON}\rangle = \frac{1}{\sqrt{2}}\left(|N,0\rangle_{a,b} + |0,N\rangle_{a,b}\right), \tag{7.1}$$

where N represents the photon number state and A and B represent two different spatial modes. Imaging with NOON states can result in an increase the accuracy or resolution of a measurement by a factor of N. Post-selection process are typically used for generating NOON states as the efficiency for generating NOON states is very low [151]. A SPD, such as the VLPC, with low timing jitter, photon number resolution, and high QE is important for increasing the efficiency of NOON state generation and imaging processes.

7.2 Ultraviolet Photon Counter

The QE of the UVPC is $5 - 20\%$ in the near UV wavelength range ($300 - 400$ nm, see Sec. 4.4), which is still far below the intrinsic QE of the VLPC ($\sim 95\%$). The QE of the VLPC in the UV is limited by absorption of UV photons within the top contact. For the UVPC described in Ch. 4, the degenerate contact of the VLPC was thinned and a thin (10 nm) Ti Schottky contact with a single-layer, anti-reflection (AR) coating was added to increase the conductivity of the contact and to reduce absorption within the contact. While the top contact of the UVPC was significantly thinner (~ 100 nm total thickness) than the VLPC top contact (~ 250

nm), absorption within the contact layer of the UVPC significantly limits the QE of the UVPC. Alternative strategies for reducing the contact layer thickness include laser-annealed contacts and epitaxial contacts.

The top contact of the VLPC is fabricated by ion implantation and a subsequent thermal anneal to re-crystallize the surface, which is damaged by the ion implantation process. While ion implantation can result in a narrow donor distribution, the final thickness of the contact is limited by diffusion of the dopants during the thermal anneal. Laser annealing uses a fast ($\sim$ 10 ns) excimer-laser pulse to locally melt a thin layer at the surface. As the layer re-cools, it will re-crystallize and activate the implanted dopants on sub-microsecond time scales. This enables formation of very heavily-doped thin contacts ($\sim$ 20 nm) [47]. Some of this thesis work was devoted towards using a laser-annealed contact for development of the UVPC; however, resource limitations made it difficult to develop a working laser-annealing process.

Ultra-thin epitaxial contacts have been used to achieve nearly reflection-limited UV performance for CCD cameras. Low-temperature molecular-beam epitaxy was used to grow heavily-doped Si contact layers as thin as 1.5 nm on fully-processed CCD arrays [48]. This technology is very promising and offers opportunities for UVPC devices to approach the very high QE levels achieved by the VLPC at visible wavelengths. The UVPC detector work presented in this thesis shows that the QE of the VLPC in the UV is limited by the contact technology. Replacing the front contact of the VLPC with a Ti Schottky contact had no observable effect on the gain or noise properties of the VLPC (see Fig. 4.6). With improved contacts, high QE in the UV should be attainable using VLPCs.

Continued improvement to the QE of the UVPC will be important for applications in ion-trap quantum computation such as the state detection of trapped ions [17, 18] and remote ion entanglement [19, 20]. For the state detection of trapped ions a cycling transition is initiated by a resonant laser scattering a single photon after

each excitation. A fraction of the emitted single photons are collected amd focused onto a single photon detector generating a photo signal, I_p, proportional to the detector QE, η, and the incident photon flux, P ($I_p = q\eta P$). The resonant transition for most ions corresponds to UV wavelengths, leading to a need for high QE SPDs in the UV. The signal-to-noise ratio (SNR) of the detection process is given by [17]

$$\text{SNR} = \frac{I_p^2}{\left(\left(i_{th}/M\right)^2 + 2qI_pF\right)B + I_B^2}, \tag{7.2}$$

where i_{th} is the circuit noise, M is the internal gain of the detector, B is the measurement bandwidth, and I_B is the dark count rate of the detector. From Eq. 7.2 it is evident that the SNR is maximized for a SPD with high QE, high internal gain, low excess noise factor, and low dark counts. Improving the QE of the UVPC through the use of laser annealed or epitaxial contacts can increase the measurement bandwidth of the state detection process.

Remote ions can be entangled by interfering emitted photons on a beam splitter [19, 20]. This scheme is important for scaling to the large number of ions necessary for quantum computation [17, 20]. The success probability for the entanglement generation is given by [20]

$$\text{Success} = (p_{Bell})\left[p_\pi \eta T_{fiber} T_{optics} \xi \left(\Delta\Omega/4\pi\right)\right]^2, \tag{7.3}$$

where p_{Bell} is the probability of being in the Bell singlet state (1/4), p_π is the probability that the photon is in the correct polarization mode (0.5), η is the QE of the detector (0.15), T_{fiber} and T_{optics} are the coupling and transmission of the fibers and optics (0.2, 0.95), ξ is related to the branching ratio into a dark state (0.995), and $(\Delta\Omega/4\pi)$ is the solid angle of the light collection optics (0.02). The success probability for the entanglement generation is $\sim 2 \times 10^{-8}$ and with a repetition rate of 75 kHz, an entangled pair is generated about once every 12 minutes [20]. Improve-

ments to the solid angle and the QE of the SPD will significantly increase the success probability of the entanglement generation process.

In both the state detection process and the remote ion entanglement process the dark count rate of the detector is also very important. Reducing the dark counts of the UVPC while maintaining high QE will be critical to improving the usefulness of the UVPC to quantum computation applications involving trapped ions.

7.3 Infrared Photon Counter

The QE of the VLPC in the infrared (IR), particularly at the telecom wavelengths of 1.31 and 1.55 μm, is limited due to very low absorption of Si at these wavelengths. The absorption of incident radiation is given by $1 - \exp(-\alpha d)$, where α is the absorption coefficient and d is the thickness of the absorbing layer. One means of increasing the QE in the IR is to increase the absorption coefficient of the absorption layer by using a material for the absorption layer that has a higher absorption coefficient for IR radiation. Chapters 5 and 6 detailed development of this approach by means of wafer bonding an InGaAs absorption layer to the Si layers of the VLPC. An alternative approach is to increase the thickness of the absorption layer.

High-purity Si is practically transparent to IR radiation, but for doped Si, there is finite absorption of IR due to photoionization of the dopants. The SSPM and VLPC are very sensitive to LWIR due to this absorption mechanism. The SSPM has a relatively thick gain layer (30 μm) and demonstrated broadband QE in the 400 nm to 28 μm range with a minimum QE of about 3% occuring at $\sim$ 1.1 μm. If the thickness of the gain layer was significantly increased to $\sim$ 1 mm, the QE near the telecom wavelengths could be improved significantly. However, epitaxial growth of 1 mm thick gain layers is impractical and sustaining appropriately high electric fields in such a device would be challenging. Additionally, the timing jitter in such a device would be very high due to very long transit times of secondary

electrons in the drift region (see Sec. 3.3). A waveguide-type detector design would allow for mm-long absorption layers without increasing the grown layer thicknesses [150, 155]. The IR QE of a VLPC or SSPM would then only be limited by the coupling and guiding efficiency and absorption outside of the gain layer (such as within the contacts). Only about half of the VLPC thickness would be sensitive to IR radiation due to the thicker intrinsic layer and the addition of the spacer layer compared to an SSPM device, which is sensitive to IR in $\sim 80\%$ of the total thickness. Ideally, an SSPM-style waveguide detector would be used for a waveguide-type IRPC. A preliminary version of a waveguide-type SSPM had a QE $> 20\%$ in the 700 nm to 20 μm wavelength range [155].

An initial IRPC device was fabricated via wafer bonding of an InGaAs absorption layer to the Si absorption layer of the VLPC. However, the QE in the IR of this first device was practically zero due to the band alignment between InGaAs and Si (see Sec. 5.3). Incident radiation was absorbed by the intrinsic InGaAs absorption layer, but hole injection from InGaas to Si was blocked due to the large valence band discontinuity. While the QE of this device was very low, dark counts of the device showed that the device still functioned, and the gain properties were unaffected by the wafer-bonding process. If the band alignment can be tuned to remove or significantly reduce the discontinuity, high QE at telecom wavelengths should be possible for the wafer-bonded IRPC device enabling use in quantum cryptography experiments.

7.4 Heterojunction Band Alignment

Wafer bonding is a challenging endeavor; however, it allows for design of new devices and integration of existing devices. However, the band alignment of heterojunctions limits the design of devices where carrier transport across the junction is important. Control of the band alignment in combination with wafer bonding would allow for immense freedom in device design and could enable exciting breakthroughs in electronic

and optoelectronic device design. The control of interface dipoles at the heterointerface offer the ability to tune the band discontinuities of heterojunctions and can be integrated with the wafer bonding process by controlling the surface chemistry of the wafers prior to bonding. The UHV system presented in Ch. 6 was developed towards this goal of band alignment control for wafer bonded heterojunctions.

Interface dipoles are formed as a result of electronegativity differences between bonded atoms. An atom with stronger electronegativity tend to have a stronger pull over a shared electron resulting in the formation of a dipole due to the uneven distribution of charge. For Si wafer bonding, H plays an important role to both the bonding process and the magnitude of the interface dipole. Initial system results presented in Sec. 6.3 show the importance of H to successful bonding between InGaAs and Si. Hydrogen increases the magnitude of surface dipoles and results in stronger Van der Waals bondings compared to surfaces without H passivation. For surfaces with higher surface roughness (such as InGaAs ~ 2 Å), strong Van der Waals bonds are critical in bringing the mating surfaces close enough to form strong covalent bonds at high temperatures (see Eq. 6.2). However, the surface dipoles, which make bonding easier also have a strong impact on the band alignment of the heterojunction. In order to understand the impact of H on the band alignment of the InGaAs/Si heterojunction, smoother InGaAs surfaces are required.

Other possibilities for improving the bondability of InGaAs and Si without H involve passivating the Si or InGaAs surfaces with other electronegative species. Oxygen is very electronegative but results in large barriers to electron and hole transport at the interface. Other potential passivants for Si and InGaAs include S, Se, and Cs [156, 157, 158, 113, 159]. Testing the impact of these passivants will require integration of atomic sources for depositing interfacial layers with the UHV wafer bonding system described in Ch. 6. The impact of these interfacial layers on both the bondability and the band alignment will need to be studied through

bonding and band-alignment measurements.

8

Conclusion

Over the past two decades, the interest in quantum information science (QIS) has exploded and promising applications such as quantum information processing (QIP) and quantum cryptography (QC) are becoming achievable. QC has been commercially demonstrated with systems deployed and in use for secure communication. A number of physical implementations for QIP have been proposed and extensively developed. While significant improvements are still needed to perform useful computations, the progress of several implementations is promising. Photons are a integral part of certain QIP implementations and an essential component in QC. As such, there is a demand for high-performance detectors to measure single photons with high speed, high accuracy, and low dark counts. Other applications, particularly in biological applications for time-correlated single-photon counting (TCSPC) measurements, have a need for high-performance single-photon detectors (SPDs).

The VLPC is one of the highest-QE detectors available and can also distinguish photon number, which is particulary important for linear optical quantum computation and for use in repeaters for long distance QC. Chapter 2 details the design and operation of the VLPC, and the detailed theory that leads to the unique perfor-

mance of the VLPC. In Chapter 3. the timing jitter of the VLPC is measured and characterized as a function of operating conditions such as bias, temperature, and photon wavelength. The measurement shows that the VLPC has a low timing jitter of ~ 240 ps, which is particulary important for high clock-rate applications such as QC and TCSPC measurements.

While the VLPC offers high QE, photon number resolution, and low timing jitter, its usefulness in a number of QIS applications is limited as the high QE operation of the VLPC is limited to visible wavelengths. For applications such as state detection in the ion-trap implementation of a quantum computer, high-QE, single-photon detection in the UV is important. The low QE of the VLPC in the UV is attributed to absorption of incident photons within the top contact of the VLPC. In Chapter 4, the ultraviolet photon counter (UVPC), a modified version of the VLPC with increased QE in the near UV, is presented. The top contact of the VLPC was thinned and replaced with a thin Ti Schottky contact with a single-layer, MgF_2, AR coating. A system QE ranging from 5% at 300 nm to 24% at 400 nm was demonstrated. Improvements in contact technologies have the potential to increase the QE in the UV even further.

For applications in QIS requiring transmission of photons over long distances such as QC, high-QE SPDs at the telecom wavelengths of 1.31 and 1.55 μm are needed. The QE of the VLPC near the telecom wavelengths is low as the Si structural layers of the VLPC are practically transparent to infrared (IR) radiation. The infrared photon counter (IRPC) was proposed, which uses a InGaAs absorption layer that is wafer bonded to the VLPC structure to increase the sensitivity of the VLPC to the IR and particularly the telecom wavelengths. Integration of InGaAs and Si requires the use of wafer-bonding technology to fuse InGaAs to Si. Chapter 5 provides an introduction to the wafer-bonding process and details the InGaAs/Si wafer-bonding process used in this thesis work. The band alignment of the wafer-bonded InGaAs/Si

heterojunction was measured, which showed a valence band discontinuity of 0.48 eV and a conduction band discontinuity of 0.1 eV. The large valence band discontinuity between InGaAs and Si means that hole injection from InGaAs to Si, which is critical to the success of the IRPC, is greatly impeded. In Chapter 6, the design and fabrication of a ultra-high-vacuum system designed for understanding the impact of interface chemistry on the band alignment was presented.

Finally, in Chapter 7, the possible future directions and impact of this thesis work was discussed. Improved VLPC models are important for developing new VLPC devices that are optimized for different QIS applications. While the demands imposed on single-photon detectors for use in QIS applications are very high, the VLPC and modified versions, such as the UVPC and the IRPC, have the potential to meet these requirements.

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Biography

Kyle McKay was born in Lima, Ohio on September 19, 1983 and grew up in Reisterstown, Maryland. He graduated from Franklin High School in 2001.

In the spring of 2001, Kyle was accepted into the University of Maryland, Baltimore County's Meyerhoff Scholarship Program. Kyle began his tenure at UMBC in the summer of 2001 and graduated suma cum laude in May of 2005 with a Bachelor's of Science in Computer Engineering.

Kyle's graduate work began at Duke University in 2005 under the guidance of Professor Jungsang Kim. He received his Master's degree in electrical and computer engineering in May of 2008. Kyle will receive a Ph.D. in electrical and computer engineering at Duke University in December 2011.

Publications

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2. K. Mckay, S. Wolter, J. Kim, "InGaAs/Si fusion-bonded heterojunction," Poster at International Symposium on Compound Semiconductors, Santa Barbara, CA, August 2009