The SiPM readout electronics in NEXT

From NEXT-DEMO to NEXT-DBDM and NEXT-100

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Executive summary

This document starts with a revision of the existing readout electronics for NEXT-DEMO, based on gated integrators. A thorough description can be found in [1]. The described electronics allow single-photoelectron resolution, show excellent linearity and good measurement accuracy. The full NEXT-DEMO tracking plane is currently being read out using these electronics.

Two major drawbacks prevent these electronics from being used in NEXT-100: (a) power dissipation and (b) offset voltage control. The analog section of the NEXT-DEMO electronics dissipates 600 mW/ch, while the goal for NEXT-100 is approx. 30 mW/ch. The offset voltage control in NEXT-DEMO is done by hand, something we cannot afford in NEXT-100. Additionally, the gated integrator approach required one switch per channel and this may provoke a large noise in a ~7.000 channel system. Thus, a new approach, aiming at reduced power dissipation, enhanced offset voltage control and reduced number of switches has been developed and tested in NEXT-DBDM. This solution dissipates 125 mW/ch, reduces the number of switches in a factor of 16 and makes it unnecessary to adjust the offset voltage. This is accomplished thanks to the use of low-power, ultra low-offset-voltage amplifiers, to the use of a passive RC integrator with a 500 ns time constant (thus replacing the gated integrator) and a 2 MHz sampling frequency.

Based on the first results with NEXT-DBDM, we propose a readout solution for NEXT-100 that further reduces the power dissipation in the analog stage to 30 mW/ch sacrificing performance (higher offset voltage and noise). Power saving is accomplished using the same circuit topology as in NEXT-DBDM but replacing the operational amplifiers with lower power ICs. The increase in offset voltage requires some sort of compensation. We propose an automatic circuit based on a DAC (Digital-to-Analog converter) that adds very little additional power.

The readout solution is completed with analog multiplexers, analog buffers, multichannel ADCs (Analog-to-Digital converter), FPGA and LVDS transceivers. A 128-ch card architecture (FEB, Front-End Board) is proposed and its main design parameters are presented. Off-detector electronics already exist, as the NEXT-DEMO DAQ system will be re-used.

NEXT-DEMO electronics

A thorough description can be found in [1], so we will just highlight the main points in this section.

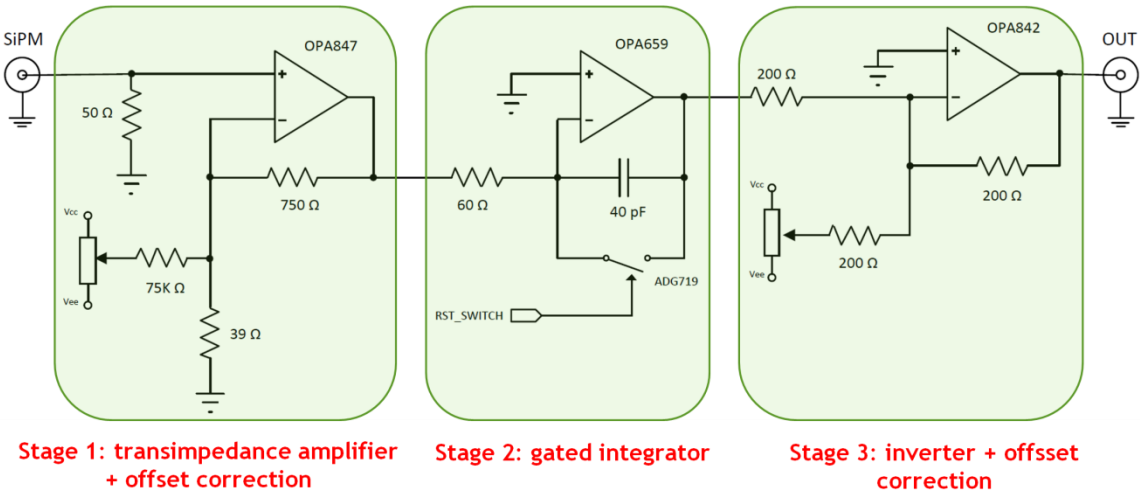

Figure 1. - The three-stage analog circuit for NEXT-DEMO

A current-to-voltage stage followed by a gated integrator and a buffer with offset control (third stage) are the heart of the NEXT-DEMO electronics. Sixteen analog paths are integrated in a readout board (Figure 2), together with a per-channel 12-bit ADC, an FPGA and an LVDS interface used to receive clock and commands from the upstream (and first) DAQ stage and to send digitized data.

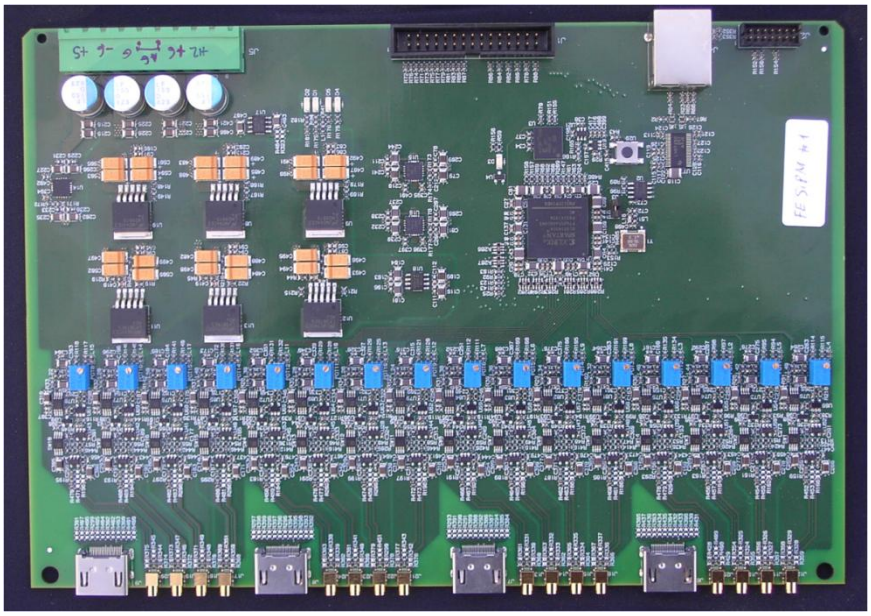

Figure 2. - The NEXT-DEMO readout board

Sixteen readout boards are enough to read out the whole tracking plane in NEXT-DEMO (248 channels). Performance is summarized in Figures 3a and 3b.

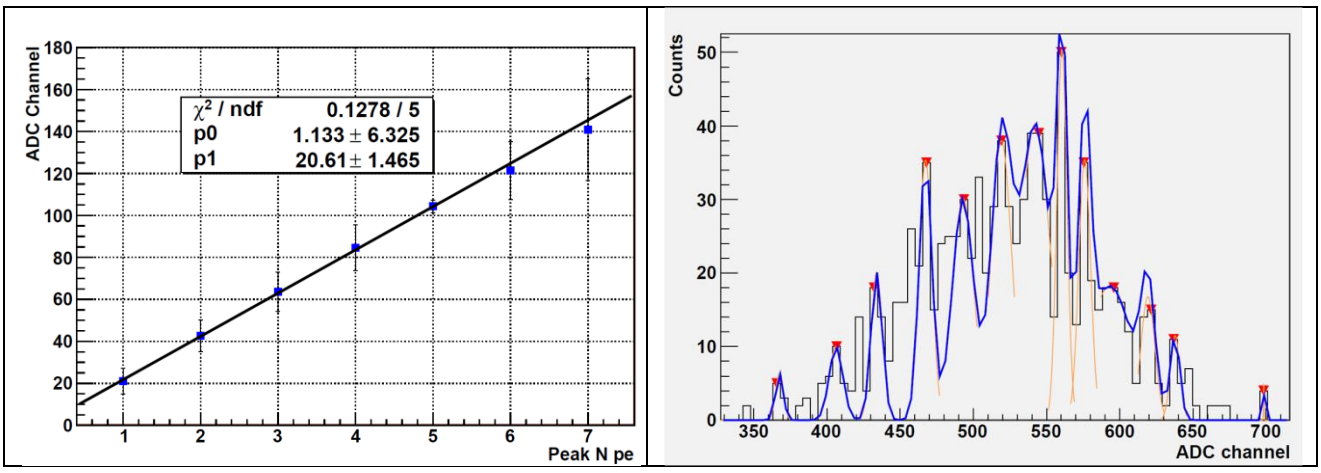

Figure 3a (left): excellent linearity and single-photoelectron resolution (1-to-7 photoelectron range). Figure 3b (right): Gaussian fit to the number of ADC counts produced by different photoelectrons

There are two major reasons for not using these electronics in NEXT-100: (a) power dissipation is too high (600 mW/ch) and (b) offset voltage adjustment by hand is required for every channel, which would be impractical in a ~7.000 channel in-vessel solution. Additionally, the gated integrator approach requires one switch per channel and this may provoke a large noise in a ~7.000 channel system.

Considerations for a NEXT-100 design

The driving requirements for the NEXT-100 in-vessel electronics design are power, reliability, cost, radiopurity and outgassing.

Very **low power** is a must as the heat is to be dissipated inside the vessel. The very front-end design and the ADC selection are key to achieve low power, as the number of channels is ~7.000. A power budget of approx. 350 W poses a limit of approx. 30 mW/ch on the analog circuit (210 W for 7 kch), as the ADCs and digital circuitry will require more than 100 W.

Highest **reliability** is mandatory as servicing the front-end requires to open the vessel, something we must avoid. Reliable PCB manufacturing, including stress tests (like thermal cycling and vibration), PCB and component selection and careful design are required if we aim at highly reliable in-vessel electronics.

Low cost per channel is required to reduce the budget, as the number of channels is approx. 7.000. Thus, analog electronics are the key section to overall cost reduction.

Even if the in-vessel electronics will be separated from the active volume by a copper shield, careful component selection is required to reduce the background. Once the passive component values are fixed, samples from several vendors can be tested to find out the cleanest ones. One of such studies, that include measurements carried out in Canfranc, can be found in http://radiopurity.in2p3.fr.

NEXT-DBDM electronics

A new approach, aiming at reduced power dissipation, enhanced offset voltage control and reduced number of switches has been developed and tested in NEXT-DBDM. This solution dissipates 125 mW/ch, reduces the number of switches in a factor of 16 and makes it unnecessary to adjust the offset voltage. This is accomplished thanks to the use of low-power low-offset-voltage amplifiers, to the use of a passive RC integrator with a 500 ns time constant and a 2 MHz sampling frequency. The analog circuit is shown in Figure 4.

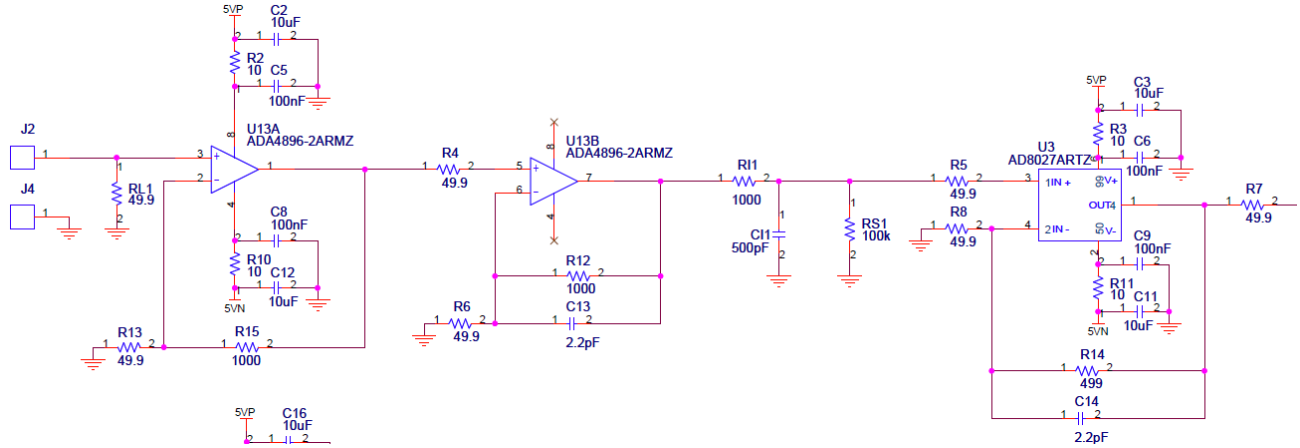

Figure 4. - The three-stage analog circuit for NEXT-DBDM. The gated integrator in NEXT-DEMO has been replaced by a passive RC filter

Two operational amplifiers (AD4896-2 and AD8027) have been chosen as they make a very low noise and offset voltage solution. A 4-channel board has been developed and tested at LBNL. It has 50-ohm termination for the SiPM cathode, two amplification stages (each one with a gain of 20) followed by a passive RC filter and a third amplification stage with a gain of 10.

The high gain (200 kΩ) aims at single photoelectron (spe) detection and at a 100-pe dynamic range using 25-micron MPPCs. Resolving spe allows tracking the gain, since it has been decided to avoid adjusting the bias voltage as the temperature changes for simplicity of the system. Figure 5 shows an average waveform from a 25 micron SiPM amplified and shaped with the front end card of the NEXT-DBDM electronics.

Figure 5. - Average waveform from a 25 micron SiPM (dark pulses) through the NEXT-DBDM front end card with a gain of 4,850 and the shaping time constant of 500 ns

In order to further reduce the dissipated power and simplify the electronics, the per-channel ADCs in the NEXT-DEMO solution are replaced by analog multiplexers, analog buffers and multi-channel ADCs. The concept is show in Figure 6.

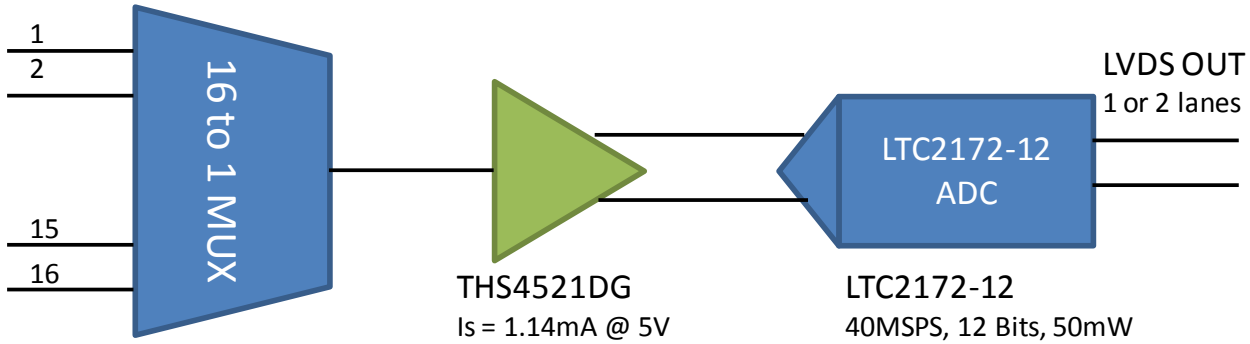

Figure 6. - Multiplexing scheme after the analog amplifiers

The multiplexer must be fast enough to allow 2-MHz sampling per channel and so the multiplexing factor may be reduced to the required level. A multiplexor board has been tested and optimized at LBNL. It consists of 16+1 switches controlled by a PLD. After the switches there is a unity-gain fully-differential amplifier that drives the signal that will come out of the pressure vessel and go straight to a 100 MHz digitizer (a total of 4 ADCs channels for a 64 channel system). Switching times of 28 ns (10 to 90%) have been measured. Figure 7 shows the switching of one of the 16+1 channels as captured on the scope.

Figure 7. – Switching speed of 28 ns in the 16+1 multiplexer channel NEXT-DBDM board. Channel 4 on this scope capture is the output of the differential amplifier immediately after the multiplexer switches.

NEXT-100 electronics

Based on the first results with NEXT-DBDM, we propose a readout solution for NEXT-100 that further reduces the power dissipation in the analog stage to 30 mW/ch, sacrificing some performance (higher offset voltage and noise). Power saving is accomplished using the same circuit topology as in NEXT-DBDM but replacing the operational amplifiers with lower power ICs. Figure 8 shows a survey of low-power operational amplifiers from Analog Devices.

Source: http://www.analog.com/static/imported-files/product_selection_guide/High_speed_amps_sel_table.pdf

Amplifier	Type	BW 3dB G=1 (MHz)	Noise (nV/√Hz)	V_{offset} (mV)	I_{bias} (µA)	$I_{quiescent}$ (mA)	Cost ($)	Power (V)
AD8005	CFA, single	270	4	30	10	0,4	1,63	5, ±5
AD8038/9	Single/dual	350	8	3	0,75	1	0,86/1,21	3, 5, ±5
AD8011	CFA, single	400	2	5	15	1	2,27	5, ±5
AD8014	single	480	3,5	5	15	1,1	1,19	5, ±5
ADA4841-1/-2	Single/dual	80	2,1	0,5	5,3	1,2	1,61/2,32	2.7, 5, ±5
ADA4940-1/-2	DIFF single/dual	240	3,9	0,4	1,55	1,25	1,79/2,95	3, 5
AD8029/30/40	Single/dual/ quad	125	16,5	5	1,3	1,3	0,86/1,21/ 1,62	2.7, 5, ±5
ADA4853	Single/dual/ triple	100	22	4	1,6	1,4	0,56/0,7/0,86	3, 5, ±5
AD8012	CFA dual	350	2,5	4	12	1,7	2,5	5, ±5
AD4896-2	Dual	230	1	0,5	17	3	3,2	3, 5, ±5
AD8027/8	Single/dual	190	4,3	0,9	6	6,5	1,2/1,91	3, 5, ±5

Valencia studies: higher noise and offset voltage but low power

LBLN prototype: higher performance but also higher power and cost

Figure 8. - Survey of low-power operational amplifiers from Analog Devices. AD4896-2 and AD8027 are used in NEXT-DBDM for very-low noise and offset voltage, though a penalty is paid in power dissipation. A design study at UPV uses AD8005 and AD8012 for lower power operation. Our proposal for NEXT-100 is to optimize the design using AD8011 AD8039.

As most of the time the SiPMs are not producing output current, most of the power consumption is just the amplifiers quiescent current. For a symmetrical ±5V operation, the power is $10 \cdot I_{quiescent}$. The proposed solution uses AD8011 in the first stage and the dual amplifier AD8038 in stages two and three, resulting in 30 mW/ch. There is a reduction factor of 20 compared to NEXT-DEMO and a factor of 4 compared to NEXT-DBDM.

The increase in offset voltage requires some sort of compensation. We propose an automatic circuit based on a DAC (Digital-to-Analog converter) at the input of the second stage that adds very little additional power. The new proposal also reduces the cost per channel. Amplifier cost (ICs only) is only $3,48.

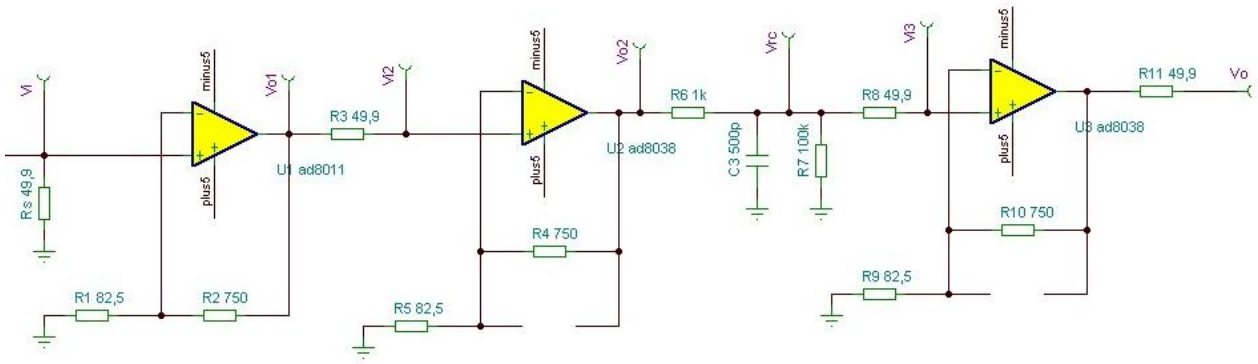

Figure 9.- Proposed analog circuit for NEXT-100. The operational amplifiers in NEXT-DBDM have been replaced by lower power ones

According to preliminary SPICE simulations, for a total gain of 50 kΩ (i.e., 50 Ω input termination followed by three stages with gain of 10) and 50-micron pitch MPPCs, output noise is 1,7 mV_{rms} and the output pulse amplitude for a single photoelectron is 10 mV. This allows a $2V_{pp}$/10mV=200 pe dynamic range.

Completing the in-vessel readout solution

Following a similar scheme as the one shown in Figure 6, the readout solution is completed with 8:1 analog multiplexers (ADG758), analog buffers (THS4521DG), multichannel ADCs (Analog-to-Digital converter) an FPGA (Xilinx Spartan-6) and LVDS transceivers.

A 128-ch card architecture (FEB, Front-End Board) is proposed (Figure 10). On the right, two flexible flat cable (FCC) connectors service two 64-ch DBs in the tracking plane. Most of the board area is used by the 128 three-stage amplifiers. On the left, sixteen 8:1 multiplexers produce sixteen analog signals which are digitized in two 8-channel ADCs with LVDS outputs. A low-power FPGA reads out the ADCs, controls the sixteen 8-ch DACs for offset voltage control and communicates with the off-detector DAQ using LVDS signals (clock, commands and trigger as inputs, data as output).

The board has an approximate size of 19,5x12,5 cm. This fits in the available volume in the endcap (Figure 11). FEBs are placed radially, approx. 15cm away from the center, mounted on copper fins attached to the shield for heat removal. If required, the vessel outer surface can be cooled to evacuate the heat.

Off-detector electronics

The DAQ system for NEXT-DEMO (based on NEXT-LVDS interface boards, NEXT-RD51 FEC cards, gigabit Ethernet links, DAQ PCs and the ALICE-DATE online system) [1-2] is a working solution (more than 1 million events have been already recorded) that will be used for NEXT-100. This will just require some firmware modification in the FEC cards, so most of the work is already done.

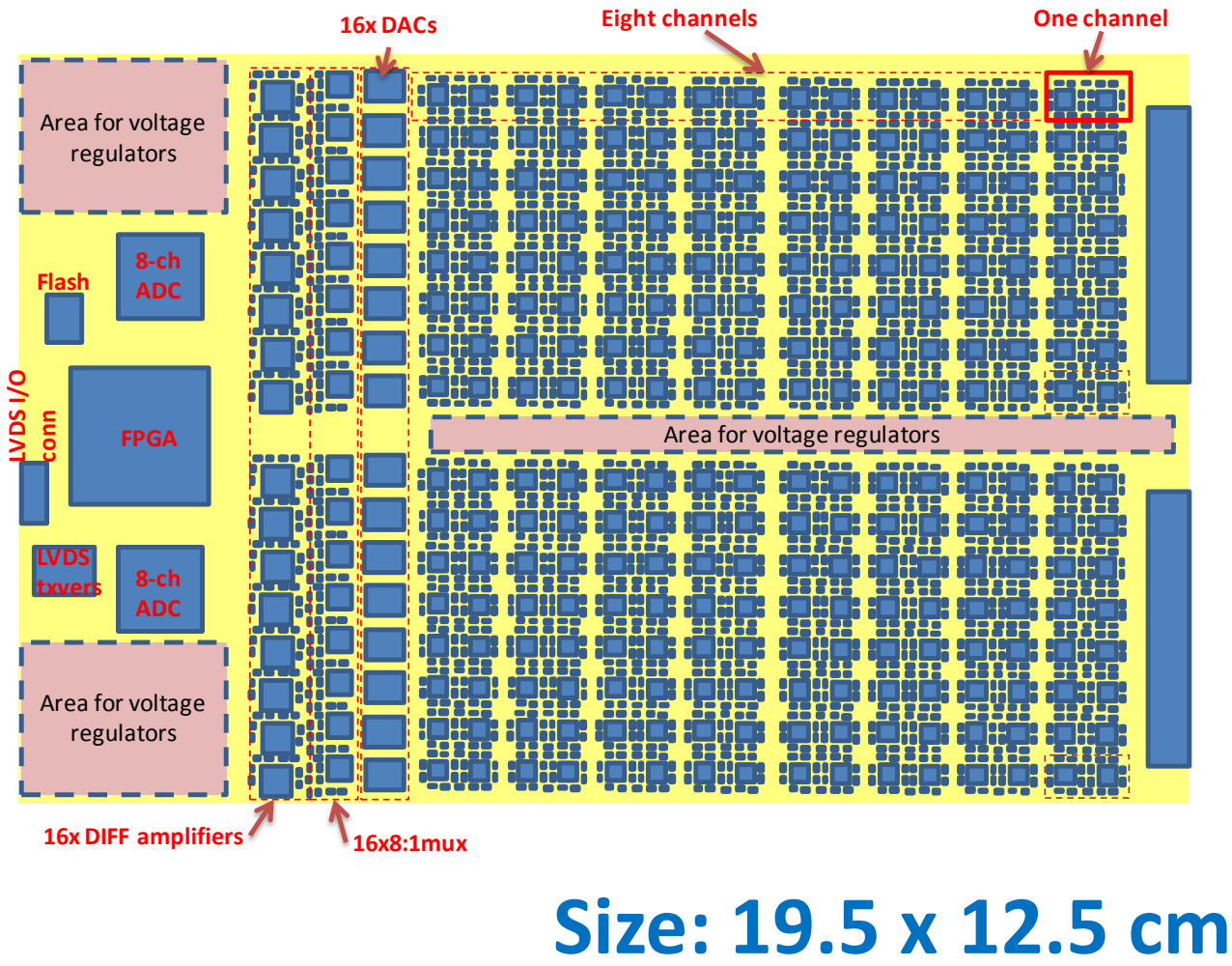

Figure 10. - Sketch of a 128-ch Front-End Board (FEB).

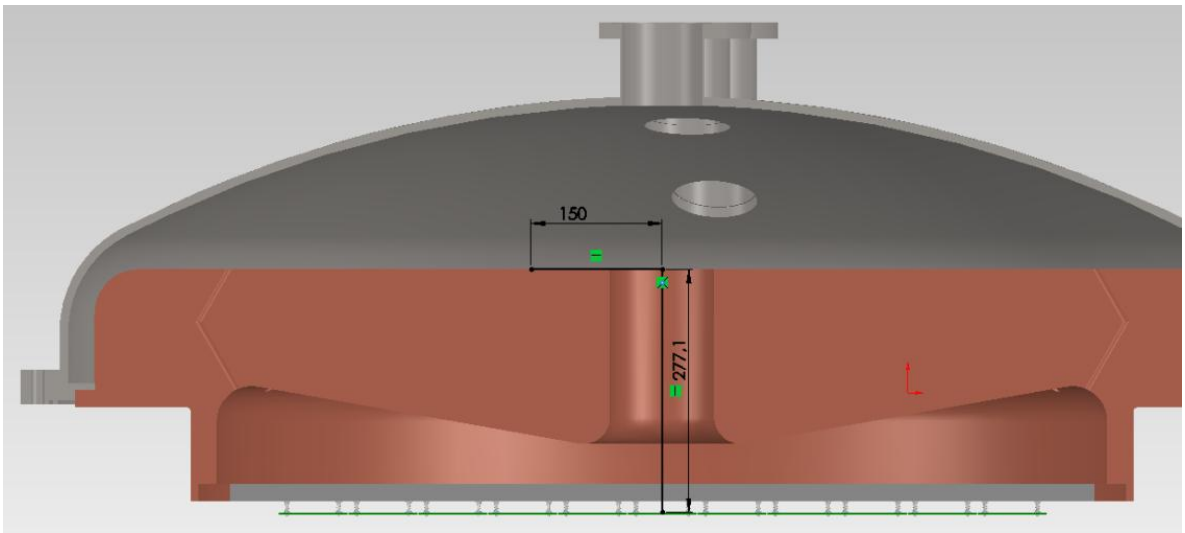

Figure 11. – The tracking plane endcap showing the copper shield (brown). Front-end electronics will sit behind the shield, in a radial configuration. A total of 7.000/128 = 55 boards are required (spaced 360º/55 ≈ 6,5º). There's a hole in the center of the shield to pass the approx. 110 flexible flat cables from the DBs to the FEBs

References

[1] V. Herrero et al., *"Readout electronics for the SiPM tracking plane in the NEXT-1 prototype,"* presented at NDIP 2011, proceedings published in Nuclear Instruments & Methods in Physics Research Section A (2011). Available online: http://dx.doi.org/10.1016/j.nima.2011.12.057

[2] J. Toledo et al., *"The Front-End Concentrator card for the RD51 Scalable Readout System,"* Journal of Instrumentation, Vol.6, issue: 11, November 2011, doi:10.1088/1748-0221/6/11/C11028