Electronics alternatives for NEXT100+

28 May 2013

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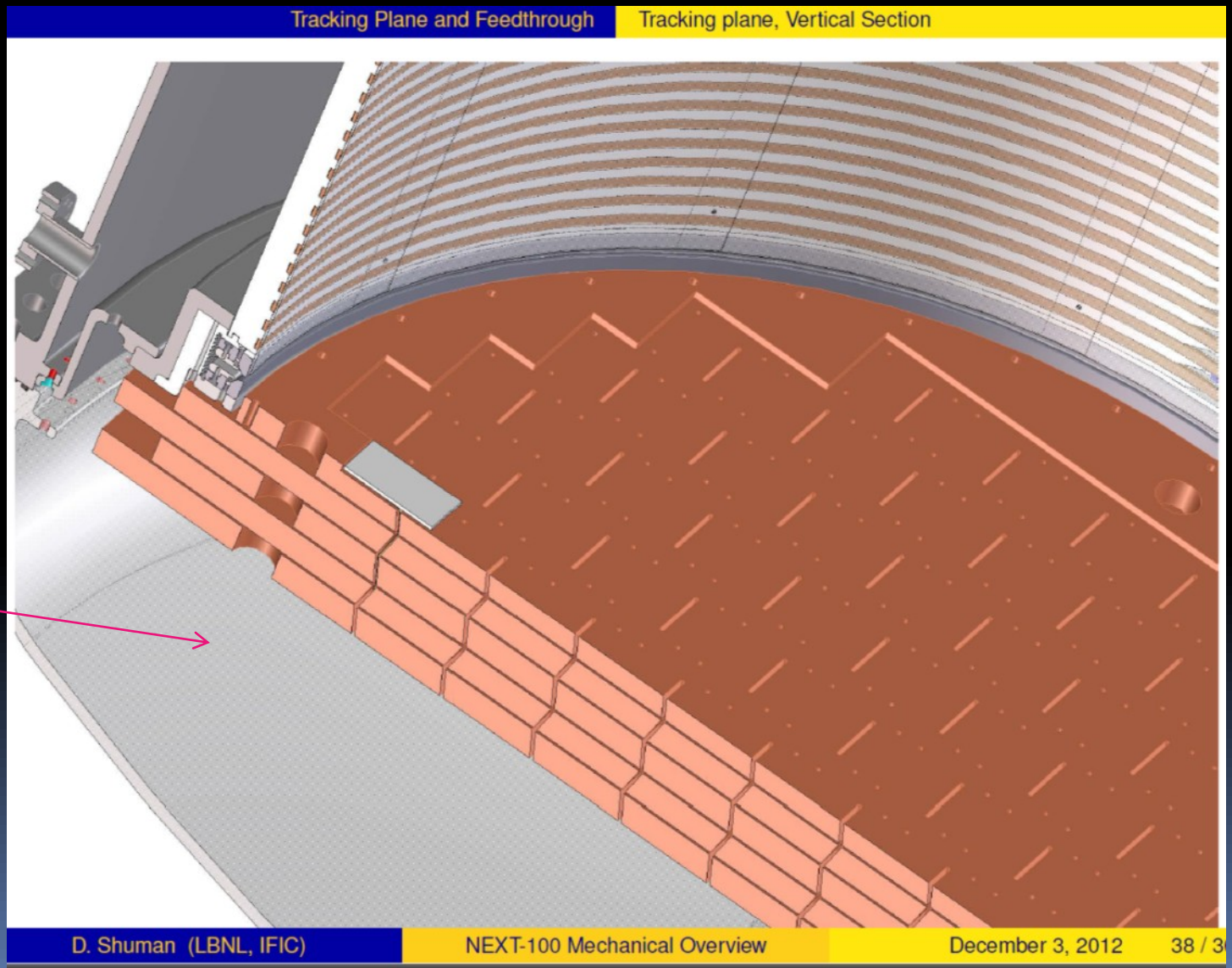
Goal: Propose ideas that

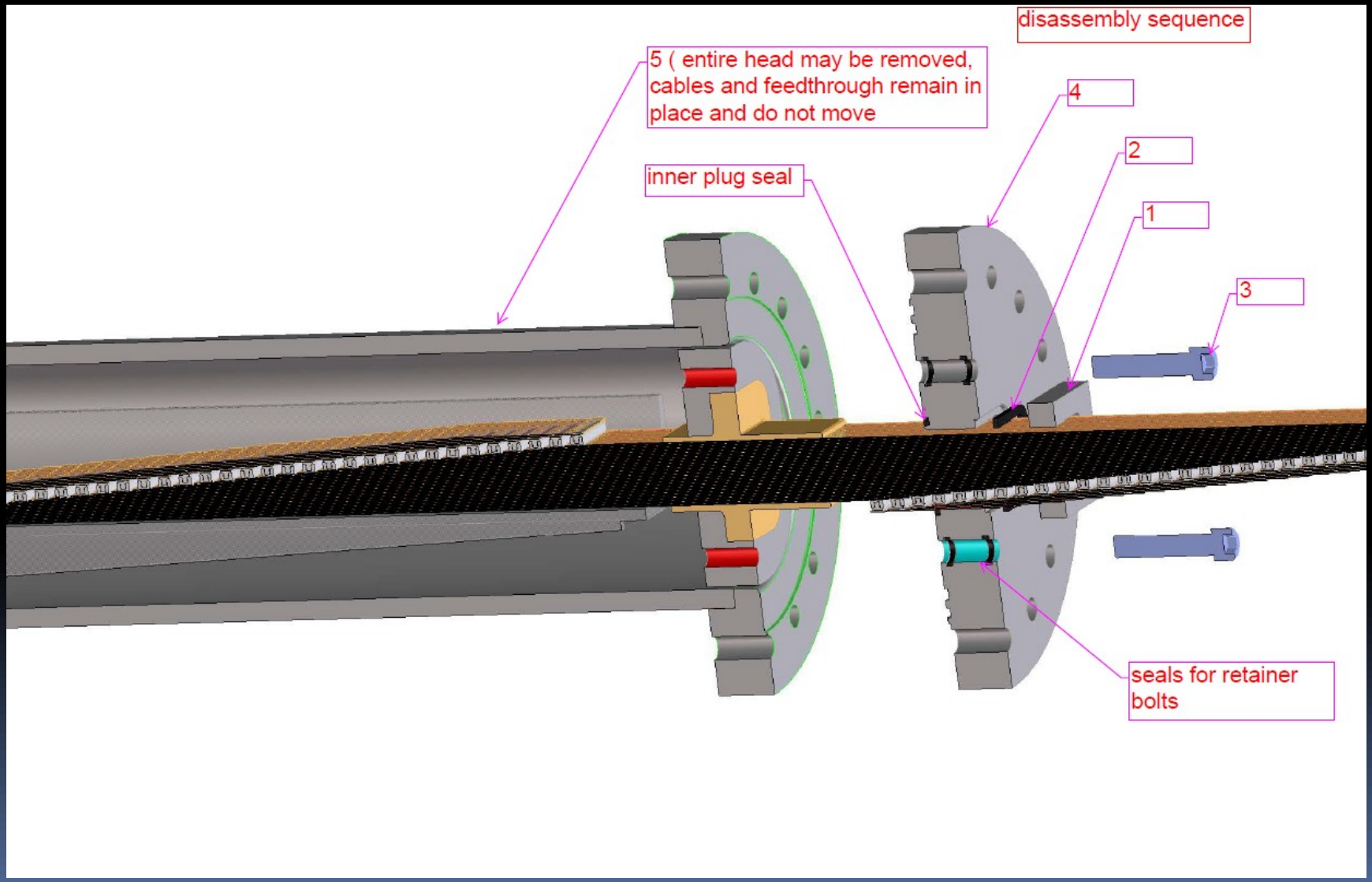
- Can keep a level of involvement with little $
  - Something can be done for a ~$20k
- Are a strength for Fermilab
  - Direct experience, good eng resources
- Help NEXT
  - Or at least don't interfere!

SiPMs Tracking plane



Is this area filled with HP Xe?
Does it need to be?

SiPM signal feedthrough



3 “features”

- Move active electronics forward
  - Separate “pressure barrier” from “Xe barrier”?
- Reduce number of conductors in the feedthrough
  - Multiplexing without switches?
- Make the feedthrough simpler
  - Can you have connectors that connect from a distance?

Reducing conductors: mux

- There are many reasons not to mux inside the detector:
  - Complexity
  - Reliability
  - Power
  - Noise

- One reason to multiplex:
  - feedthrough

The point

The NOVA APD Readout Chip

Tom Zimmerman
Fermilab - Particle Physics Division
October 31, 2007

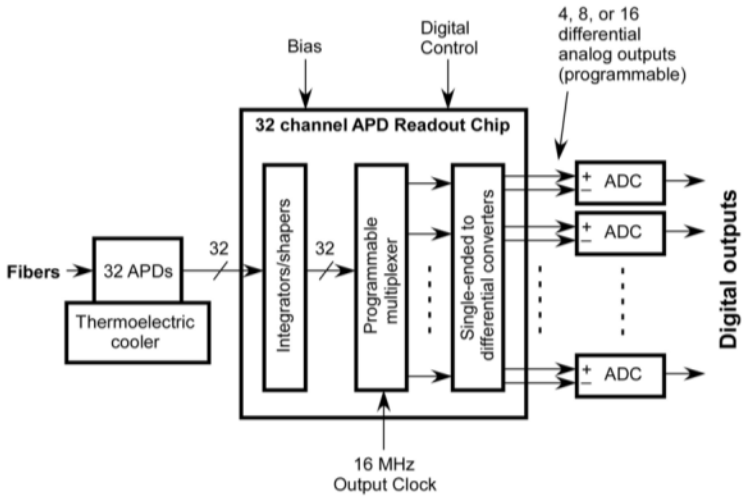


Figure 1. NOvA APD readout system front end

Interesting specs

- Mux by 2:1 or 8:1 or 16:1
- Rise time adjustable from 35ns to 780ns
- Fall time adjustable from 20us to ~0.5us
- Power is ~3 to 5 mW/ch (adj bias current)
- Noise is < 200e equivalent @ 10pF
  - too good, too much gain (lowest is 22mv/fc)
  - Could easily be 200 times worse and be ok!

Circuit description

Figure 2 is a more detailed depiction of the internals of the final readout chip.

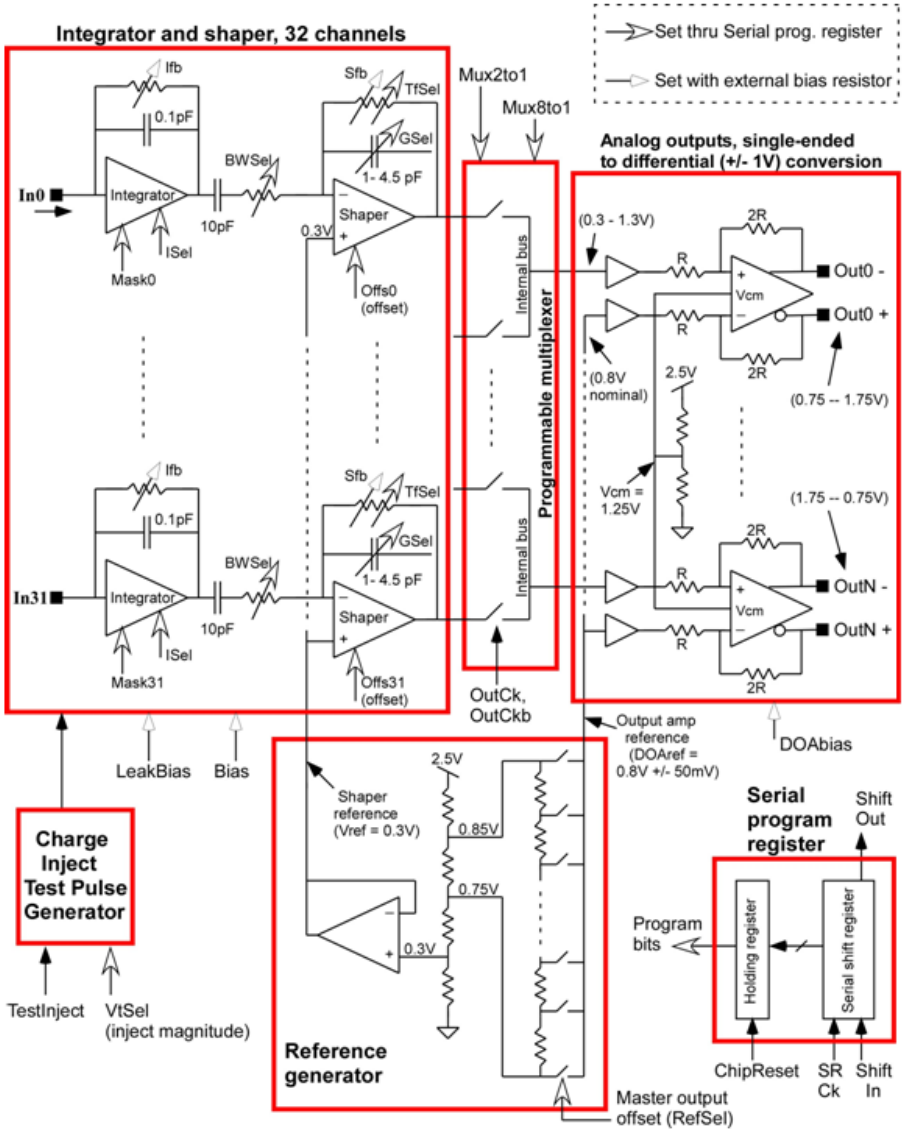
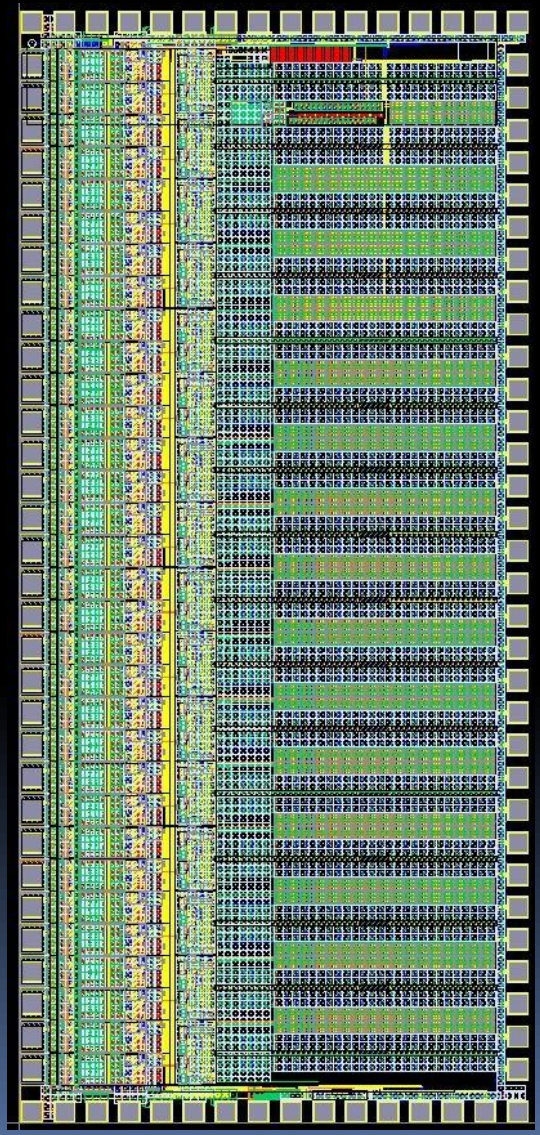


Figure 2. NOvA readout chip

No such thing as a free lunch: Using the NOvA ASIC for NEXT

- Would need to be tweaked for lower gain
  - So there would be some engineering
- Could be made to work with NO or LITTLE external bypass capacitance
  - Definitely needs some engineering by designer

A large fraction of the area is “fill”



FAQ: using the NOvA ASIC

Q: Is it expensive? A: ~$30k for 2x

MOSIS QUOTATION

To: deptuch
FNAL
, IL 60510

deptuch@fnal.gov

Quote ID: 171573-A
Date: 23-APR-2013
Expires: 23-MAY-2013
Payment Terms: See below
MOSIS Account: 573-COM-RLAB/FERMI

Issue Purchase Order to: University of Southern California **Tax ID:** 95-1642394

Item	QTY	Unit	Part No	Description	Unit Price	Extended Price
1	1	LOT	12400	Lot of 40 TSMC 0.25 um Mixed-mode MS G ICs (minimum 25mm^2) Price based on area of 6 mm^2.	14,000	14,000
2	5	LOT	12403	Additional lot of 40 TSMC 0.25 um Mixed-mode MS G ICs (minimum 25mm^2)	1,500	7,500
						=======
						21,500

These prices include Federal Express 2 day shipping; delivery is best effort.

Terms and conditions are defined in the customer agreement signed by your organization on 28-MAR-1990.

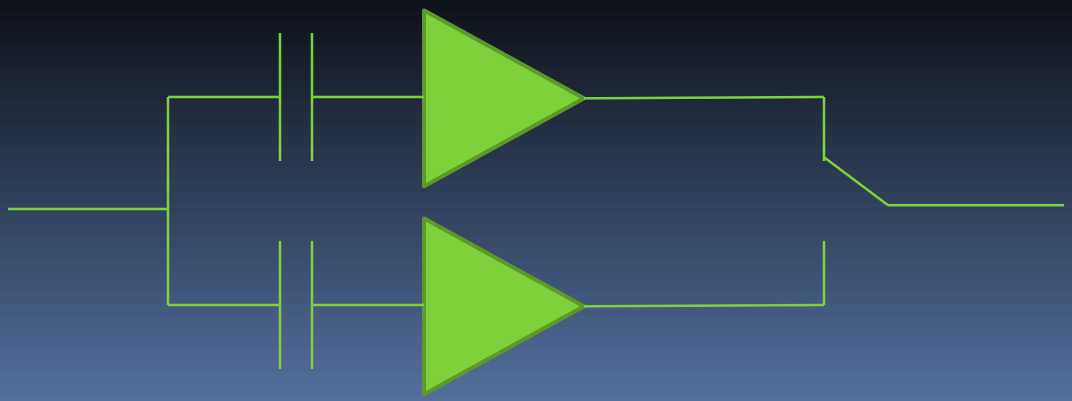
FAQ: using the NOvA ASIC

Q: Is it reliable? A: 0.25um TSMC is very reliable, mature, stable and popular. Typical yields are in the mid 90s

NOvA ASIC is a fairly simple chip- analog mux

Use 2x number of chips needed

Idea would be to capacitively split the signal to two chips- power one or the other

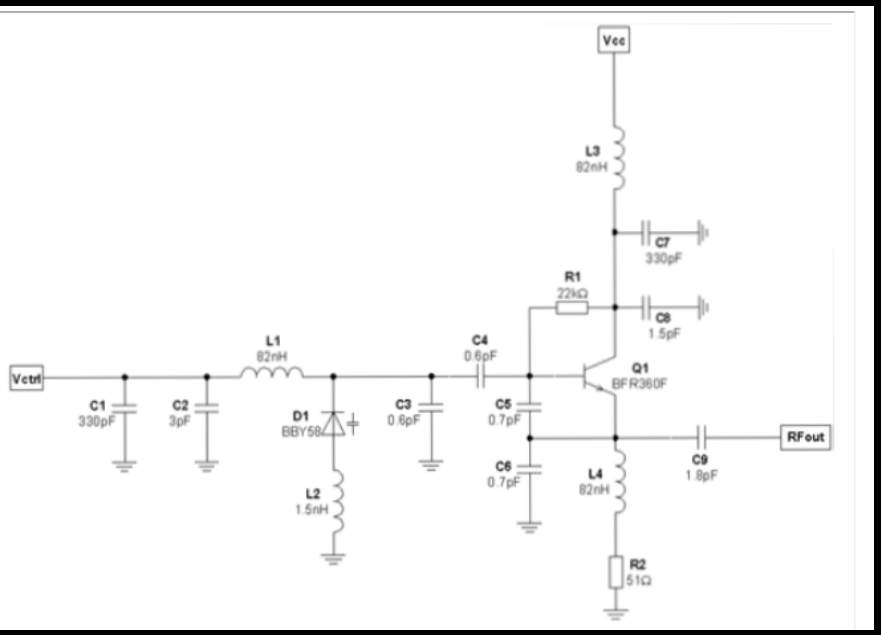


Other ideas

- The NOvA chip is a type of Time Division Multiplexing
- It is also possible to utilize Frequency Division Multiplexing

- Basic idea: use a low voltage tuning diode to "tune" a VCO based on the output of the amplified SiPM signal

Freq Div continued

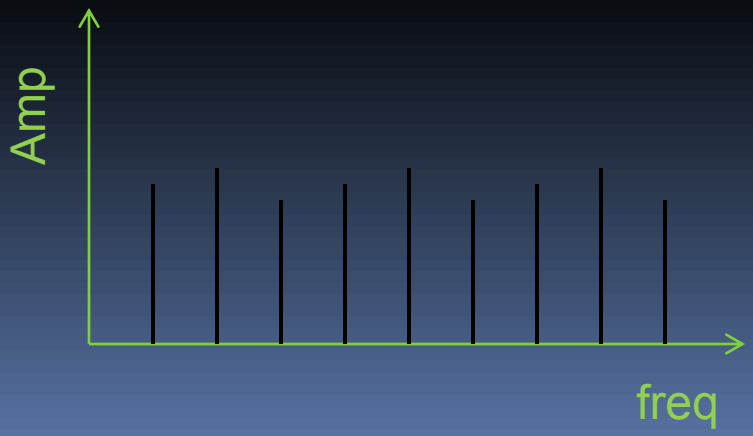


Advantages:

- few components, cheap
- low power (5mW/ch added)
- simple

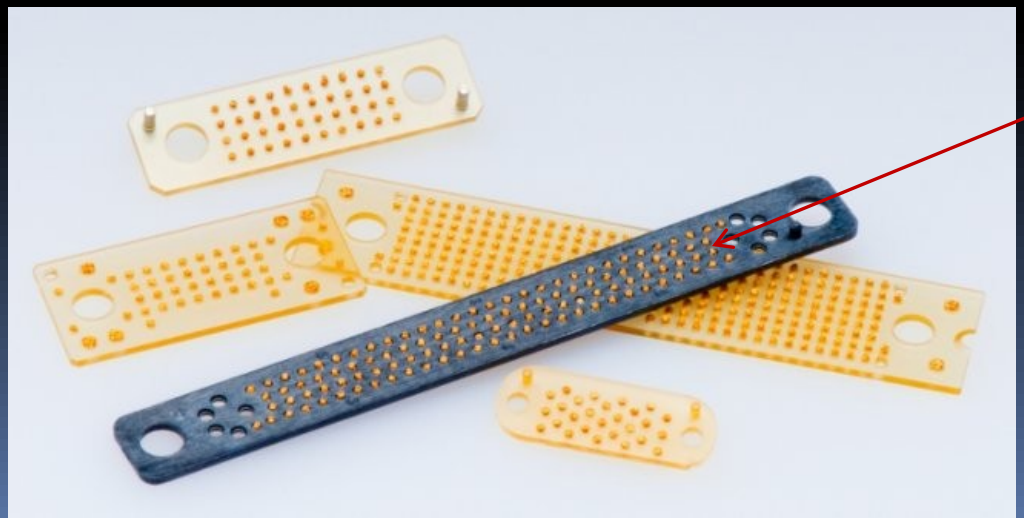
Disadvantages:

- very limited dynamic range
- need good cables
- somewhat limited multiplexing (16:1)
- limited time response (>1us)

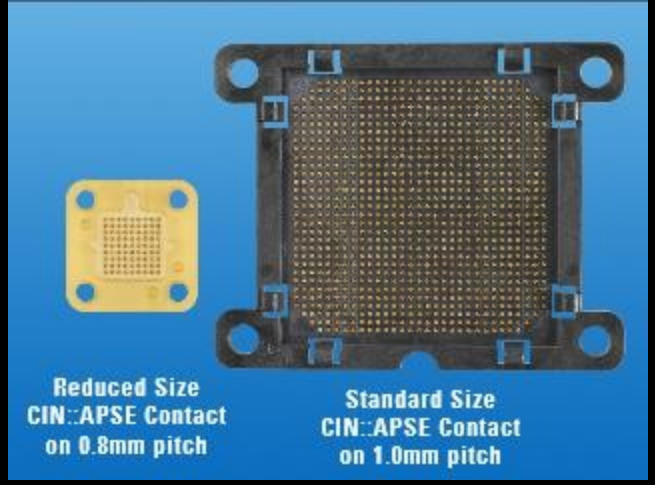


More other ideas

- Remote connectors?
  - Dzero tracker had a similar problem- must make connections (>100k in all) where there was no space for hands:
- Solution: cin:apse connectors from Cinch



CIN:APSE

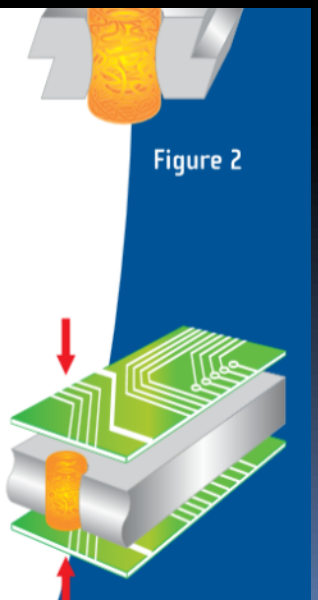


- Can be very dense: ~100 contacts/sq cm
- Just squeeze between two PCBs (5g/contact) (can be FPC, with rigid backing)

The basic CIN::APSE contact configuration consists of a contact installed into a customized plastic insulator with the patented Cinch hourglass hole design (Figure 2). Once in place, the contact extends on both sides of the insulator.

Quick, Solderless Installation

CIN::APSE is easily installed in two basic steps, without soldering. First, using alignment features, the CIN::APSE interconnect is positioned between two components with matching connection footprints. Next, the two components are compressed and fastened together (Figure 3).



Conclusions

- We want to be involved in NEXT

  (because Adam said so)
- We have little support, but I would like to offer some ideas that
  - Are in line with Fermilab expertise
  - Don't require huge resources
  - Don't interfere with NEXT progress