1.1 Trap L1ID and BCID values in EFB

L1ID and BCID data can be trapped on the EFB to allow the user to view diagnostic data when event synchronization issues occur. The trap operates on single events only and the global enable signal must be cleared and set prior to filling the internal memory used to store the Event ID data. The trap engine operates on each EFB data processing path independently, and each path can process separate events simultaneously, so in a single trap run there may be data from 2 different L1 triggers in the data record. The trap implementation includes a Global Enable signal, a Trap Full signal, a single register location to latch the current TTC values for L1ID and BCID, and a block of memory to store the Module L1ID and BCID and the calculated L1ID values. The structure is shown in the tables below:

Description	REG ID	Address	Access	Width
EFB: EFB Command 0 Register, EFB_CMND_0	1A4	00402210	RW	32
			Bit Value	
			1	0
Bit 11 : L1ID Trap Enable When this bit is set, the EFB will trap L1ID values in a block RAM. Describe the Trapping algorithm			Enable	Idle

Description	REG ID	Address	Access	Width
EFB: Run-Time Status Register, EFB_RUNTIME_STAT_REG	1A6	00402218	R	16
			Bit Value	
			1	0
Bit 11: L1ID Trap data ready for read out			Data Ready	Idle

Description	REG ID	Address	Access	Width
EFB: L1ID/BCID TTC Trap Value		0040227C	RW	1
The TTC values for BCID and L1ID when trapping Event ID data.			Bit Value	
			1	0
Bits[3: 0]: EFB Engine 0 – TTC L1ID			Value	
Bits[15: 8]: EFB Engine 0 – TTC BCID			Value	
Bits[19:16]: EFB Engine 1 – TTC L1ID			Value	
Bits[31:24]: EFB Engine 1 – TTC BCID			Value	

Description	REG ID	Address	Access	Width
EFB: Link/Module L1ID/BCID Trap Value			R	32
Link0/Link48 Trap Values		00402280		
Link1/Link49 Trap Values		00402284		
…				
Link46/Link94 Trap Values		00402338		
Link47/Link95 Trap Values		0040233C		
Event ID data value trap memory. The data field includes the L1ID and BCID values received from the module or chip and the expected L1ID value used in the error checking process. [n=0 to 47]			Bit Value	
			1	0
Bits[3: 0] : Module/Chip L1ID – Link(n)			Value	
Bits[7: 4] : Expected Link L1ID – Link(n)			Value	
Bits[15: 8] : Module/Chip BCID – Link(n)			Value	
Bits[19:16] : Module/Chip L1ID - Link(n+48)			Value	
Bits[23:20] : Expected Link L1ID – Link(n+48)			Value	
Bits[31:24] : Module/Chip BCID – Link(n+48)			Value	

To operate the L1ID/BCID trap, at any time before or during data-taking, set the L1ID trap enable signal, Bit[11], in the EFB_CMND_0 register to value '1', then monitor the L1ID trap data ready bit in the EFB_RUNTIME_STAT_REG register. When the value of Bit[11] is '1', read out the data from address locations 0x0040227C to 0x0040223C. To restart the trap, clear the L1ID trap enable signal and check to see that the L1ID trap data ready signal value returns to '0', then set the L1ID trap enable signal to value '1'.