ATLAS Pixel Electronics

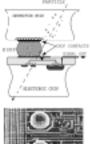## Analog/Digital IC Design, VHDL and Software Engineering, High Speed Board Design

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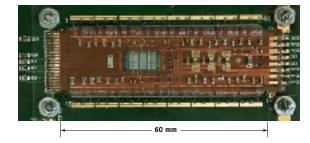
The PIXEL Concept

The pixel sensors are fabricated in much the same way as conventional silicon microstrip detectors. One side of the sensor is segmented into individual pixel implants, each forming a junction diode to the implanted back surface. During operation the sensor is reverse-biased so that the bulk material is depleted of free carriers. For ATLAS the pixel implants have a pitch of 50 μm in the r-ϕ direction and 400 μm in z (300 μm in the B-layer). Each pixel implant is DC-connected to a dedicated electronic readout channel using a bump-bond. The readout channel comprises a charge-sensitive preamplifier AC-coupled to a fast discriminator.

When a charged particle traverses the bulk sensor material, free electron-hole pairs are liberated along the path. These drift in the electric field that exists across the sensor (due to the bias potential), resulting in a fast current pulse in the pixels that reside close to the interception point. The discriminator thresholds are finely tuned such that minimum-ionizing particles (MIPs) are detected at high efficiency (>99%) while fake hits arising from noise are suppressed.

Each module in the ATLAS pixel system (of which there are 2,228) is composed of a single sensor tile bump-bonded to 16 front-end chips. There are 2,880 pixels in each FE chip arranged into 18 columns X 160 rows; thus each module has a total of 46,080 channels, (except in the B-layer, where the finer z-pitch results in 61,440 channels per module). The total number of channels in the pixel tracker is around 140 million.
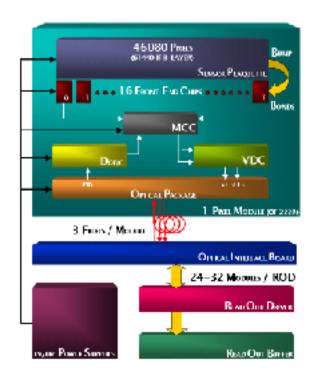

60 mm

Pixel System Electrical Scheme

Each individual FE chip has a single LVDS output that transmits data at 40 MHz. These data contain information corresponding to the pixel location and charge of any hits that have been encountered. The readout sequence is initiated by the arrival of a level-1 trigger, which has a precise latency relative to the beam-crossing within which the triggered event occurred. Any hits occurring that are not matched by the arrival of a trigger are deleted from the storage buffers that exist on the FE chip.

Each module is served by a single module-controller Chip (MCC), which has 16 input FIFOs to receive the serial data streams from the FE chips. Local module "events" are constructed within the MCC for subsequent transmission on 1 or 2 output links (each of which may operate at 80 Mbits/s using NRZ-protocol). The MCC is also responsible for providing the common control waveforms and clocks to the FE chips along with distributing level-1 triggers.
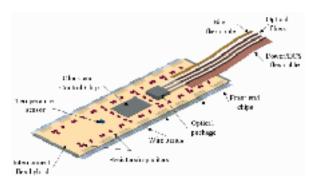
Optical fiber links are incorporated for all data transmission to and from the modules to achieve the requisite bandwidth. Thus each module has dedicated optical receiver/decoder chips and transmission components.

Module Hybridization

This diagram depicts the hybridization scheme incorporated in the inner and outer layers along with the forward discs. The lowest layer of the module is formed by the FE chips, which have their backplanes in intimate thermal contact with the integrated support and cooling structure. The FE chips are bump bonded to the sensor tile, which in turn has a flex-kapton bussing piece glued to its back surface. The FE chips protrude along the long edges of the module so that they may be connected up to the flex-hybrid using conventional wire bonds. The hybrid provides all necessary connections to the MCC, which sits near the center. All local power-decoupling capacitors, along with some temperature-sensing components, are incorporated into the hybrid.
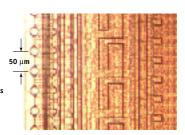

The power for the electronic components, along with the high voltage used to bias the sensor, is provided individually for each module. These supplies are located remotely along with the off-detector readout electronics at 150 m from the ATLAS detector. At the heart of the off-detector readout electronics is a read-out-driver (ROD) board, which uses state-of-the-art gate-array technology to control and read out up to 32 modules. The ROD also incorporates a DSP-based back end, which has the intelligence to perform dedicated module testing and calibration.

Front-End Readout Electronics

LBNL plays a major role in the synthesis of the FE electronics design. The upper photograph shows one corner of the latest FE chip (FE-D) which was fabricated using the radiation-hard DMILL process. The lower photograph shows an area of the chip containing 6 individual pixel cells.
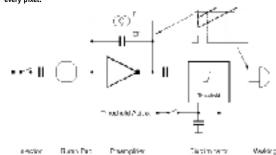
The block diagram below depicts the basic functionality of an individual readout channel. Each pixel has its own digital logic at the back end that may store the timing and charge information of a hit locally, along with indicating the presence of such a hit to the end-of-column (EoC) readout logic. Each pair of columns (comprising 320 channels) is served by a data bus that connects all pixel back ends to a set of 24 buffers at the bottom of the chip. Here the hits are stored for one level-1 trigger latency period. If a matching trigger is encountered, then the hit information is strobed serially off the chips, otherwise being deleted.

50 μm

Other logic blocks in the EoC region of the chip include a 16-deep FIFO for level-1 trigger storage and a 7-bit Greycode generator used to provide the 40 MHz timestamp information (corresponding to the beam cross over frequency), which is distributed to every pixel.
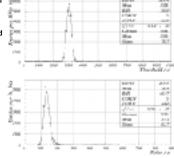

Requirements

The analog front-end circuitry must be fast enough to associate particular hits to the correct beam cross-over (BCO) with one crossing occurring every 25 ns. Meanwhile the equivalent noise charge should be less than 250e-, while the power consumption is restricted to <40 mW per pixel. The crosstalk between neighboring pixels must be less than 5% at a pitch (in r-ϕ) of 50 μm providing the best possible spatial resolution.

One of the greatest challenges for the ATLAS pixel tracker is that it must withstand the most extreme radiation exposure over the course of its 10-year lifetime while still delivering a hit-finding efficiency of >97% and a fake hit occupancy of < 10^{-5} per pixel per trigger.
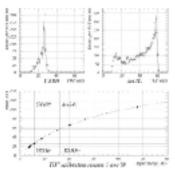
Hadronic radiation causes lattice defects in the bulk sensor material, thus increasing the required bias voltage. Electromagnetically interacting radiation is most harmful to the readout electronics, since this causes an enhancement of trapped charges at the semiconductor-dielectric interface. The total hadronic fluence anticipated for the inner layer is 10^{15} per cm^2, while the electromagnetic dose is around 50 Mrad. The B-layer has even higher exposure levels; for this reason it will be replaced after ~4 years.

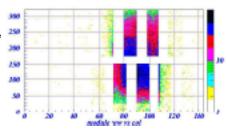## Laboratory and Testbeam results

This plot shows distributions of threshold and noise measured on a prototype pixel module in the laboratory. Every channel has its own 3-bit DAC, which may be used to make fine adjustments to the threshold, thus providing a means of overall threshold dispersion reduction. This module has been tuned to the nominal operating threshold of 3000e-; the dispersion is measured to be 171e-. The noise distribution peaks at 137e- ENC.

The time-over-threshold (TOT) charge measurement is calibrated in the laboratory using two photon sources (Cd109 and Am241). The upper two plots show the spectra derived for one particular pixel. In the lower plot the amplitude of a calibration input voltage step (applied to the 10-fF calibration capacitor which exists for each pixel) is plotted against the mean TOT obtained. When the values for the fitted Cd109 and Am241 photo peaks are compared, an agreement of < 5% is obtained for this channel.

The following is a hit map obtained from a prototype module in a testbeam at the SPS accelerator facility at CERN. The beam profile is seen to overlap around 9 of the FE chips at once.

A 4-stage silicon microstrip hodoscope was used to extrapolate the particle tracks to the module position with an accuracy of 3 μm from which an overall hit efficiency of 99% was derived. The overall resolution in the r-ϕ dimension is measured to be 13.5 μm.