ELECTRONIC PACKAGING & SPACE PARTS NEWS

EEE Links

July 1998, Vol. 4 No. 3

In this issue:

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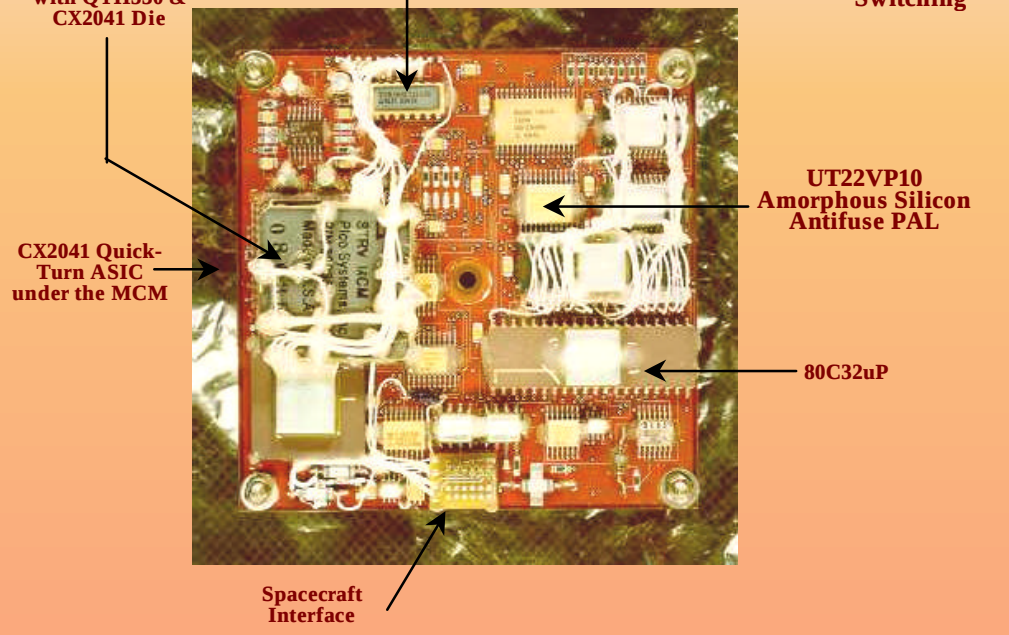

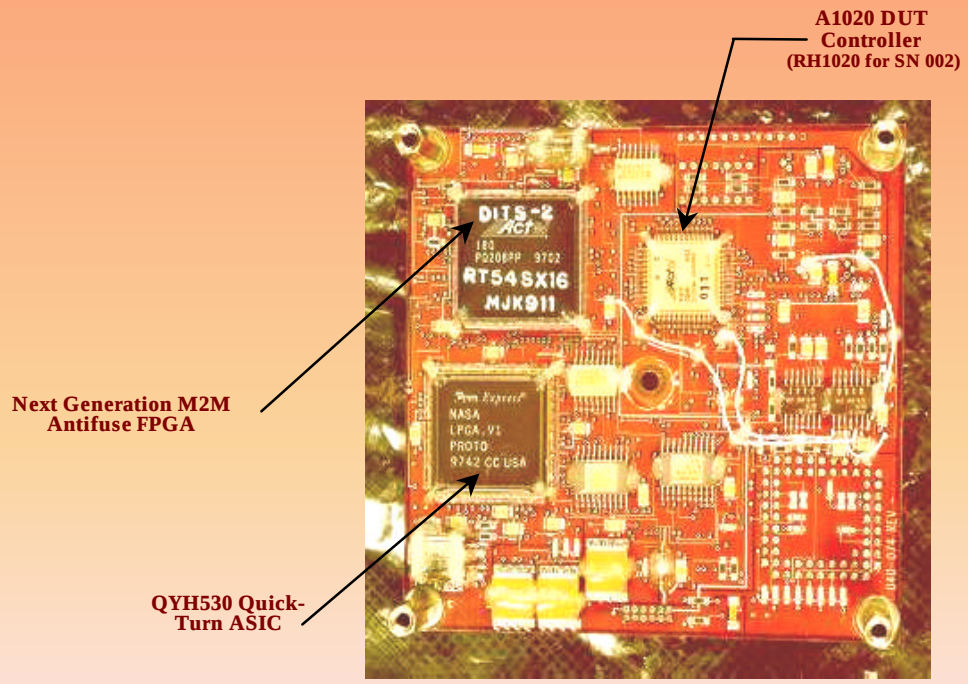

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The above picture shows both sides of a STRV-1d/COTS-2 flight card. The card incorporates a number of technologies, including quick-turn ASICs, prototype next-generation FPGAs, radiation-hardened FPGAs and PALs, programmable substrates, plastic packaging, a fuzzy logic processor, compact HEXFETs, and a variety of commercial memory devices. The card is heavily instrumented to measure the affects of the space radiation environment on the components and data will be compared with that obtained from the ground test program

c o n t e n t s

Articles

Articles

Letter from the Editor

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Welcome to the July issue of EEE Links. In the last issue I mentioned that in an effort to improve accessibility to the electronic version of the EEE Links we switched to a PDF format for the EEE Links Web page. In addition we are also in the process of updating past issues to the PDF format.

Please note the new URL address for EEE Links is http://misspiggy.gsfc.nasa.gov/ctre/hq/eee_links.

As always, please keep us informed with your questions and needs so we may be able to better provide the information you need and want.

1998 Military and Aerospace Applications of Programmable Devices and Technologies Conference

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The conference will address devices, technologies, usage, reliability, fault tolerance, radiation susceptibility, and applications of programmable devices and adaptive computing systems in military and aerospace systems. The technical program will consist of oral technical presentations as well as industrial exhibits. The conference will be held at the NASA Goddard Space Flight Center in Greenbelt, Maryland.

Presentations will be in all aspects of the use of programmable elements, devices, and applications for military and aerospace applications. These include: PALs, FPGAs, PROMs, Programmable Substrates, FPIC, Programmable Analog Circuits, adaptive computing systems and related technologies. All presentations are expected to be technical in nature. Each presentation will be twenty-five minutes. Conference proceedings will be published and distributed to all attendees.

Topics include (but are not limited to) the following:

- Programmable Technologies and State-of-the-Art Devices
  - COTS and MIL/AERO
  - New Technology Development
  - Adaptive Computing Systems
- Radiation Effects, Device Reliability and Element Characteristics
- Device Architecture, Performance, and Capabilities
- Applications and Novel Techniques for Military and Spaceflight Circuits.
  - Signal Processing
  - High-Speed Designs
  - System Impact of State-of-the-Art Technologies
  - Reconfigurable Processing
  - Low Power Designs
  - Advanced Packaging
- Use of COTS Devices in the Military and Spaceflight Environment
  - PEMS
  - Shielding, Latchup Protection
  - SEE including SEFI and Destructive Effects
  - System Protection
  - Testing and Analysis Techniques
  - Performance Results
  - Use of Programmables in Critical Systems
  - Software Tools for Design/Analysis
    - Synthesis
    - Macro Generators
    - Timing Analysis and Simulation
    - Redundancy, Fault Tolerance, and SEU-Hardening

PRELIMINARY CONFERENCE SCHEDULE

September 14
NASA/GSFC Tours, and early registration at the GSFC Visitor Center, Soil Conservation Road.

September 15 and 16
In addition to over twenty presentations, keynote speakers are Dennis Andrucyk of the Goddard Space Flight Center who will address "Achieving the Earth Science Vision"; John Birkner, Vice President and Cofounder of Quicklogic Corporation, addressing "From Simple PALs to High-Speed, High Density Leading Edge FPGAs, their Technologies and Applications"; Janet Barth of the Goddard Space Flight Center providing "An Overview of the Radiation Environment for Spaceflight Electronics"; and Jose

Munoz addressing "DARPA's Adaptive Computing Systems (ACS) Program."

A Posterboard session will be held Tuesday evening for additional presentations.

The conference is sponsored by (preliminary list): NASA/GSFC, JHU/Applied Physics Laboratory, and the NASA Radiation Effects Program.

For event schedules, a list of presentations, and more information on the conference please see http://rk.gsfc.nasa.gov/richcontent/Ksymposium/kSymposium.htm

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Challenges of Implementing CSP Technology

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Availability of board solder joint reliability information is critical to the wider implementation of Chip Scale Packages (CSPs). CSPs are defined as packages that are up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Many manufacturers now refer to CSP as the package that is a miniaturized version of the previous generation.

A consortium was formed from the team members of the original JPL-led BGA consortium and new members added with experience in this technology. All participants have furnished in-kind contributions by providing their expertise and resources required to complete the objectives of the program. Diverse participants, including those from military and commercial sectors permitted implementation of the objectives of the program in a concurrent engineering environment.

In the process of building the first test vehicle of CSPs, many challenges were identified regarding various aspects of technology implementation. Key challenges are summarized as follows:

Maturity and availability – Availability of CSPs for use and attachment reliability evaluation is the most challenging issue. There are numerous publications on a wide range of CSPs, but most packages are at their early stages of development and lack package reliability data. Assembly reliability data are rare. Most packages were available in prototype form and this does not guarantee the uniform package characteristics for the production version or even their availability. Delay on package delivery from the projected time is the norm.

Lack of Design Guideline Standards– Currently, guidelines and standards on various elements of CSPs are not available. For our design, guidelines developed by the package suppliers were used when available. Otherwise, available knowledge and engineering judgment were considered. Packages chosen

had different pitches, solder ball volumes, solder ball compositions, and daisy chain patterns. In most cases, these patterns were irregular and much time and effort was required for design. This was especially cumbersome for packages with higher I/Os and many daisy chain mazes. Board design guidelines are needed, especially for the build up (microvia) configuration.

PWB Materials – The standard PWB design could be used for low I/O CSPs. Our test vehicle included several of these packages with the objective of characterizing assembly reliability when conventional PWB design was used. Higher I/O packages with active dies require the use of buildup (microvia) board technology. For testing purposes, however, it was possible to design high I/O daisy chain packages on a standard board. Another version of our test vehicle included a PWB with microvia technology.

Applications – There were a number of packages from low I/O (<50) to higher I/Os selected for characterization. It became apparent that for the near future, 1-3 years, the dominant packages would be those with less than 50 I/Os. Specific application requirements could utilize packages with much higher I/Os. Mixture of conventional SM packages, direct chip attachment, BGAs, and CSPs on one board is another expected design and assembly challenge.

TEST VEHICLE DESIGN

The consortium agreed to concentrate on the following aspects of CSP technology after numerous workshops, meetings, and weekly teleconferences.

Package – Numerous packages from leaded and leadless to micro type ball grid arrays were selected for evaluation. I/Os ranged from 40 to 300 to meet the short and longer term applications.

PWB Materials and Build – Both FR-4 and BT (Bismaleimide Triazine) materials were available in the resin copper coated form for evaluation. Both standard and microvia board technologies were used. In design of daisy chains, it became apparent that the standard PWB technology could not be used for the majority of packages.

Surface finish – At least three types of surface finishes are being considered for evaluation: OSP, HASL, and Au/Ni. Other surface finishes are also being considered. Three types of solder pastes will be evaluated: no clean, water soluble and RMA.

Underfill – Packages with underfill requirements will be evaluated both with and without underfill to better understand the reliability consequence of not using underfill.

Test vehicle feature – The test vehicle is 4.5 by 4.5 inches and divided into four independent regions. Each region has four daisy chains and can be cut for failure analysis without affecting the daisy chains of other regions. All packages are daisy chained and have up to two internal chain patterns.

Environmental testing – At least three conditions will be considered; -30 to 100°C and -55 to 125°C, to link our data to those generated for the Ball Grid Arrays. Also, thermal cycling will be performed between 0 and 100°C to meet the needs of commercial team members. In addition, mechanical vibration and shock will be performed and theoretical modeling will be carried out as needed.

STATUS OF THE MICROTYPEBGA PROGRAM

The consortium has completed the design of two test vehicles: one from collective team effort (TV-1) and the other initiated internally by a team member (TV-H). The trial assembly of the TV-H is now complete. These assemblies were evaluated and the required changes were implemented for full production assembly. The only remaining challenge is the process optimization for a flip chip package. Flip chips with and without bridges were built. One possible reason for bridging was the lack of solder mask between the pads. The solder mask was not feasible to apply because of the fine pitch pattern.

The TV-1 trial boards were built to optimize the assembly processes and to verify continuity of daisy chains. The consortium is currently assembling the full production test vehicles. We will assemble nearly 300 test vehicles with CSP I/Os from 40 to 300.

ACKNOWLEDGMENTS

The research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

I would like to Acknowledge in-kind contribution and cooperative efforts of MicrotypeBGA consortium team members and those who have been contributing to the progress of the program.

COTS Effort at JPL & Launch of a COTS Website

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As JPL moves toward the new millenium, new commercial technologies and microelectronics will be used more and more to help meet mission constraints and requirements and in consort with a faster, better, cheaper environment within NASA. Commercial microelectronics (parts) offer some advantages such as reduced weight with plastic packaging, more performance with advanced processes and designs, and an assortment of integrated functions only available as commercial off-the-shelf (COTS) parts.

Using COTS in space successfully requires complete understanding of the product's capabilities and limitations under a space environment. Since COTS by definition are not designed to operate in Space, there may be serious or compromising factors that could jeopardize mission success if not understood. Although, there are some situations where COTS can be used satisfactorily provided all potential risks are known or can be mitigated.

Office 507 has undertaken an initiative to evaluate and explore the issues regarding the use of COTS parts in Space. In addition, Office 507 can help JPL projects in ascertaining the suitability of COTS in their applications. This is accomplished by utilizing characterization, reliability evaluation, and risk assessment. The use of COTS in Space applications is increasing and making a prominent presence, including in the military and aerospace industries. To stay abreast with the developments in COTS parts, Office 507 has developed a web site to disseminate information on COTS that will help users in evaluating, ascertaining risk, or selecting parts for their applications.

The web site has technical reports, presentations, data, and news related to COTS work completed by the electronic parts engineering group and others.

This new web site called "COTS Microelectronics in Space" can be found at: http://cots.jpl.nasa.gov/.

As always, comments are welcome. Check on the "access" button on the home page for information.

Low Power Evaluation of COTS 4Meg SRAMs for Space Applications

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An evaluation was performed under the auspices of JPL Office 507 LPSEP (Low Power Space Electronic Parts) task whose objective is to identify flight worthy 3.3V state-of-art devices. 5V commercial 4-megabit static random access memories (4Meg SRAMs) from Sony, Hitachi and Motorola which were characterized for operation at 3.3V. This work was done in collaboration with Space Electronics, Inc. (SEI). Based on the test results and the fact that they already sell a 5V radiation tolerant 4Meg SRAM with Hitachi die, SEI has offered to make a 3.3V Hitachi version for the space community.

For a copy of the report, go to JPL COTS website (http://cots.jpl.nasa.gov)and look under reports.

Evaluation of ESD Effects During Removal of Conformal Coatings Using Micro Abrasive Blasting

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The following is an abstract of a paper published and presented at the IPC Printed Circuits Expo'98 held in Long Beach, California on April 26-30, 1998.

ABSTRACT

Recent environmental regulations such as Montreal Protocol and Clean Air Act have had a significant impact on Coating Technology including equipment, materials, application and removal processes, particularly with regard to control of volatile organic compounds (VOCs) and ozone depleting chemicals (ODCs). Manufacturers and suppliers of conformal coatings materials have been developing non-solvent based coatings and environmentally acceptable methods of application, curing and removal processes.

The most commonly used methods for removal of polymeric coatings from printed wiring assemblies (PWAs) involve thermal, chemical, mechanical, micro abrasive, plasma and laser based systems and processes. The need for rework or repair of a conformal coating can arise at any time after completion of an assembly due to a variety of process / product requirements or component replacement issues.

NASA's objective is to determine the effectiveness of micro abrasive blasting techniques to remove conformal coatings from printed circuit boards (PCBs) and assemblies. Micro abrasive systems generate static electricity as the high velocity particles impinge on the PWB surface. The ESD voltage generated at the point of contact can cause damage to components and electrical circuits on a PWA.

This paper presents the preliminary results of NASA study on the level of ESD damage at the point of contact and any visible physical damage as a result of micro blasting during removal of urethane and parylene conformal coatings. The final study is expected to be completed by FY 1999.

The Rational Use of Plastic Parts in Satellites

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Key Words -- Commercial Off The Shelf (COTS), Handling, Plastic Encapsulated Microcircuit (PEM), Qualification, Screening

Summary & Conclusions --Management of plastic encapsulated microcircuits begins and ends with a concurrent engineering effort. The effort begins with the establishment of partnerships with a handful of world-class suppliers and ends with the development, documentation, and enforcement of rigorous in-house controls regarding device handling, screening, qualification, uprating, derating and storage.

The Johns Hopkins University Applied Physics Laboratory (JHU / APL) has successfully selected screened and qualified PEMs for multiple artificial satellite applications. We discuss the rationale on how these commercial devices can be properly qualified and applied.

1. INTRODUCTION

Trends in the marketplace for smaller, more cost effective, state-of-the-art technologies are rapidly forcing obsolescence and leading to decreased availability of military-grade hermetically sealed electronic components. PEMs, once a non-alternative for space flight applications, have become a necessity. Predominant factors to consider such as vendor selection, environmental considerations, procurement, handling, screening and qualification strategies with associated systems implications are presented. The Thermosphere- Ionosphere - Mesosphere - Ener-

getics and Dynamics Program (TIMED) is used to describe the JHU/APL approach.

TIMED Program

The TIMED Program is the first mission in the National Aeronautics and Space Administration's (NASA) Solar Connections Program. TIMED will explore the Earth's mesosphere and lower thermosphere in the 60km - 180km range. TIMED has a 3 year development cycle, followed by a 2 year mission life; launch is expected in January 2000. Key technical accomplishments for TIMED include: 2GB solid-state recorder, radiation-hardened 32-bit RISC processor, redundant MIL-STD-1553 data bus, and the integrated command, telemetry, radio-frequency communications, global positioning system and data storage module.

To accomplish the TIMED mission objectives, it was necessary to successfully balance the *risks* associated with using commercial technology against the *need* for space-level component reliability. For example, high-density commercial memory devices were the enabling technology that allowed the development of the TIMED 2GB solid-state recorder. While suitable PEMs were found for TIMED, it may not be possible to find PEMs that are useable for every high-reliability application. It is expected that this will change over time as the risks associated with PEM usage are fully understood.

Looking more specifically at TIMED, **Table 1** provides a breakdown of the electrical, electronic, and electromechanical (EEE) parts that comprise the TIMED spacecraft. The numbers are representative of unique line items, whereas, multiple occurrences of a device is not shown. Definitions for the column headings are as follows:

Military: All military specifications, /883, QML, DESC-SMD and NASA specifications

SCD: JHU/APL source control drawings (SCD), purchase order line-item requirements, manufacturer's internal hi-rel flow

PEM: A PEM is a COT which has a plastic package. A PEM can be a microcircuit, semiconductor, passive component, or otherwise.

COTS: Any commercially developed component.

Table 1. TIMED Parts Breakdown. COTS represent 16% of the total line items used on the TIMED Program.

	Military	SCD	PEM	COTS
Capacitor	124	1		3
Connector	38	31		47
Diode	27	1		3
Int-Ckt	134	11	8	4
Magnetics	8			11
Oscillator	4	4		4
Relay	2	6		
Resistor	321	21	7	24
RF-Devices	4	19		24
Transistor	12	4	1	3
Miscellaneous	34	21		15
Totals	708	119	16	138

2. PEM SELECTION CRITERIA

JHU/APL utilizes a four-tiered approach to part selection: Concurrent engineering; evaluation of each part for its intended application; partnership with world-class suppliers; and review of manufacturer's reliability data.

An effective parts management program begins with a **concurrent engineering** effort. Key team players from the following disciplines are required: Design, Manufacturing, Component Reliability, Logistics and Purchasing. It is the responsibility of the team to **evaluate** each part selected for its **intended application**. It is important to realize that a PEM which is suitable and qualified for a particular application on a spacecraft, may be completely unusable in another application on the same spacecraft! This simple concept is often overlooked by the traditionalist who is accustomed to approving a part solely on the basis of its *military designation* and not its intended application.

To help simplify the selection process, efforts are made to form **partnerships** with only a select handful of **world-class suppliers**. The rationale behind limiting vendor selection is founded in a variety of reasons. First, limiting the number of vendors ultimately reduces the number of parts that have to be evaluated by the engineering team. Secondly, it facilitates the working relationship between JHU/APL and the manufacturer. Having good and reliable

contacts is crucial to overcoming the service aspects of being identified as a *small volume customer*. This ties into the third reason, JHU / APL needs access to **manufacturers' reliability reports** and technical staff. The TIMED program has very specific guidelines regarding vendor selection and PEM reliability that need to be met. As such, the adequacy of a given manufacturer's reliability report ultimately becomes the basis for acceptance, as well as the foundation for the screening and qualification regime employed by JHU / APL.

3. PEM HANDLING ISSUES

As with PEM selection, JHU / APL employs a four-tiered approach to handling: Use of finger cots and / or gloves; moisture protection; conformal coating; and adherence to ElectroStatic Discharge (ESD) sensitivity practices and procedures.

The rationale for taking such precautions is *corrosion avoidance.* For galvanic corrosion to occur in PEMs, the following elements are necessary: *a bimetallic couple*, most often gold-aluminum, present in the gold bond wire to the aluminum metallization pad; *free mobile ionic contamination*, usually chlorine, potassium, bromine, and / or sodium; and *moisture*, diffused from the atmosphere, to form an electrolyte [1].

We can identify two sources of ionic contamination: Traditionally, the encapsulant material was the main source of ionic contamination internal to the PEM. However, the present generations of molding compounds are considered ion-free since the typical ionic residue level in today's parts is less than 10 part per million (ppm) [2]. The second potential source is incidental contamination, external to the PEM. This contamination can be from sources such as the atmosphere, human handling, and cleaning agents.

The ionic transport of incidental ionic contamination to the die surface is still the subject of intense debate. The addition of up to 80% silicon fillers to produce the epoxy novolac encapsulant used today in most PEMs allows for limited ionic mobility. The encapsulant material manufacturers reacted to this limited ionic mobility by adding an *ion-getter*, or *scavenger*. The incorporation of alkali- and halide-ion gettering agents into the epoxy-molding compound makes migrating ions in the epoxy unavailable for dissolution into any diffused or accumulated water in the package [3]. The diffusion of ionic contaminants through epoxy-novolac encapsulant is presented in the next section.

The Case for Finger Cots and Gloves

The case for finger cots and / or gloves is a strong one. **Figure 1** depicts data from a recent University of Maryland CALCE Electronic Packaging Resource Source Center study. The study has demonstrated that the rate of ionic diffusion through the encapsulant is a function of the ionic concentration, the epoxy novolac formulation, and the additives in the epoxy-novolac [4]. This study was conducted by separating two cavities with a slice of epoxy novolac; CALCE personnel filled one cavity with distilled water and

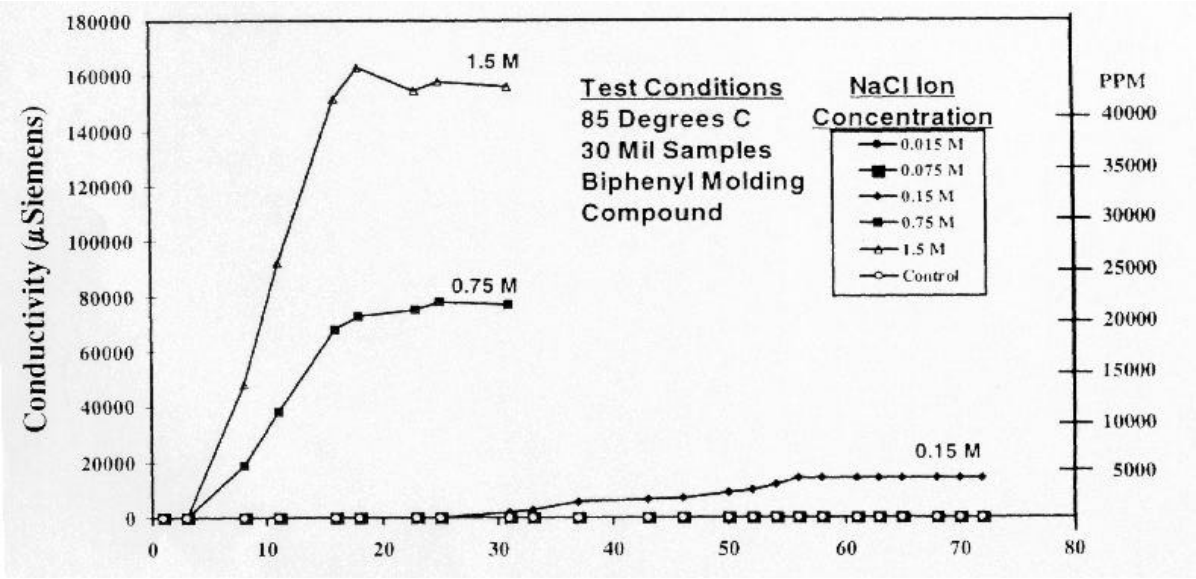

Figure 1. Effect of Concentration on Ion Diffusion. No diffusion occurs for several days

the other with a solution of ionic contaminants. They evaluated various combinations of ionic species, concentrations, temperatures, and epoxy formulations. The diffusion rate of ionic species throughout the epoxy was measured by sampling the distilled water and analyzing it.

Two points can be gleaned from the graph presented. First, since the diffusion rate is directly related to ion concentration, it becomes necessary to limit the introduction of any external contaminants, thus justifying the use of finger cots and/or gloves. Secondly, the use of ion-getters impedes the diffusion of ions. Unfortunately, it can be seen that these ion-getters are a *limited* resource. From **Figure 1**, after approximately 18 days the ion getters were completely exhausted and the solutions reached equilibrium.

What is truly frightening is that the University of Maryland study was based on epoxy novolac slices of approximately 30 mils. How much time does a device have, such as **Figure 2**, where only approximately 6 mils of separation exist between the PEM surface and the bond wires? Hours may pass, not days, before ionic contamination could travel along the bond wire to the surface of the die under similar conditions. The authors anticipate a much slower ionic diffusion rate for PEMs under normal usage because the moisture available will be limited and far less than 100% saturated as in the CALCE study.

Figure 2. Samsung 32MB Flash Static Random Access Memory (SRAM). Note the close proximity of the bond-wire loop to the top surface of PEM.

The Need for Moisture Protection

Moisture protection techniques are required for two distinct reasons: First, to alleviate any potential "popcorning" of PEMs during the fabrication process, and secondly, in general, to combat corrosion. JHU/APL's approach to controlling moisture involves timely *bake-out* of components, environmentally controlled storage areas, and the use of *dry boxes*.

In terms of popcorning prevention, devices undergo a bake-out for 24 hours at +125°C at the conclusion of all incoming inspections. However, some parts may not be baked at +125°C due to solderability and lead finish concerns. Alternative methods, such as vacuum bakes at lower temperatures may be used. Then, all parts are individually vacuum sealed in dry-nitrogen purged bags prior to placement in flight stores. Once the dry-bag is opened, the part has a limited time duration to be soldered before it must be baked-out again. The actual time allotted (out-of-bag-time) varies for each part and is a function of the moisture sensitivity level ascribed to it in accordance with Interconnections Packaging Circuitry Standard IPC-SM-786A.

In regards to combating corrosion, we have already explained how finger cots and/or gloves can be effective in reducing external contaminants. However, since it is not possible to eliminate all sources of ionic contaminants additional prevention techniques must be employed. The focus of these techniques is centered upon moisture avoidance.

From discussion above, moisture serves as the transport vehicle which allows ionic contamination to reach surface of the die. The simplest methods used to minimize the moisture ingress have already been discussed under popcorn prevention: use of dry-nitrogen purged bags and bake-out of PEMs. However, it is not sufficient to rely solely on a dry-bag for protection. Cleanliness and moisture avoidance are conjoined. A JHU/APL study has demonstrated that dry-bags serve only as barriers to moisture, not air [5]. Data from the study shows noticeable air-exchange occurring within a one week period and complete air exchange occurring within a month's time. To assure cleanliness, it is necessary to maintain parts in environmentally controlled storage areas or dry-boxes until needed. The dry-boxes can be

used, as long as it is practical, during piece-part testing, during board fabrication, and prior to and after conformal coating [6]. In fact, entire printed circuit board assemblies can be placed in the dry-box.

The Need for Conformal Coating

JHU/APL has performed numerous studies, reviewed industry data, and continues to conduct studies in the area of *long term dormant storage*. The results of these studies evidence to the fact that *delamination* may be present in the "as-received" condition of devices directly from the manufacturer.

While it is true that differing opinions exist regarding the validity and concerns placed on delamination, until definitive answers can be ascertained JHU/APL will continue to take a very conservative approach. When a PEM exhibits large delaminations we assume that these are a path for moisture and contaminants to reach the surface of the die by traversing along the lead frame and bond wires. Therefore, we need conformal coating to seal this path. Conformal coating is known for increasing the reliability of assemblies containing PEMs [7]. Since conformal coating will not prevent moisture diffusion entirely (only slow it down), we speculate that it will preserve ion getters by filtering out some ionic species. The specific conformal coating recommended by JHU/APL is Parylene. The choice of Parylene is based on a study conducted for the JHU/APL managed Full Signal Translator (FST) program, as well as other industry data [7]. The FST study involved subjecting three groups of parts simultaneously to Steady State Temperature Humidity Bias Life Testing (85/85). The three categories of parts were: uncoated PEMs; PEMs with Urelane conformal coating; and PEMs with Parylene conformal coating. After 500-hour 85/85, only the Parylene coated parts were functional.

In addition, a recent *chip-on-board* (COB) study, also conducted by JHU/APL, has validated the recommendation for Parylene. The COB study demonstrated that a Parylene/epoxy combination was effective in protecting unpassivated Sandia National Laboratory "Triple-Track" die during 1,000-hour 85/85 [8].

As with any good thing, there are always some drawbacks. Several associated usage issues need to be addressed regarding Parylene. First, Parylene requires a vacuum deposition process. As such, access to appropriate equipment is required. In addition, the effects of the vacuum deposition process on non-hermetically sealed or vented components is not fully understood. It therefore becomes necessary to mask-off certain devices and interconnect pads of the board. Secondly, rework becomes difficult once a device is coated with Parylene. Either mechanical stripping or localized heating can be used to remove a device. Both of these approaches can lead to *cosmetic scarring* of the printed wiring board (PWB) assembly. In efforts to minimize PWB damage, NASA Goddard Space Flight Center is currently investigating an alternate method that involves a "fine-nozzle" sand-blaster with ionizers to offset ESD concerns.

ESD Practices and Procedures

The final topic to be discussed under PEM handling has to do with ESD awareness. ESD is an issue independent of PEM usage. It is prudent practice to handle *all* components in such a manner as to avoid ESD damage. JHU/APL has an established ESD program that conforms to MIL-STD-1686, "Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment." In addition, local ionizers are recommended to further dissipate electrostatic charges.

4. PEM SCREENING

For the TIMED program, individual piece part testing involves electrical verification (at the mission temperature profile), radiographic inspection, and visual & mechanical inspection. With the exception of mechanical inspection, all screening tests are performed on a 100% basis.

Electrical Verification

Most PEMs do not meet standard military temperature range (i.e., -55°C to +125°C). This should not be viewed as an immediate cause for concern, but a risk to be mitigated. The process which is used to reduce the risk involved in using components and/or systems outside the manufacturer's temperature specifications has been termed by the University of Maryland CALCE, as *uprating* [9].

What is most important is for the PEM in question to meet the appropriate **mission temperature profile.** In most instances the most severe temperature

extremes occur during ground based testing, not during actual flight. For TIMED, the most severe environment occurs during spacecraft thermal vacuum testing, -40°C to +100°C; actual component temperatures during flight are not expected to exceed +5°C to +50°C.

It is not JHU/APL's intention to automatically use a part outside its intended manufacturer's temperature rating in a flight application. In fact, JHU/APL *derates* components to minimize the occurrence of this possibility. Derating is defined as a process in which device voltage, current and power are reduced by a certain percentage to extend longevity. However, if no alternative part can serve, it becomes necessary to assure that part can function at the temperature profile required.

The choice to uprate comes with various legal consequences. Manufacturers have advocated that using a part outside its intended temperature range will automatically invalidate any implied warranty. There may be even more serious legal repercussions, including the possibility of defamation lawsuits.

To assure a part will function reliably in the intended flight application JHU/APL performs 100% electrical verification at the mission temperature profile extremes. Since little power is dissipated during electrical tests, the device integrity is not compromised. In addition, sample parts are subjected to a selected set of qualification tests. Determination of specific tests to perform is based upon detailed analysis of the manufacturer's reliability data. The purpose of qualification testing is to compliment what has already been accomplished by the manufacturer. Ramifications associated with qualification testing will be discussed in more detail under **Section 5**.

Radiographic Examination

Radiographic examination (X-ray) is performed, on a 100% basis, in accordance with MIL-STD-883, Method 2012, "Radiography." JHU/APL recommends and uses *real-time* X-ray to obtain beneficial results. Unlike film, real-time X-ray provides high resolution images in various planes by rotating the devices inside the chamber. This enables the PEMs user to develop a three-dimensional abstraction of the device internal construction. **Figure 3** provides an excellent view of the results obtained using the real-time technique. The photograph is representative of a Samsung 64MB Dynamic Random Access Memory (DRAM). This DRAM is the integral part of the TIMED solid-state recorders. **Figure 2** also emphasizes the superior capabilities of real-time X-ray.

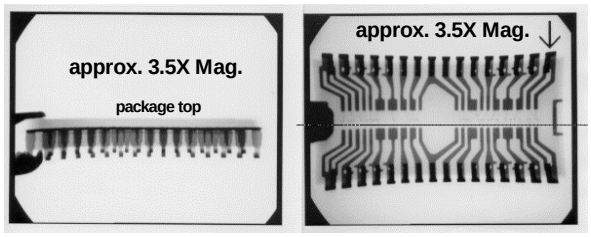

Figure 3. Real-Time X-ray of Samsung 64MB DRAM. From "Top View," the die occupies a proximately 90 percent of the package, with the lead frame on the top.

Performance of X-ray should not be viewed in the context of *pass/fail* criteria attributed to lot rejection. Rather, the purpose of performing the examination is to gain knowledge regarding overall device construction. Information learned serves as an invaluable aid toward device decapsulation; a process necessary to accomplish Single Event Upset (SEU) testing and/or failure analysis. Additional information regarding SEU testing can be found in **Section 5**.

Visual & Mechanical Inspection

Visual inspection is performed, on a 100% basis, in accordance to the nearest applicable standard (i.e., military, JEDEC, best commercial practices, etc.). Mechanical inspection is performed, on a sample basis, in accordance to the same. The intent of these inspections is to ensure device compliance to purchase order requirements.

5. PEM QUALIFICATION

JHU/APL approach to PEM qualification is centered around a five-tiered testing regime: radiation hardness assurance, temperature cycling, steady-state temperature humidity bias life test, destructive physical analysis, and high temperature operating life. For reasons that will be outlined below, all testing performed is considered to be *destructive* in nature. The selected regime is designed to qualify PEMs for all its mission environments, including

integration, test, storage, transportation, launch, and mission life.

Radiation Hardness Assurance (RHA)
All parts, commercial and/or military must be evaluated for RHA. When required, testing is performed in accordance with MIL-STD-883, Method 5005, "Qualification and Quality Conformance Procedures," Group E, or equivalent.

It has been the experience of JHU/APL that total dose is not the main cause for concern for RHA. The majority of parts chosen either meet the low total dose requirements associated with the TIMED mission, or can be adequately shielded against such effects. The primary issue associated with RHA, for any part, is SEU immunity. For PEMs, SEU testing can be cause for concern. Specifically, in question, is the ability to decapsulate the PEM in order to perform the SEU test. PEM decapsulation will be covered in more detail under *Destructive Physical Analysis*, below.

One final thought in regards to RHA, it is necessary to compensate for the affects of burn-in. Data presented by Shaneyfelt, Winokur, Fleetwood, Hash, Schwank & Sexton, has demonstrated that burn-in may affect radiation results [10]. As a result, parts used for RHA testing *must* resemble those in the flight configuration. If 100% burn-in was performed as a screen, it becomes necessary to ensure parts chosen for RHA are burned-in equally.

Temperature Cycling (T/C)
The purpose of performing T/C is to cull potential coefficient of thermal expansion (C_{TE}) mismatch concerns. T/C testing can induce or exacerbate delamination, aiding corrosion by creating pathways for moisture ingress. Mitigating against the effects of delamination justifies the need to conformally coat PWBs, as outlined above in **Section 4.**

When T/C testing is performed, JHU/APL follows the guidelines established in Joint Electron Device Engineering Council (JEDEC) Standard JESD-22-A104, "Temperature Cycling." After the completion of T/C testing, final electrical measurements at the mission temperature extremes (e.g., cold, room, & hot) is performed. Finally, selected T/C samples are subjected to DPA.

As an alternative to *preconditioning*, all parts used for T/C testing are assembled onto flight-like boards (e.g., same materials & manufacturer as flight boards) and conformally coated prior to conducting the T/C test. Preconditioning, as defined by JEDEC Standard A113-A, "Preconditioning of Plastic Surface Mount Devices Prior to Reliability Testing," aids in the evaluation of long term part reliability by taking into account the impact of multiple solder reflow operations. JHU/APL's approach of assembling PEMs onto flight-like boards and conformally coating them prior to test qualifies the intended flight application.

T/C testing is performed as a result of reviewing the manufacturer's reliability data.

Steady-State Temperature Humidity Bias Life Test (85/85)
The purpose behind performing 85/85 testing is to assure that parts can survive in the uncontrolled moisture laden environment prior to launch. Specifically, variances in moisture and temperature during integration, test, transportation and storage of the spacecraft.

Once in the vacuum of space, moisture becomes a non-issue; moisture is immediately depleted upon entering the vacuum environment. Protecting the devices while still on the ground requires the maintenance of a "moisture-free" environment. As already stated, JHU/APL uses both dry-boxes and conformal coating to minimize moisture. Dry-boxes, by their very nature, are moisture free. Conformal coating will not stop water, but it will slow it down and filter it.

When 85/85 testing is performed, JHU/APL follows the guidelines established in JEDEC Standard JESD-22-A101, "Steady-State Temperature Humidity Bias Life Test." Testing is done in a manner consistent with that of T/C testing. The parts are assembled onto flight-like boards and conformally coated prior to conducting the test. After completion of testing, three temperature final electrical measurements are taken and selected samples are subjected to DPA.

85/85 testing is performed as a result of reviewing the manufacturer's reliability data.

Destructive Physical Analysis (DPA)
As with radiographic inspection, above (**Section 4**), the purpose of conducting DPA is to build a knowledge base of component construction technology. Special attention is given to the effects of T/C and 85/85 testing on PEM reliability. It is hoped that observations and measurements made during DPA will aid in the establishment of uniform pass/fail criteria associated with scanning acoustic microscopy results (delaminations).

When DPA is performed, JHU/APL follows the guidelines established in MIL-STD-1580, "Destructive Physical Analysis for Electronic, Electromagnetic, and Electromechanical Parts," as applicable.

To further understand delamination phenomena, all samples are subjected to C-mode scanning acoustic microscopy (C-SAM) prior to decapsulation. This topic will be discussed in more detail under **Section 6** (reference U.S. Army Missile Command Study).

Currently JHU/APL utilizes three decapsulation methods: *oxygen plasma* etching; wet etching with either *red fuming nitric* and/or *red fuming sulfuric acid*; and *thermo-mechanical* means including grinding, heating, and breaking of the plastic encapsulation by force. Each method has associated advantages and drawbacks. Final selection of a particular method is dependant upon the end-results desired (e.g., functionality, access to internal structures, etc.).

High Temperature Operating Life (HTOL)
Burn-in is only performed as part of qualification testing on a sample size basis. The first and fore most reason for performing burn-in during qualification has to do with time. Applying the Arrhenius equation, with an assumed activation energy of 0.7 V, a standard burn-in of 168 hours, at +125°C, extrapolated to +70°C, would require 3,272 hours to complete! Another reason for performing burn-in as a qualification test has to do with temperature. As already stated, the majority of PEMs are not rated to +125°C.

From **Section 4**, it has been established that during TIMED spacecraft thermal vacuum testing some PEMs will exceed their data sheet temperature limits. As such, survivability of devices at these temperatures must be assured. The purpose of performing HTOL, therefore, is to provide justification for *uprating* of components.

When HTOL is performed, JHU/APL follows the guidelines established in JEDEC Standard JESD-22-A108, "Bias Life." Dynamic bias is preferred, but not mandatory. Sample size for HTOL is 22 pieces. The time and temperature used are 1,000 hours, and +125°C, respectively. Unlike T/C or 85/85 testing, there is no need for preconditioning or to conformally coat. HTOL is concerned with infant mortality and the long term reliability of devices to withstand temperature extremes. At the completion of testing, final electrical measurements are taken at three temperatures.

6. LONG-TERM DORMANT STORAGE

The qualification tests outlined in **Section 5,** above, concentrate solely on the individual effects of temperature and/or moisture on PEMs. Limited studies have been conducted on what has been classified as the *wooden-round* concept. The wooden-round concept is concerned with the *synergistic* effects of moisture and temperature on PEMs under uncontrolled long term dormant storage conditions.

JHU/APL has already completed one such study for the U.S. NAVY F/A-18 Program. A total of 92 PEMs were involved in this effort, with parts dated as early as 1967. The results of the investigation revealed that only two devices, both 28 years in age, exhibited evidence of corrosion, and that a total of 91% of parts were delaminated.

Recently, JHU/APL has been selected to be an independent assessor for the U.S. ARMY Missile Command (MICOM). The MICOM study involves 16 PEM lots, consisting of 10 manufacturers, for a total of 160 pieces per lot. Each lot will be split into three groups of 50 parts, with three control samples per group, and subjected to the testing outlined in **Figure 4**. The purpose of the study is to gain further knowledge of the synergistic effects of temperature cycling and moisture on PEMs as related to long term dormant storage issues. Of particular interest are the effects of these conditions in the presence of delaminations. The performance of C-SAM and DPA, both pre and post test, is done for this very reason.

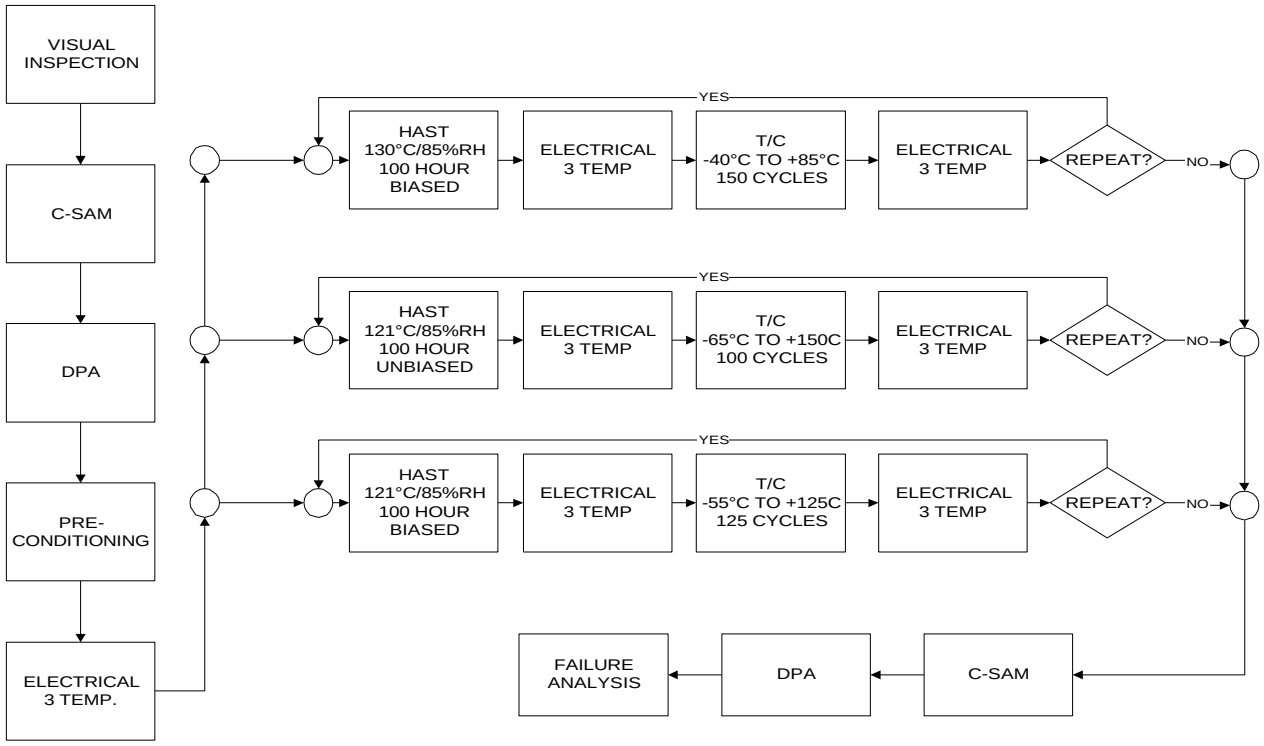

Figure 4. JHU/APL U.S. ARMY MICOM Study. Investigating the effects of multiple environmental stresses applied to PEMs.

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Programmable Logic Application Notes

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This column will be provided each quarter as a source for reliability, radiation results, NASA capabilities, and other information on programmable logic devices and related applications. This quarter's column will include some announcements and some recent radiation test results and evaluations of interest. Specifically, the following topics will be covered: the Military and Aerospace Applications of Programmable Devices and Technologies Conference to be held at GSFC in September, 1998, proton test results, heavy ion test results, and some total dose results.

MAPLD

Registration is now open for the Military and Aerospace Applications of Programmable Devices and Technologies Conference, to be held at NASA's Goddard Space Flight Center September 15-16, 1998. Late news poster papers are also being accepted. The program will consist of 4 invited talks, 4 technical sessions, a poster session, and an industrial exhibit. For registration and program information, including abstracts, please see http://rk.gsfc.nasa.gov.

NSREC '98

The 35th Annual Nuclear and Space Radiation Effects Conference was held in Newport Beach, California, July 20-24. Several papers were presented covering programmables and ASICs including: *Current Radiation Issues for Programmable Elements and Devices*, R. Katz, et. al., which gives an overview of state-of-the-art technology and their radiation characteristics, *Erasure of Floating Gates in the Natural Radiation Environments of Space*, P. McNulty, et. al., which discussed the floating gate technology, *Single Event Effect and Proton Damage Results for Candidate Spacecraft Electronics*, M. O'Bryan, et. al., which gives a broad overview of recent technologies, *Total Dose and Single Event Effects Testing of UTMC Commercial RadHard Gate Arrays*, D. Kerwin, et. al., showing radiation-hard performance, *High Total Dose Response of the UTMC Gate Array Fabricated at Lockheed-Martin Federal Systems*, J. Benedetto, et. al., showing the capability of the ASIC on the radiation-hardened line, *Total Ionizing Dose Effects on Flash Memories*, D. Nguyen, et. al., showing the effect of internal cell structures and charge pumps on radiation performance, *Anatomy of an In-flight Anomaly: Investigation of Proton-Induced SEE Test Results for Stacked IBM DRAMs*, K. LaBel, et. al., discusses test techniques for devices with small cross-sections, including the A1280A, etc., and *Neutron Single Event Upsets in SRAM-based FPGAs*, discusses the performance of an SRAM-based FPGA with neutrons.

MAPLUG

A military/aerospace programmable logic users group is being formed. The goal of the organization is, similar to other disciplines, promote sharing of

ideas, techniques, information, product announcements, alerts, and experiences between users of the technology, parts and reliability engineers, and vendors. Individuals and vendors may join by emailing: maplug@pop700.gsfc.nasa.gov. There will be no fee and no advertising. Membership lists will by default not be distributed as we wish to remain spam-free.

Proton Test Results from IUCF

A variety of FPGAs and a quick-turn ASIC was tested at the Indiana University Cyclotron Facility in June, 1998. All tests were run with ~ 193 MeV protons; the fluence varied according to the part type and test being performed. Devices tested were the RH1020, QL3025, A1280A/MEC, A54SX16 prototype (CSM), RT54SX16 prototype (MEC), and the QYH530 (Yamaha, two lots). The internal code name 'CKJ911' was used for the A54SX16 prototype in the test report.

Below are reports on each of the tests. These are available on-line at http://rk.gsfc.nasa.gov. Key results included good SEU performance of the 0.35 µm/3.3V devices from Actel and Quicklogic. Small cross-sections were measured for the RH1020 and the A1280A devices. No upsets were detected in the QYH530, operated at V_{CC} = 3.3VDC.

Total dose responses of the devices involved in this test was also measured, with I_{CC} vs. total dose curves given for many of the devices; tables are provided for some. There was reasonable agreement between the radiation response with protons and the Cobalt-60 radiation tests. No latchups, clock upsets, or configuration upsets were detected from SEU affects.

SUMMARY OF PROTON TEST ON THE ACTEL A1280A AT INDIANA UNIVERSITY JUNE, 1998

Prepared by: R. Katz, K. LaBel NASA/GSFC
Date: June 23, 1998

Test Facility

The Actel A1280A FPGA was tested at the Indiana University Cyclotron Facility (IUCF). The proton energy was 193 MeV and the flux was set at approximately 2 x 10^8 p/cm^2/sec. The total fluence for each device was determined by the total dose response of the device and it's affect on the current draw; details for each device including bias are given in the tables below. The device was irradiated normal to the beam.

Device Under Test

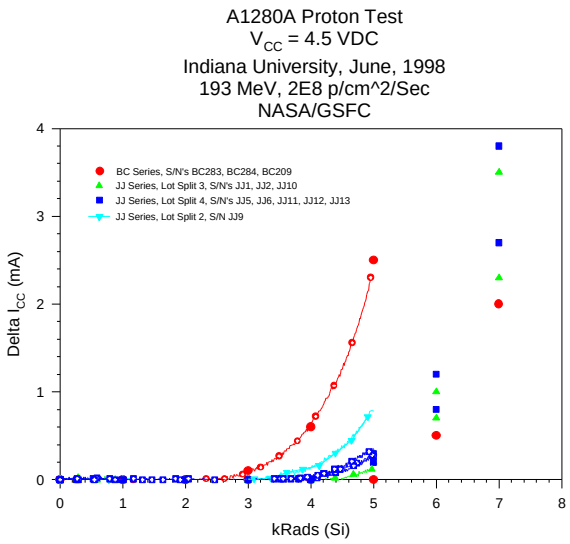
The A1280A devices were in a CPGA176 package and were active during irradiation. All die were from the Matsushita (MEC) foundry with a 1.0 µm feature size. Upsets and currents were monitored in real-time with the device being clocked at 1 MHz. The stimulation pattern was a 500 kHz square wave. The test pattern used, the TMRA2.C, contains 522 S-Module flip-flops and 40 C-Module flip-flops.

Sample devices were taken from several lots used previously in radiation tests along with a few 'spare devices' to increase sample size. A total of 19 devices were used in this study. The intent of the study was to investigate the proton response of the hard-wired S-Module flip-flops with a large sample size. Previous testing did not detect proton upset within the operating voltage range but used a low fluence.

TEST RESULTS

Nineteen devices were irradiated, with 12 devices at a worst-case bias of 4.5V and the remaining 7 devices at a nominal bias of 5.0V. An estimate of the cross-sections, by lot and bias, are given in Table 1 and Table 2, above. Previous tests of the A1280 (1.2 µm) and the A1280A (1.0 µm) did not detect proton upset. The large sample size for this study, with upsets detected in each device, shows that this device is sensitive to protons for S-Modules. No upsets were detected in the C-module flip-flops. However, there was a small number of flip-flops in this pattern so a different pattern should be used for measuring the C-module flip-flops' sensitivity to protons. Note that the C-module flip-flops in the RH1020, tested in June 1998, have a small, but non-zero cross-section for 193 MeV protons.

There was no clock upset detected in any of the devices. The device's total dose performance falls into the radiation-soft range, typical for devices of this class. The data within a lot was relatively consistent.



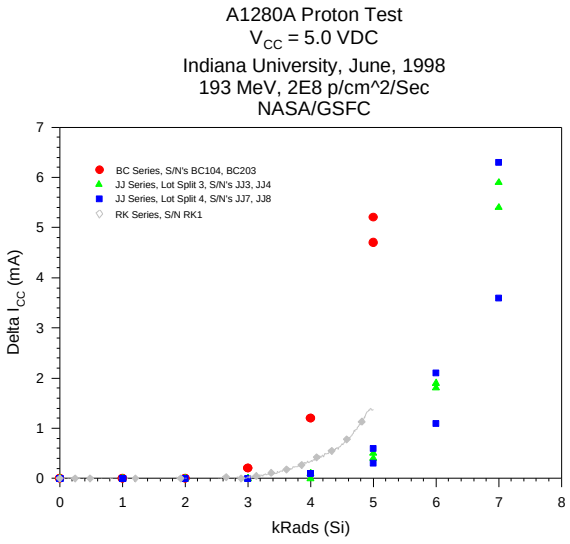


Table 1. Summary for V_{CC} = 4.5VDC.

S/N	Lot	Total Dose kRads (Si)	Upsets	Fluence (p/cm²)	Estimated Cross-Section (cm²/flip-flop) by Lot
BC284	9424	5	6	80 x 10^9	
BC283	9424	5	2	80 x 10^9	
BC209	9424	5	4	80 x 10^9	96 x 10^{-15}
JJ9	9614 Lot Split 2	5	5	80 x 10^9	120 x 10^{-15}
JJ1	9614 Lot Split 3	7	13	112 x 10^9	
JJ2	9614 Lot Split 3	7	7	112 x 10^9	
JJ10	9614 Lot Split 3	5	2	80 x 10^9	139 x 10^{-15}
JJ5	9614 Lot Split 4	7	9	112 x 10^9	
JJ6	9614 Lot Split 4	7	14	112 x 10^9	
JJ11	9614 Lot Split 4	5	6	80 x 10^9	165 x 10^{-15}
JJ12	9614 Lot Split 4	5	4	80 x 10^9	

Table 2. Summary for V_{CC} = 5.0VDC.

S/N	Lot	Total Dose kRads (Si)	Upsets	Fluence (p/cm²)	Estimated Cross-Section (cm²/flip-flop) by Lot
JJ3	9614 Lot Split 3	7	7	112 x 10^9	137 x 10^{-15}
JJ4	9614 Lot Split 3	7	9	112 x 10^9	
BC203	9424	5	5	80 x 10^9	83.8 x 10^{-15}
BC104	9424	5	2	80 x 10^9	
JJ7	9614 Lot Split 4	7	8	112 x 10^9	154 x 10^{-15}
JJ8	9614 Lot Split 4	7	10	112 x 10^9	
RK1	9415	5	4	80 x 10^9	95.8 x 10^{-15}

SUMMARY OF PROTON TEST ON THE ACTEL RH1020 AT INDIANA UNIVERSITY JUNE, 1998

Revision A.
Prepared by: R. Katz, NASA/GSFC
Date: June 18, 1998

Test Facility

The Actel RH1020 was tested at the Indiana University Cyclotron Facility (IUCF). The proton energy was 193 MeV and the flux was set at approximately 1 x 10^9 p/cm^2/sec. The total fluence for each device was 1.6 x 10^{12} p/cm^2 corresponding to a total dose of 100 kRads (Si); details for each device including bias are given in the tables below. The device was irradiated normal to the beam.

Device Under Test

The devices were in a CQFP84 package and were active during irradiation. Upsets and currents were monitored in real-time with the device being clocked at 1 MHz. The stimulation pattern was a 500 kHz square wave. Since the devices are quite hard to total dose effects, the test equipment was run in an SEU time-tagging mode to aid in the detection and instrumentation of clock upsets. The test pattern used, TMRA1BRB, contains 136 flip-flops with 102 in a TMR configuration and 34 in a shift register. The Act 1 architecture only has routed flip-flops; there are no hard-wired or I/O module flip-flops.

Sample devices were taken from two lots, a "pre-production" lot and a production lot. In this case, the difference between the devices were an improved clock buffer for 'clock upset' (production lot) and the thickness of the antifuses, with the production devices having a 90Å thick antifuse and the pre-production devices having a 96Å thick antifuse.

Test Results

The table included below summarizes the device, bias conditions, and irradiation.

Five devices were irradiated with a 5V bias and three with a 4.5 bias with a total of 3 upsets for all of the runs. The cross-sections can be estimated as 1.8 x 10^{-15} cm^2/flip-flop at V_{CC} = 5V and 1.5 x 10^{-15} cm^2/flip-flop at V_{CC} = 4.5VDC. Obviously, with the small error counts, the statistics are poor, and it would be expected that the device would have a larger cross-section at the lower bias level.

There was no evidence of any clock upset in either the pre-production devices or the hardened production lot.

The device's total dose performance was excellent, with changes of currents not exceeding more than a few hundred microamps. This also shows, as expected, no antifuse damage. Previous testing has shown that at LET = 37 MeV-cm^2/mg, a bias of 6.1 volts was necessary to rupture a production device (two samples tested). Note also that these devices had already been previously irradiated during heavy ion tests.

S/N	Lot	Bias (Volts)	Total Dose kRads (Si)	Upsets	Fluence (p/cm$_2$)
RH3	Production	5.0	100	0	1.6 x 10^{12}
RH4	Production	5.0	100	0	1.6 x 10^{12}
RH6	Production	5.0	100	2	1.6 x 10^{12}
RH1095	Pre-Production	4.5	100	0	1.6 x 10^{12}
RH1098	Pre-Production	4.5	100	1	1.6 x 10^{12}
RH1099	Pre-Production	5.0	100	0	1.6 x 10^{12}
RH1101	Pre-Production	5.0	100	0	1.6 x 10^{12}
RH3769	Pre-Production	4.5	100	0	1.6 x 10^{12}

SUMMARY OF PROTON TEST ON THE ACTEL CKJ911 PROTOTYPE AT INDIANA UNIVERSITY
JUNE, 1998

Prepared by: R. Katz, NASA/GSFC
Date: June 18, 1998

Test Facility

The Actel CKJ911 prototype FPGA was tested at the Indiana University Cyclotron Facility (IUCF). The proton energy was 193 MeV and the flux was set at approximately 1 x 10^9 p/cm^2/sec. The total fluence for each device was determined by the total dose response of the device and it's affect on the current draw; details for each device including bias are given in the chart below. The device was irradiated normal to the beam.

Device Under Test

The devices were in a PQFP208 package and were active during irradiation. Upsets and currents were monitored in real-time with

the device being clocked at 1 MHz. The stimulation pattern was a 500 kHz square wave. The test pattern used contains 400 flip-flops. The CKJ911 architecture only has hard-wired flip-flops with the available software; there are no I/O module flip-flops.

Sample devices were taken from a prototype lot, with I_{DDSB} currents higher than would be expected from a full-scale production lot. The "p-fuse" was not programmed on these devices and the TCK pin (an input to the IEEE 1149.1 JTAG TAP controller) was not active.

Test Results

The following table summarizes the device, bias conditions, and irradiations.

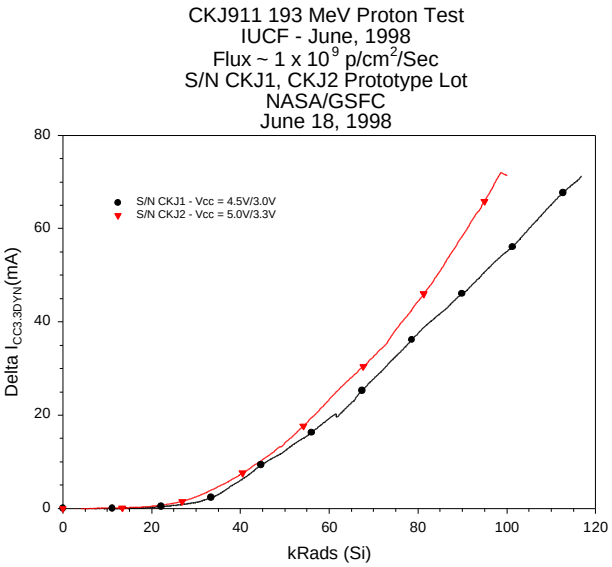
S/N	Lot	Bias (Volts)	Total Dose kRads (Si)	Upsets	Fluence (p/cm$_2$)
CKJ1	Prototype	4.5/3.0	116.9	2	1.9 x 10^{12}
CKJ2	Prototype	5.0/3.3	100.1	0	1.6 x 10^{12}

Two devices were irradiated, one with biases of 4.5V and 3.0V and the other with biases of 5.0V and 3.3V. An estimate of an upper bound for the cross-sections can be computed as 2.6 x 10^{-15} cm^2/flip-flop at the worst-case voltage and, assuming a single upset, as 1.6 x 10^{-15} cm^2/flip-flop at nominal supply voltages.

There was no clock upset detected in any of the devices and no upsets were detected in the JTAG TAP controller.

The device's total dose performance was good, despite the high initial device bias currents. The dose rate was high at 252 kRads (Si) / hour for S/N CKJ1 and 316 kRads (Si) / hour for S/N CKJ2. Details are shown in the strip charts below for the 3.3V supply currents.

Only moderate (< 250 µA) changes in the 5V bias currents were observed.



SUMMARY OF PROTON TEST ON THE ACTEL RT54SX16 PROTOTYPE AT INDIANA UNIVERSITY
JUNE, 1998

Prepared by: R. Katz, NASA/GSFC
Date: June 18, 1998

Test Facility

The Actel RT54SX16 prototype FPGA was tested at the Indiana University Cyclotron Facility (IUCF). The proton energy was 193 MeV and the flux was set at approximately 1 x 10^9 p/cm^2/sec. The total fluence for each device was determined by the total dose response of the device and it's affect on the current draw; details for each device including bias are given in the chart below. The device was irradiated normal to the beam.

Device Under Test

The devices were in a PQFP208 package and were active during irradiation. Upsets and currents were monitored in real-time with the device being clocked at 1 MHz. The stimulation pattern was a 500 kHz square wave. The test pattern used contains 400 flip-flops. The RT54SX16 architecture only has hard-wired flip-flops with the available software; there are no I/O module flip-flops.

Sample devices were taken from a prototype lot, and $I_{DDSTDBY}$ currents were normal, just a few hundred microamps. The "p-fuse" was programmed on these devices and the TCK pin (an input to the IEEE 1149.1 JTAG TAP controller) was not active for runs with S/N MKJ1 and MKJ2; it was active at 6 kHz for MKJ3. The date code was 9733 with the chip also marked as PO6GNC WFR #7,8.

Test Results

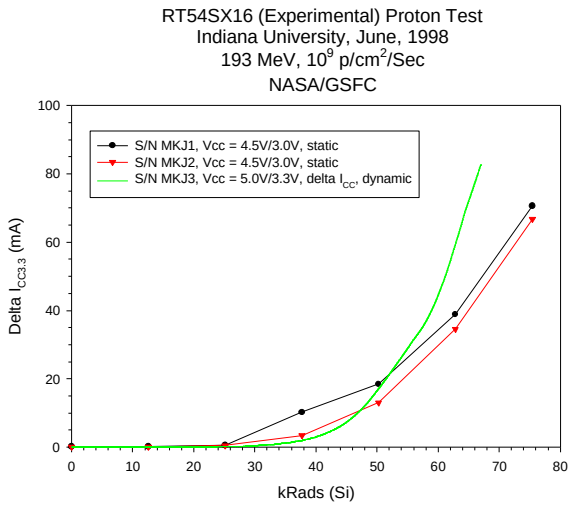
The following table summarizes the device, bias conditions, and irradiations.

S/N	Lot	TCK	Bias (Volts)	Total Dose kRads (Si)	Upsets	Fluence (p/cm²)
MKJ1	Prototype D/C 9733	Off	4.5/3.0	75.4	2	1.2×10^{12}
MKJ2	Prototype D/C 9733	Off	4.5/3.0	75.4	4	1.2×10^{12}
MKJ3	Prototype D/C 9733	6 kHz	5.0/3.3	103.1	2	1.6×10^{12}

Three devices were irradiated, two with worst-case biases of 4.5V and 3.0V and the other with a nominal biases of 5.0V and 3.3V. An estimate of the cross-sections can be computed as 6.3×10^{-15} cm²/flip-flop at the worst-case voltage and as 3.1×10^{-15} cm²/flip-flop at nominal supply voltages. Obviously, with the low error counts, more devices would be needed to get an accurate cross-section.

There was no clock upset detected in any of the devices and no upsets were detected in the JTAG TAP controller.

The device's total dose performance was good, falling into the rad-tolerant range. The curves for S/N MKJ1 and S/N MKJ2 are made by plotting static currents at the end of each proton run, with the symbols representing each step. The curve for S/N MKJ3 is the delta current recorded during the run. The dose rate was high at about 250 kRads (Si) / hour. Only moderate (< 1.5 mA) changes in the 5V bias currents were observed for S/N MKJ1 and S/N MKJ2. For S/N MKJ3, which had the higher total dose, the 5V bias current increased to 1.1 mA after 67 kRads (Si) and to 8.1 mA after 103 kRads (Si). Note that further experiments on this part type has shown lot splits with > 100 kRads (Si) total dose capability.



SUMMARY OF PROTON TEST ON THE CHIP EXPRESS QYH530 AT INDIANA UNIVERSITY JUNE, 1998

Prepared by: R. Katz, NASA/GSFC
Date: June 17, 1998

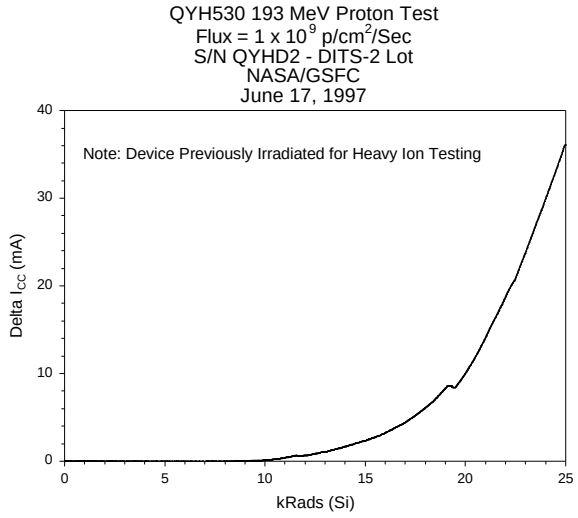
Test Facility

The Chip Express QYH530 was tested at the Indiana University Cyclotron Facility (IUCF). The proton energy was 193 MeV and the flux was set at approximately 1×10^9 p/cm²/sec. The total fluence for each device was determined by the total dose response of the device and it's affect on the current draw; details for each device including bias are given in the tables below. The device was irradiated normal to the beam.

Device Under Test

The devices were in a PGA180 package and were active during irradiation. Upsets and currents were monitored in real-time with the device being clocked at 1 MHz. The stimulation pattern was a 500 kHz square wave. The test pattern used contains 1200 flip-flops. The QYH500 architecture only has routed flip-flops; there are no hard-wired or I/O module flip-flops.

Sample devices were taken from two lots, a "DITS-2" flight lot and a production lot used for shielding experiments; no radiation shields were used on any of the devices in this test. All devices were processed with Chip Express' One-Mask technology with no laser programmed devices tested during these runs. These devices had already been subjected to heavy ion tests at Brookhaven National Laboratory.



Test Results

The following table summarizes the device, bias conditions, and irradiations.

S/N	Lot	Bias (Volts)	Total Dose kRads (Si)	Upsets	Fluence (p/cm2)
QYHD1	DITS-2	4.5	18.9	0	0.3×10^{12}
QYHD2	DITS-2	3.3	25.1	0	0.4×10^{12}
QYHD3	DITS-2	3.3	25.1	0	0.4×10^{12}
QYH55	LOT OF 70	3.3	25.1	0	0.4×10^{12}
QYH56	LOT OF 70	3.3	25.1	0	0.4×10^{12}

Five devices were irradiated, one with a 4.5V bias and four with a 3.3 bias with no upsets for all of the runs. An estimate of an upper bound for the cross-sections can be computed, assuming a single upset, as 0.5×10^{-15} cm^2/flip-flop. There was no clock upset detected in any of the devices.

The device's total dose performance was good, even though the devices had been previously irradiated. Nevertheless, the following table and figure shows radiation-tolerant performance. The dose rate was high at 216 kRads (Si) / hour.

Table 1. Static current after each run in mA.
Note: Devices previously irradiated with heavy ions.

	6.3 kRads (Si)	12.6 kRads (Si)	18.8 kRads (Si)	25.1 kRads (Si)
QYHD1	0	1.7	31.6	
QYHD2	0	0.6	8.5	35.9
QYHD3	0	0.0	7.3	32.9
QYH55	0	0.2	5.1	25.5
QYH56	0	0.0	3.3	23.3

SUMMARY OF PROTON TEST ON THE QUICK LOGIC QL3025 AT INDIANA UNIVERSITY JUNE, 1998

Prepared by: R. Katz,
NASA/GSFC
Date: June 16, 1998

Test Facility

A pAsic3 QL3025 was tested at the Indiana University Cyclotron Facility (IUCF). The proton energy was ~ 193 MeV and the flux was set at approximately 1×10^9 p/cm^2/sec. The total fluence for the run was 5.12×10^{11} p/cm^2 corresponding to a total dose of 32.1 kRads (Si). The device was irradiated normal to the beam.

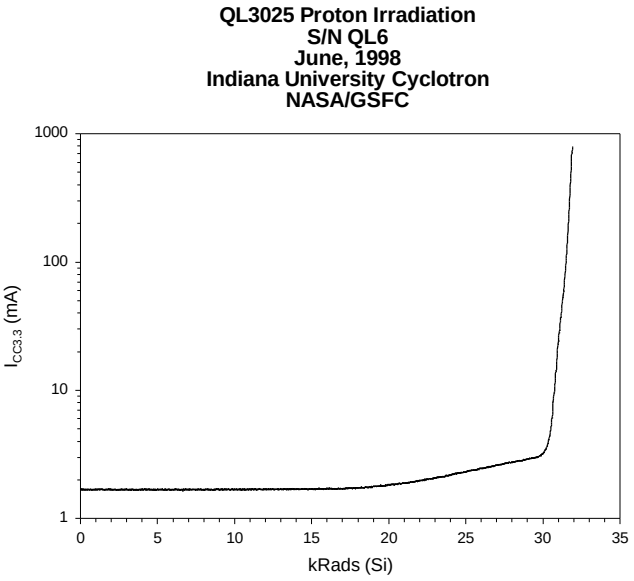
Device Under Test

The device was in a PQFP208 package and was active during irradiation. Upsets and currents were monitored in real-time with the device active at 1 MHz. The stimulation pattern was a 500 kHz square wave. Both internal hard-wired flip-flops and I/O module flip-flops were tested. This pattern contains 500 internal flip-flops with 300 in a TMR configuration and 200 in a shift register. 50 I/O module flip-flops were tested.

Test Results

No upsets were detected for this one sample, consistent with our quick-look heavy ion data, taken at an LET of 18.8 MeV-cm^2/mg. The total fluence for the heavy ion data was limited and complicated by the device's latchup characteristics. No evidence of latchup or any unusual current disturbances were observed.

The device showed a moderate increase in current at approximately 20 kRads (Si) and a current runaway at approximately 31 kRads (Si). This is thought to be a consequence of a charge pump failure. The total dose data, shown in the chart below, is comparable to our Cobalt-60 data where the device exhibited runaway at approximately 37 kRads (Si), while dosed at the relatively low rate of 0.5 kRads (Si)/hour in a static configuration. Dose rate during the proton irradiation was at the much higher rate of ~ 247 kRads (Si)/hour.



Functional Failure of EEPROMs in the Heavy Ion Environment

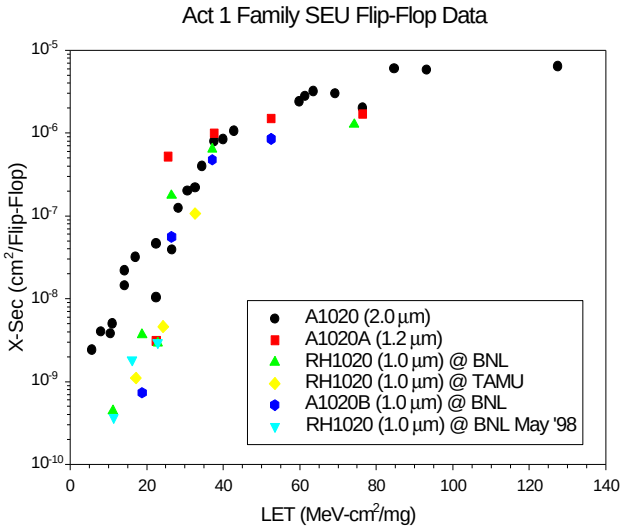
It has been demonstrated that devices, including EEPROMs, may lose functionality when upset by a single heavy ion. The Atmel AT28C010 is one example. Additionally, excess current was observed in the device. No permanent damage was detected. For the AT28C010, three types of SEUs were identified. one type was an upset in the output register, causing a read operation to fail. Additionally, there were two types of upsets where the device lost functionality over multiple cycles and entering a non-operating state.

This phenomena was covered in a good overview in "Single Event Functional Interrupt (SEFI) in Microcircuits," published in RADECS 97, Proceedings of the Fourth European Conference on Radiation and its Effects on Components and Systems. The authors are R. Koga, S. Penzin (Crain), K. Crawford, and W. Crain from the Aerospace Corporation.

Recently, a similar effect was demonstrated and analyzed in FPGAs utilizing IEEE 1149.1 JTAG circuitry, in an implementation without the optional TRST- pin. An application note on use of JTAG is in preparation and will be published shortly.

Act 1 SEU Summary

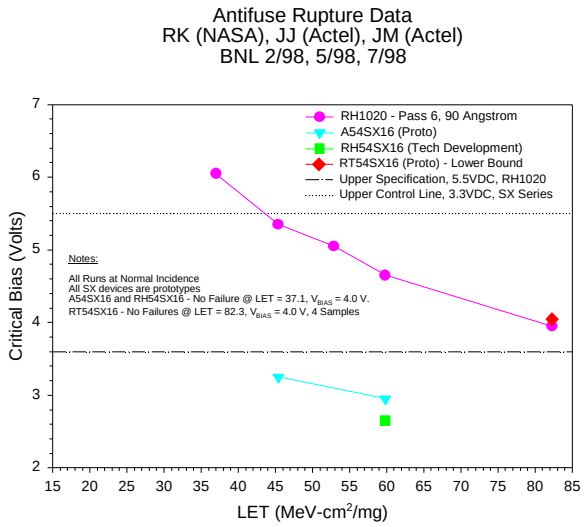
The Act 1 architecture has been fabricated in a number of technologies, many of which are utilized in space flight hardware. These consist primarily of the MEC foundry 2.0, 1.2, and 1.0 µm devices as well as the RH1020 built at Lockheed-Martin. The following chart summarizes the SEU performance of these devices. Some other variants are being flown, such as the TI A1020B, but this is relatively infrequent and the data is not included here.



Antifuse Hardness

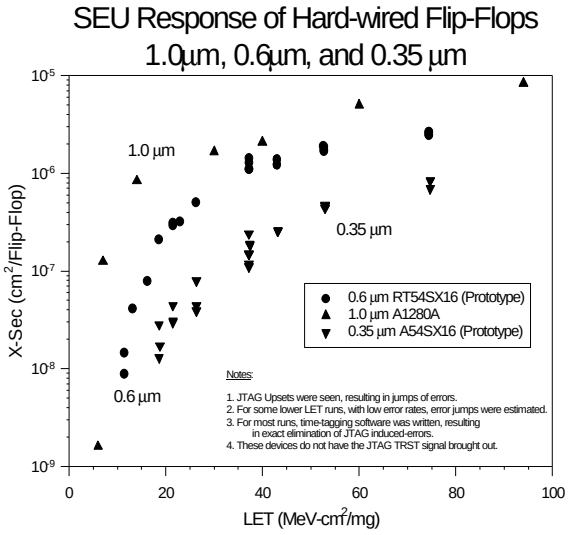
The following chart gives an update on antifuse hardness testing. Shown here is data on the RH1020 devices as well as prototypes from the SX series of FPGAs. Please note that these are prototypes used for technology assessment and development. Characteristics of production devices will differ and the user should be sure to obtain up-to-date data.

None of the antifuse 'recipes' showed any problems at an LET of 37 MeV-cm^2/mg with the ions normal to the device, which is worst-case for this effect. Note that the usual cosine law for SEU and SEL do not apply here. Of particular note is antifuse recipe 'M', which was hard (four sample devices) at an LET of 82.3 MeV-cm^2/mg with V_{DD} = 4.0 VDC; maximum rated voltage for this class of device is 3.6 VDC.



SEU Comparison of 1.0, 0.6, and 0.35mm Hard-wired Flip-Flops

The following chart shows the SEU response of *hard-wired* flip-flops from an A1280A (5V / 1.0 µm) and prototype RT54SX16 (3.3V / 0.6 µm) and A54SX16 (3.3V / 0.35 µm) devices. The hard-wired flip-flops are dedicated on the chip and are not formed by feedback connections in the routing channels. These are called 'S-Module flip-flops' in the A1280A and 'R-Cell' in the SX architecture.

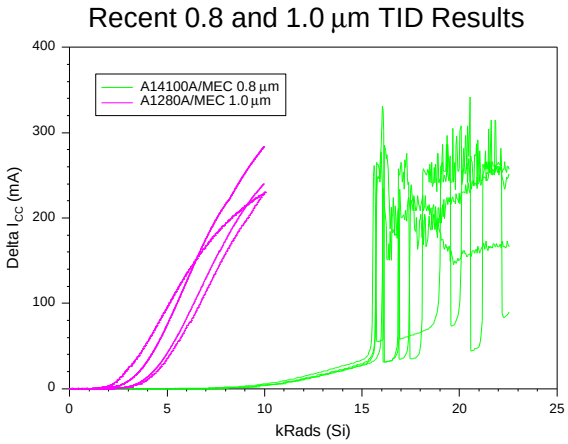


As can be seen, the smaller feature-sized parts, operating with the lower bias voltage, had improved single event upset (SEU) performance over its older, higher voltage predecessors. As can be seen from the proton data, and limited heavy ion data, the QL3025 3.3V / 0.35 µm device also performed well. Modern FPGAs will continue to scale and we expect to have test 0.25 µm feature size in the near future.

Recent Act 2 and Act 3 Total Dose Results

Below is a chart showing total ionizing dose (TID) test results for flight lots of A1280A / MEC (left) and A14100A / MEC (right). Static I_{CC} is plotted against accumulated dose.

As can be seen, these lots of devices are performing worse that 'typical' lots of these device types. While our database is not large enough to declare a trend, the decrease in TID performance is being watched, closely. A second batch of A14100A's are being qualified to 11 ± 10% kRads (Si) and are currently in high-temperature annealing.

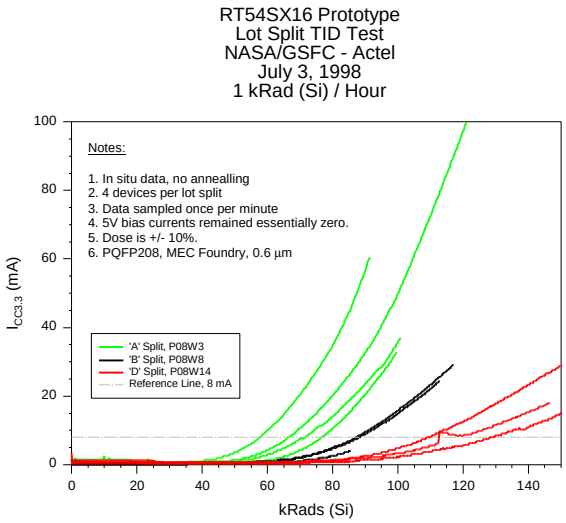


Additional data sets will be obtained in the near term, with lots of A1425A / MEC, A1460A / MEC, and A1280A / MEC being queued for test.

Recent Sub-micron Total Dose Results

The graph below summarizes the performance of sub-micron devices recently testing. Data on the prototype XQR4062XL, using a modified process, was supplied by Xilinx Corporation. Note that heavy ion test data for this prototype devices showed no latchup at an LET = 100 MeV-cm² / mg, at a temperature of 100°C.

The following chart shows the results from modifications made to prototype RT54SX16's, with the results for three lot splits shown. The reference line is arbitrary and is used as a very conservative estimate of performance and a means for making comparisons between the lot splits. Even without annealing, performance levels exceeding 100 kRads (Si) were achieved on a commercial fabrication line.



Miscellaneous

A number of items of interest are on the www site. This includes data, such as heavy ion and total dose tests on Chip Express devices, presentations from the SEE Symposium (April, 1998 in LA), and more research papers on topics such as antifuse reliability and efficiently supporting fault-tolerance in FPGAs. TID papers on EEPROMs are also being posted.

Jet Propulsion Laboratory Parts Analyses

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Failure analyses (FA), destructive physical analyses DPA) and part construction analyses (PCA) have been performed on the following part types. For a copy of the report, contact me (phone 818-354-9529, fax 818-393-4559 or e-mail to joan.c.westgate@jpl.nasa.gov) and request the desired document by "Log#".

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FAILURE ANALYSIS				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
6798	Harris Semiconductor (HAR)	9405B	2K x 8 PROM	HS9-6617RHB
6950	MDI	9651	Hybrid DC-DC Power Converter: ±12V, +5V	3310
8000	International Rectifier Corporation (IRC)	9617	Power Hexfet	2N7225
8001	Hewlett Packard Company (HPC)	9541	Dual Channel Optocoupler, HCPL-6731	5962-89785022A

DESTRUCTIVE PHYSICAL ANALYSIS				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
6981	UTMC	9647	Programmable Array Logic	5962R9475401QXC
7048	NSC	9736B	Low Power Low Offset Voltage Comparator	LM193J / 883
7049	LNT	9443	Single Supply Dual Precision Operational Amplifier	LT1211MJ8

DESTRUCTIVE PHYSICAL ANALYSIS (CONTINUED)				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
7050	LNT	9629	Pulse Width Modulator, Power Controller	LT1243MJ8
7051	LNT	9616	Pulse Width Modulator	LT1245MJ8
7052	Linfinity	9345	Power Supply Output Supervisory Circuit	SG1543L/883
7053	TIX	9736C	Adjustable Precision Shunt Regulator	TL431MJGB
7055	Motorola	9706	Silicon Controlled Rectifier	MCR-265-4
7056	INR	9546	HEXFET	IRHF7130
7057	INR	9723	HEXFET	IRHF7230
7058	INR	9507	HEXFET	IRHG6110
7063	ILC Data Device Corporation	9749	1553 BC/RT/MT W/SRAM Hybrid	BU-61582F1-300
7067	LNT	9649A	Voltage Reference	RH1009MH (label) SL50233 (on part)
7076	Analog Devices	9708	Sample and Hold Amplifier	SMP11
7077	NES (New England Semiconductor)	9615	NPN Transistor	JV2N2484
7086	Teledyne Relay	Unknown	Latching Relay	442K-12WP-001
7087	Q-Tech	9742	Crystal Oscillator	21054687-101
7088	Q-Tech	9742	Crystal Oscillator	21054687-102
8005	Harris Semiconductor	9623	Quad Differential Line Driver	HS9-26C31RH-8
8006	Harris Semiconductor	9711	Schmitt Hex Inverter	54HCS14KMSR
8007	Harris Semiconductor	9536	Dual 4-Input AND Gate	54HCS21KMSR
8013	CDI	NONE	Diode	JANTXV1N5711-1

PART CONSTRUCTION **ANALYSIS**				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
6745	Intel Corporation	N/A	Intel 16 Mb "Smart Voltage" Flash Memory	DA28F016SV
7010	Lambda Advanced Analog	9736	DC-DC Converter	AHF2812D/CH

Goddard Space Flight Center Parts Analyses

Listed below are the EEE parts analyses completed by the GSFC Parts Analysis Laboratory. The GSFC reports are available to NASA personnel and current NASA contractors by contacting your NASA project office.

EV JOBS							
Job Number		**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
80650	EV	NATIONAL SEMICONDUCTOR	9648	MICROCIRCUIT	54ACT374	P	04/27/98
CA JOBS							
Job Number		**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
80851	CA	MICROSEMI, INC.	9606D	DIODE	JANTX1N4104UR-1	F	06/04/98
88026	CA	ROUSEMOUNT AEROSPACE	9812	THERMISTOR	1621896	P	05/01/98
88235	CA	FAIR-RITE	UNKN	FERRITE BEAD	2943666671	P	05/26/98
88240	CA	ELMWOOD SENSORS, INC	9811	THERMAL SWITCH	G3111P641/01J-40D-15C	P	05/28/98
80953	CA	COMPENSATED DEVICES, INC.		DIODE	JANTXV1N4572A-1	P	07/14/98
88209	CA	SEMICON COMPONENTS	9805	DIODE	JANTX1N5816	P	04/17/98
88227	CA	HARRIS SEMICONDUCTOR	9633	MICROCIRCUIT	5962R9581201VCC	P	04/26/98
88205	CA	SEMICON COMPONENTS	9808	DIODE	JANTX1N5816	P	04/17/98
88225	CA	NATIONAL SEMICONDUCTOR	9439	MICROCIRCUIT	M38510/75307BEA	P	04/15/98
88221	CA	LOCKHEED MARTIN	9751	MICROCIRCUIT	198A592-225	P	04/21/98
88198	CA	NATIONAL SEMICONDUCTOR	9745A	MICROCIRCUIT	5962-9218601MSA	P	04/15/98
FA JOBS							
Job Number		**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
88162	FA	HARRIS	9718	FLIP-FLOP MICROCIRCUIT	5962R9579301VRC	F	05/08/98
88213	FA	TEXAS INSTRUMENTS	8040	LINE DRIVER	679-9111	P	05/06/98
88232	FA	SPACE ELECTRONICS	9451	MICROCIRCUIT	G311P-783-200	F	06/22/98

GIDEP & NASA Advisory Impact Report

NASA Advisories, GIDEP Alerts, Problem Advisories, Safe Alerts, Product Change Notices, Diminishing Source Notices and Agency Action Notices Related to EEE Parts

GIDEP & NASA Advisory Impact Report summary will no longer be included in the EEE Links publication. For the most current information on parts issues please refer to the EPIMS database on the WWW. The URL for EPIMS-WEB is : http://epims.gsfc.nasa.gov

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