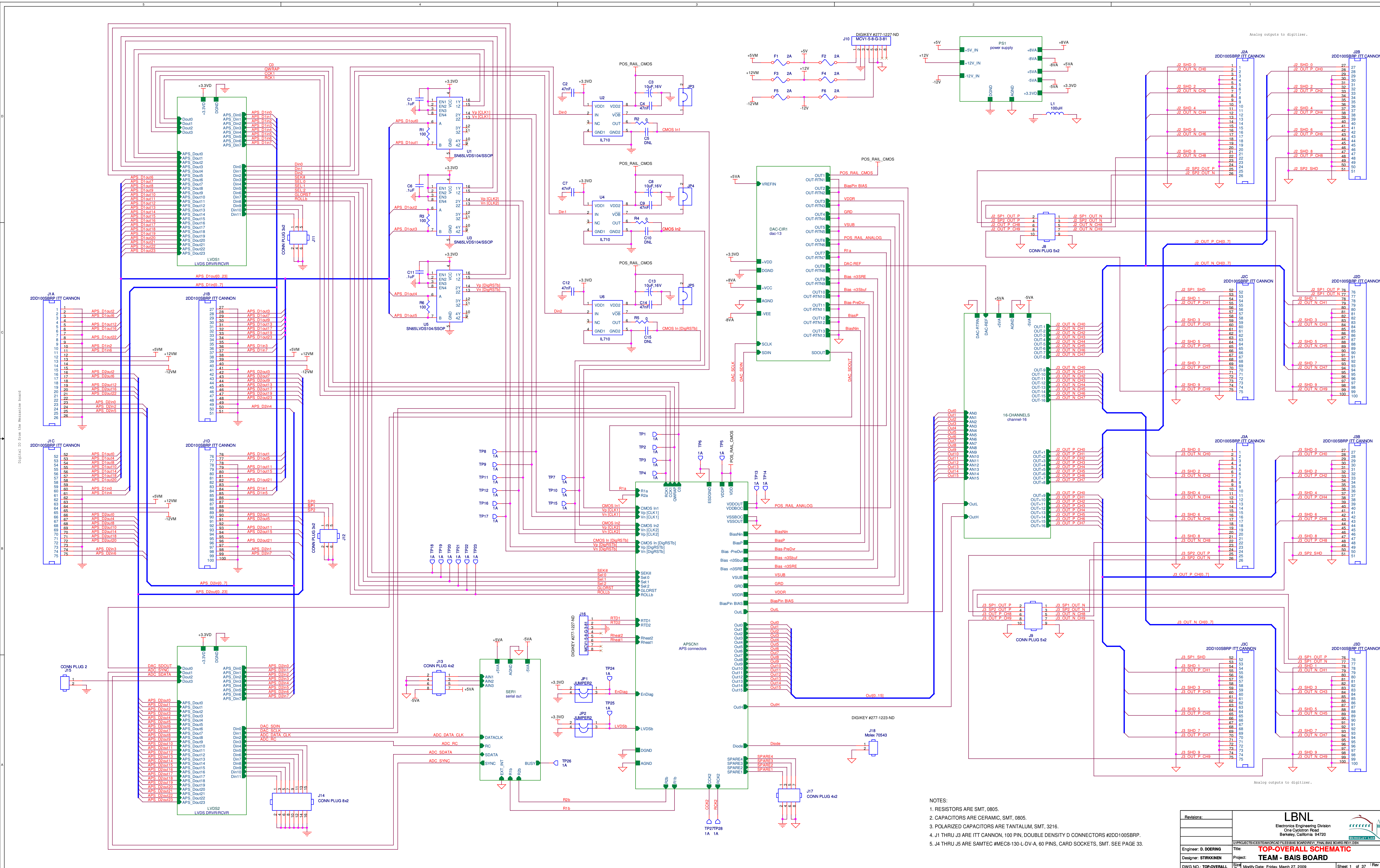
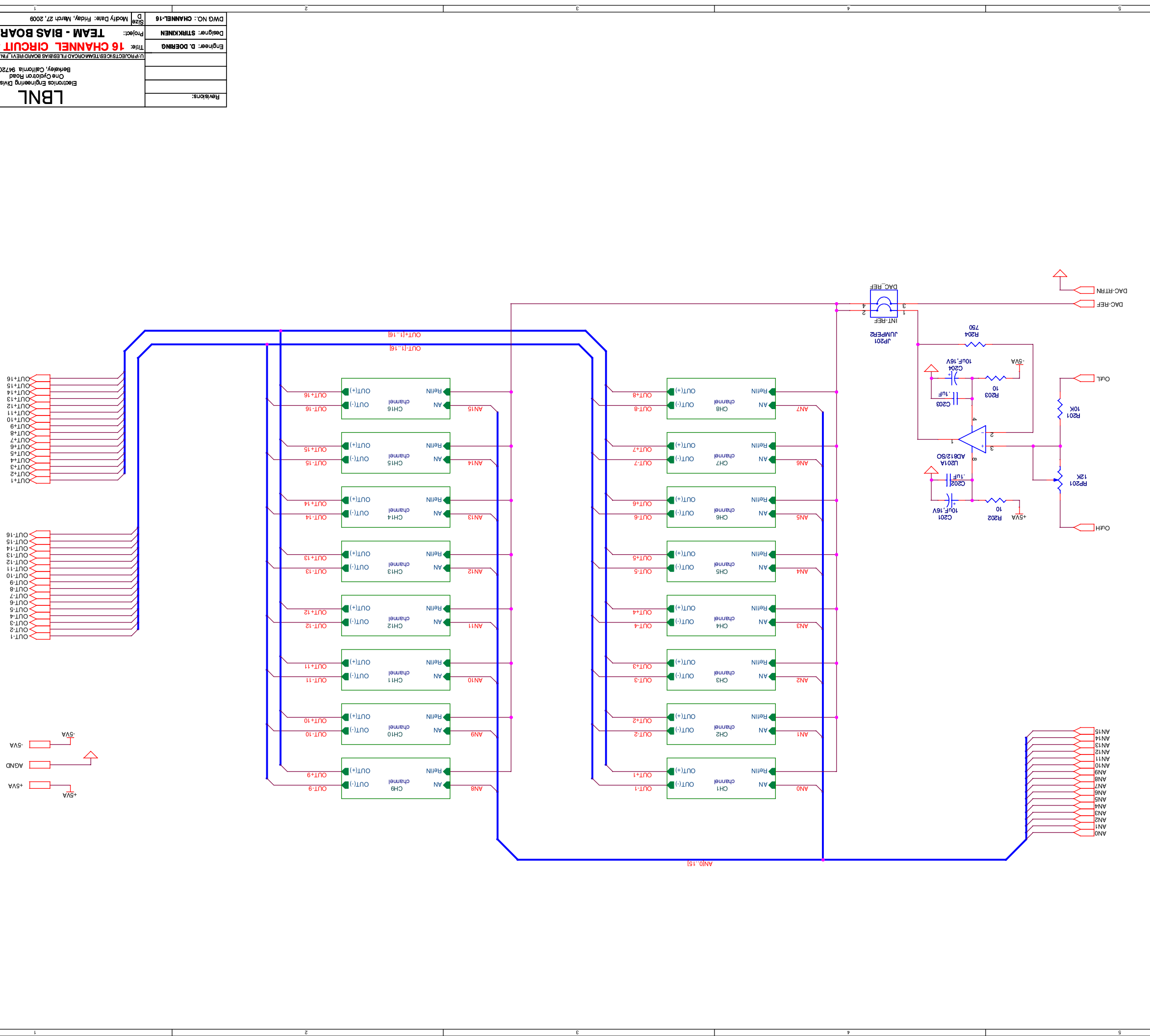


NOTES:

1. RESISTORS ARE SMT, 0805.
2. CAPACITORS ARE CERAMIC, SMT, 0805.
3. POLARIZED CAPACITORS ARE TANTALUM, SMT, 3216.
4. J1 THRU J3 ARE ITT CANNON, 100 PIN, DOUBLE DENSITY D CONNECTORS #2DD100SBRP.
5. J4 THRU J5 ARE SAMTEC #MEC8-130-L-DV-A, 60 PINS, CARD SOCKETS, SMT. SEE PAGE 33.

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN
Engineer: D. DOERING	Title: TOP-OVERALL SCHEMATIC
Designer: STIRKKINEN	Project: TEAM - BAIS BOARD
DWG NO.: TOP-OVERALL	Size D · Modify Date: Friday, March 27, 2009 · Sheet 1 of 37 · Rev 0

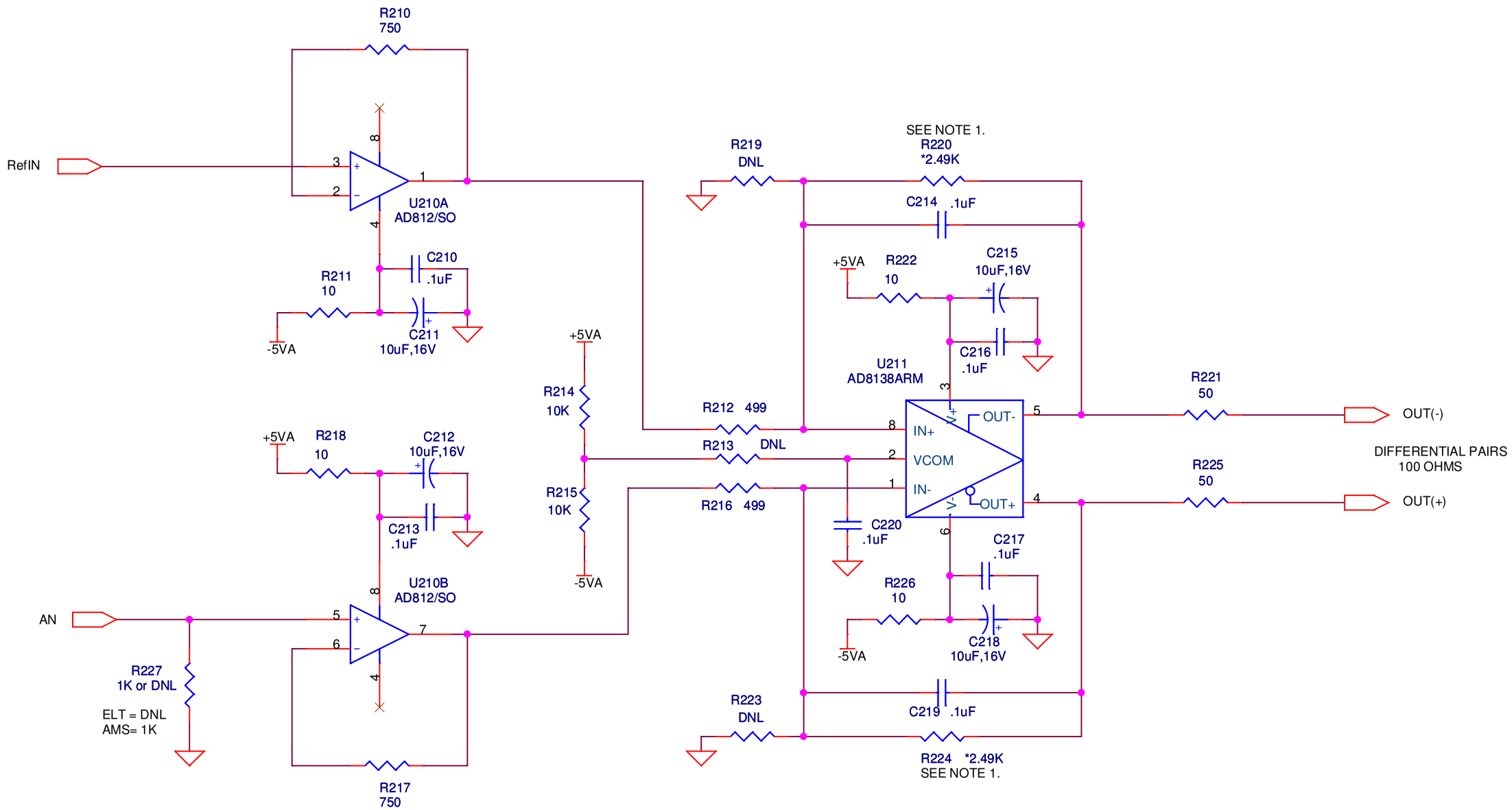


Revisions:	

LBNL
Electronics Engineering Division
One Cyclotron Road
Berkeley, California 94720
BERKELEY LAB

U:\PROJECTS\CES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN

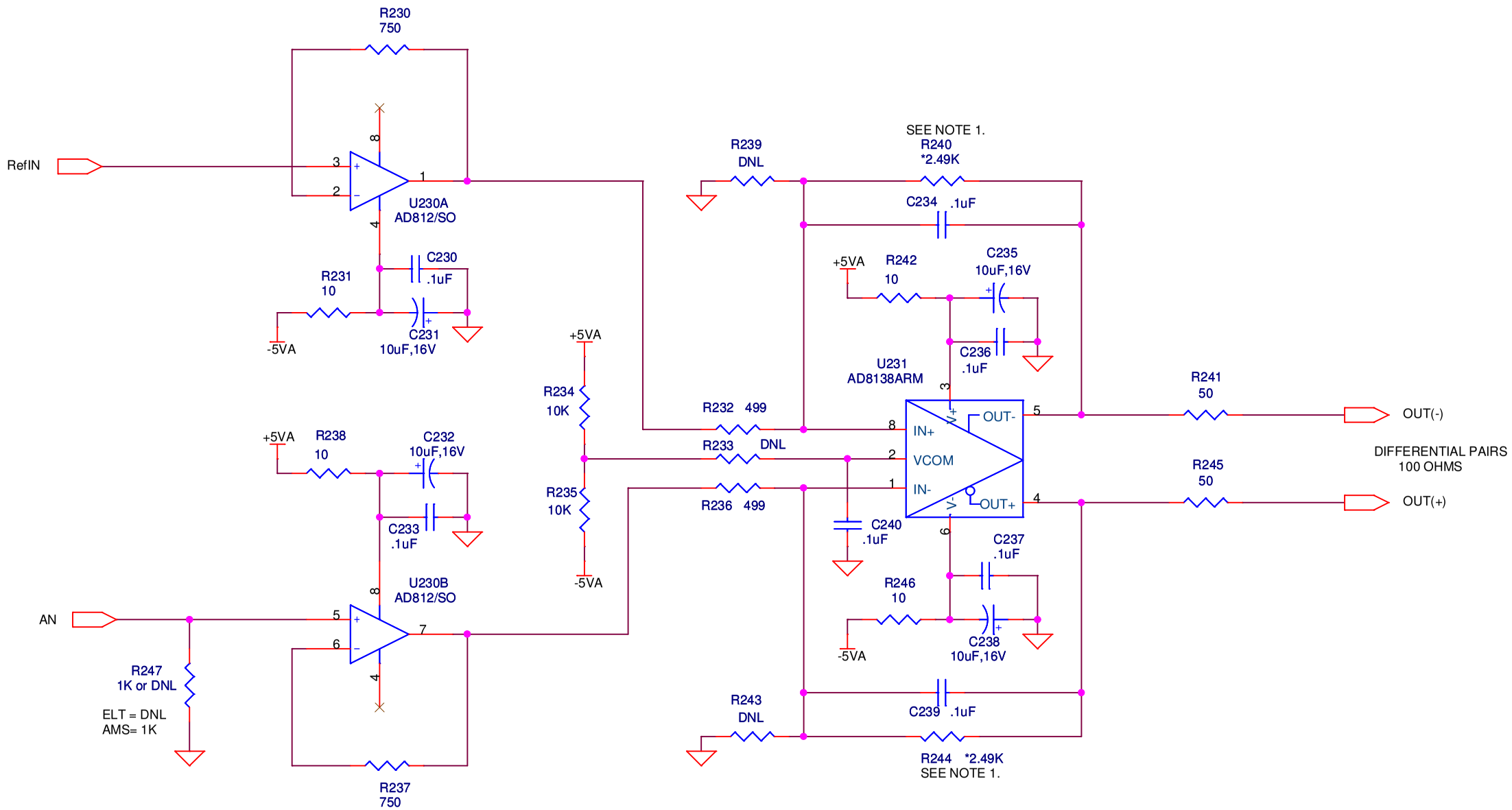
Title:	**16 CHANNEL CIRCUIT SCHEMATIC**
Project:	**TEAM - BIAS BOARD**
Designer:	**STRIKKINEN**
Engineer:	**D. DOERING**
DWG NO.:	**CHANNEL-16**
Size: D	Modify Date: Friday, March 27, 2009 Sheet 2 of 37 Rev 0



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

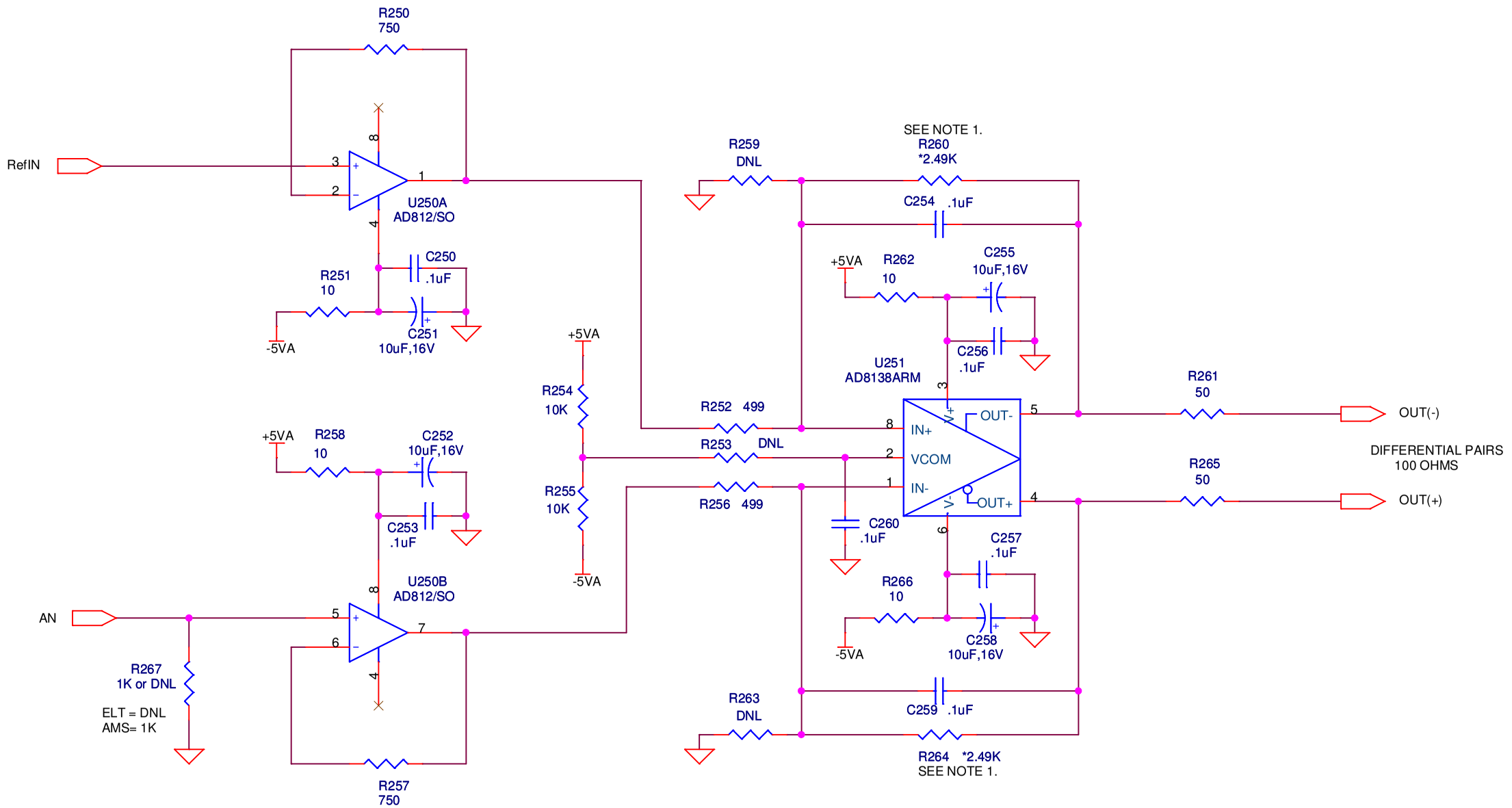
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 3 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

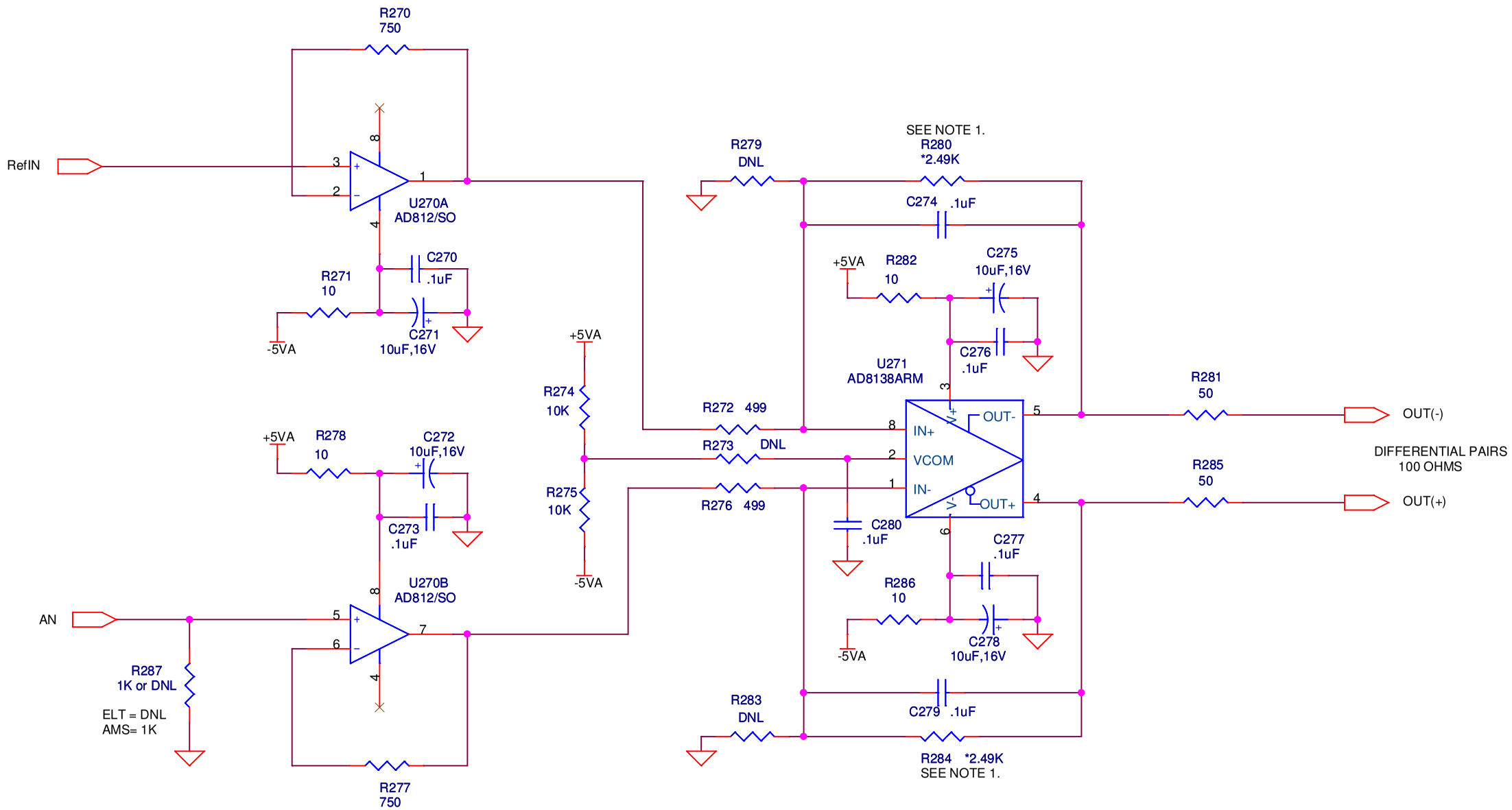
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 4 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

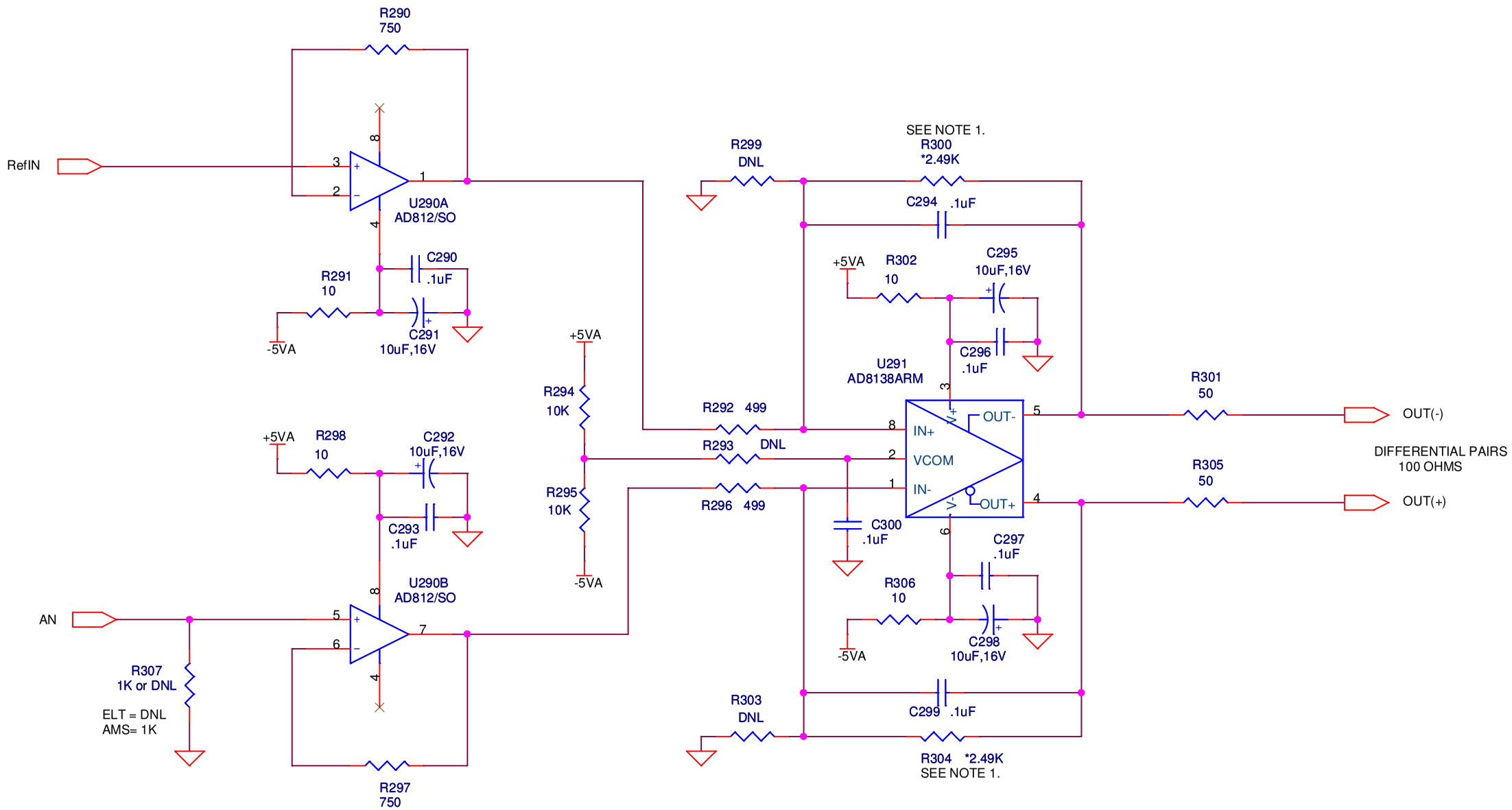
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 5 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

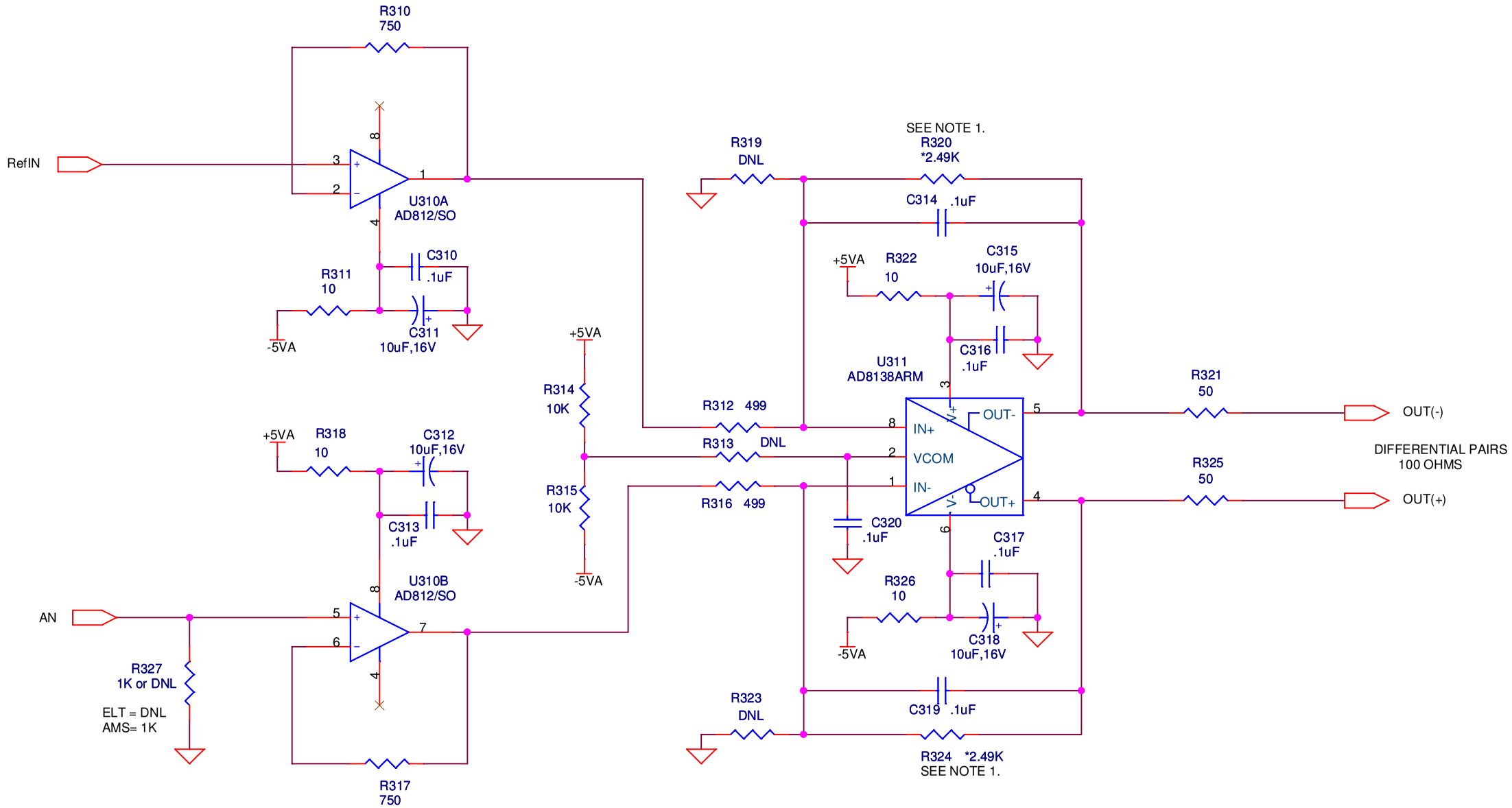
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 6 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

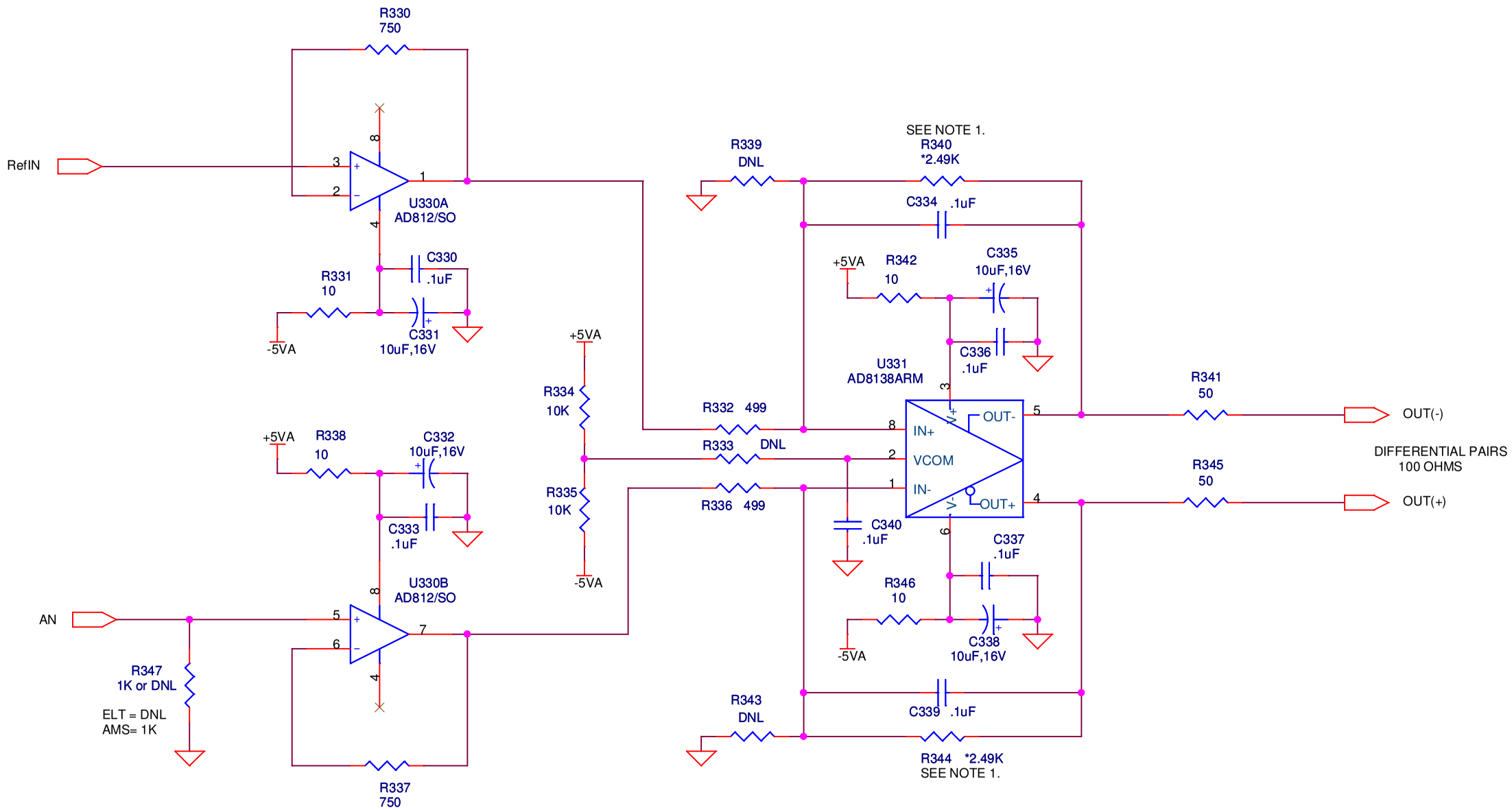
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 7 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

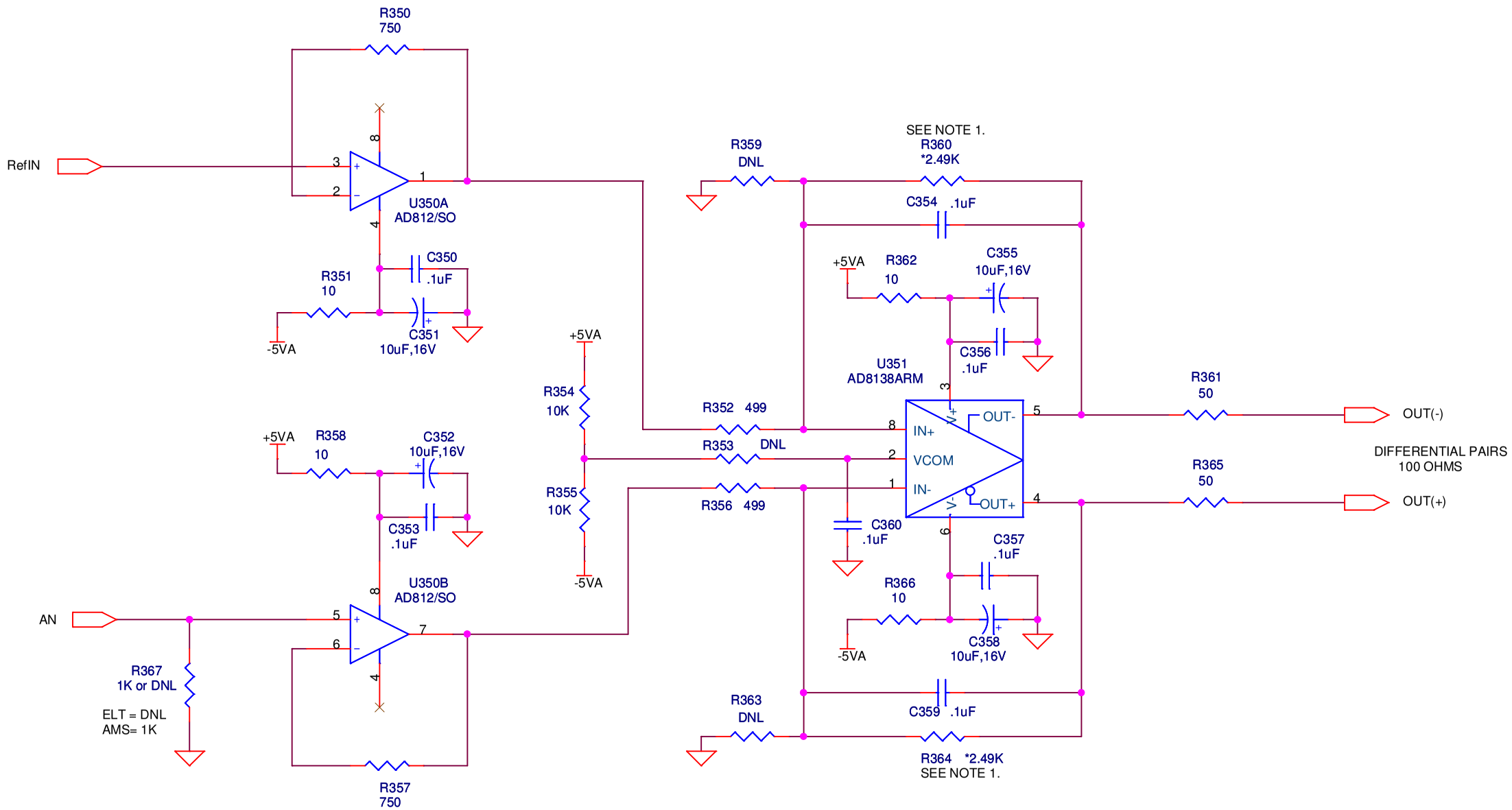
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 8 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

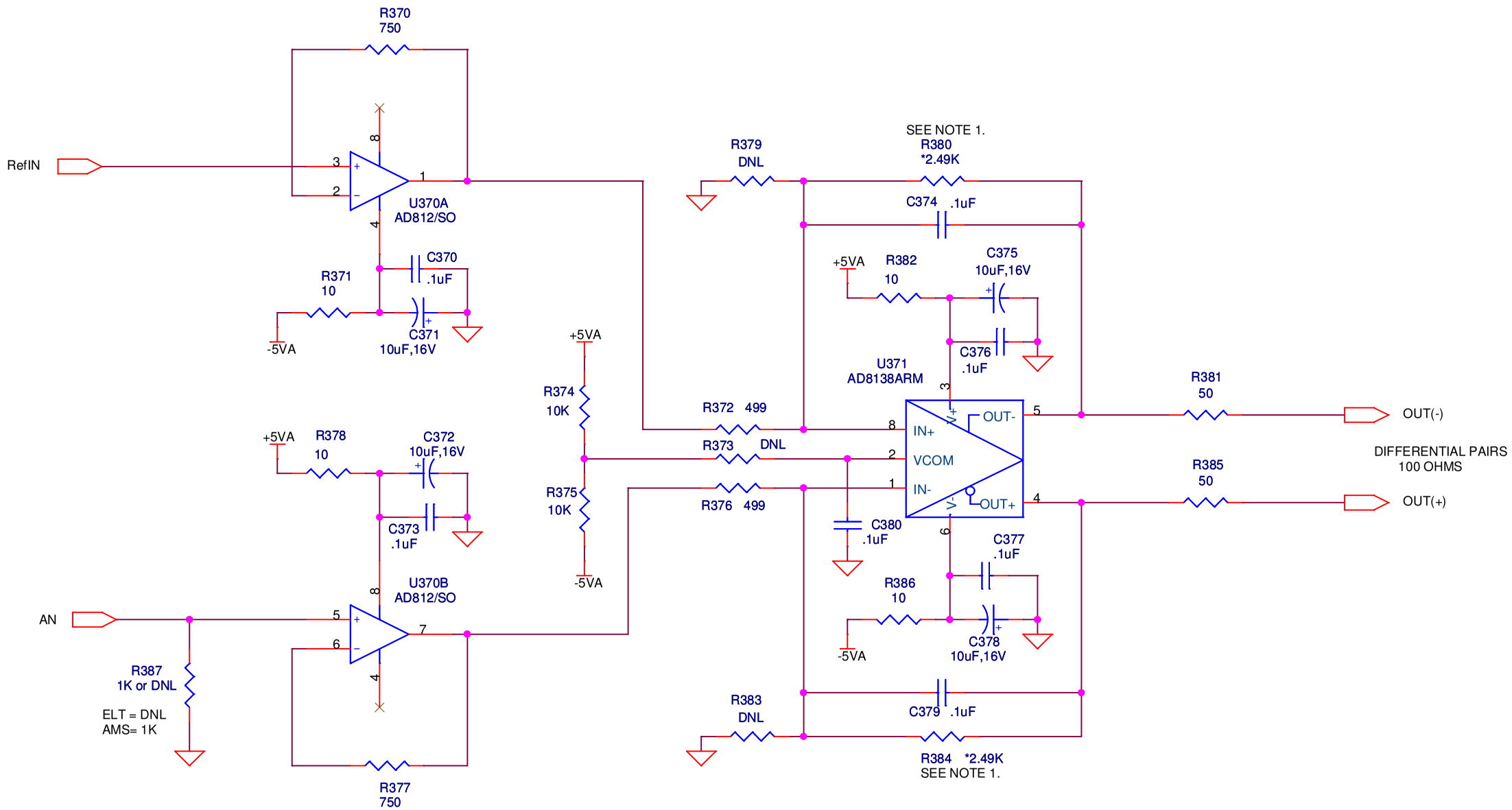
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 9 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

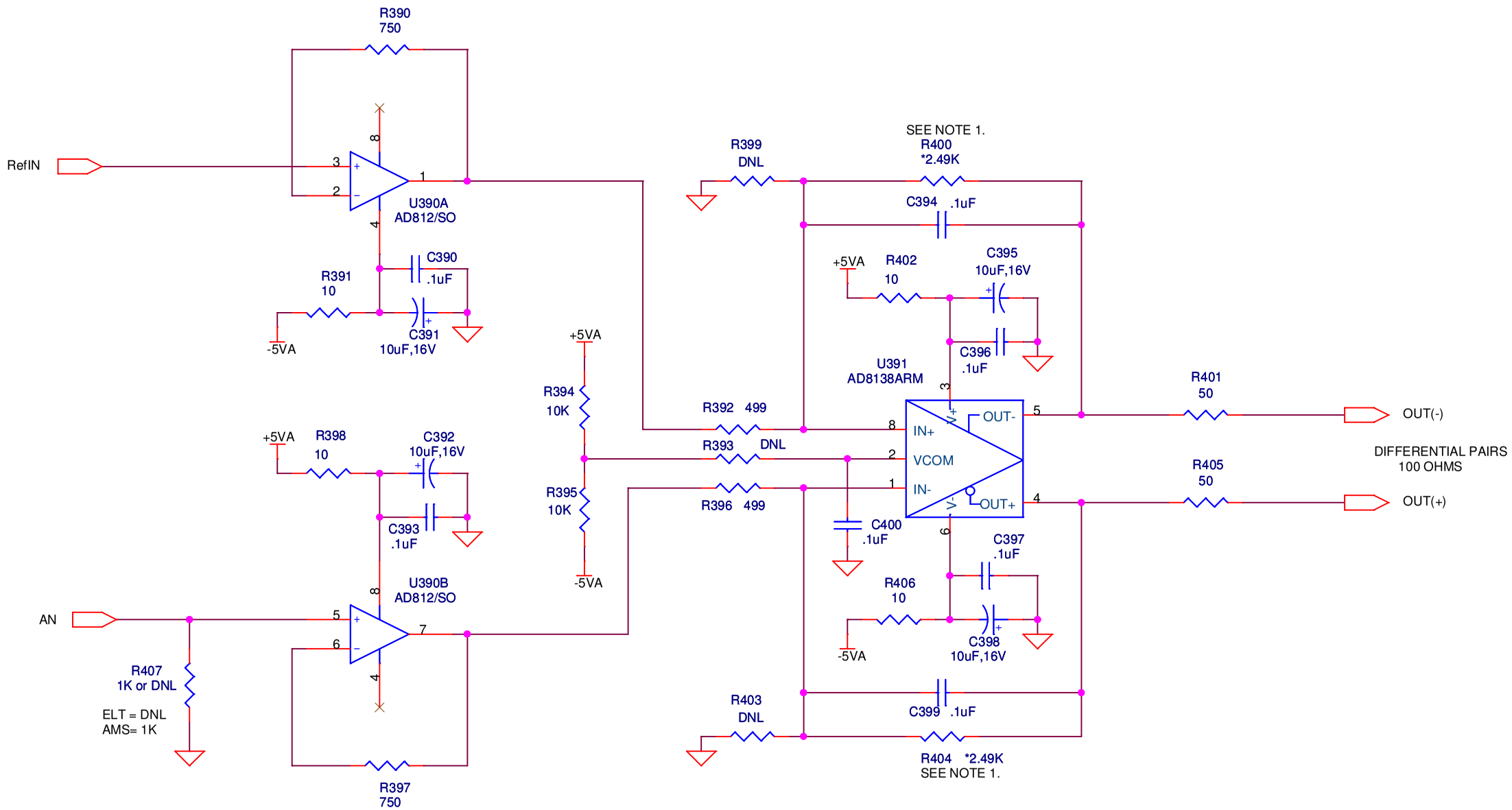
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 10 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

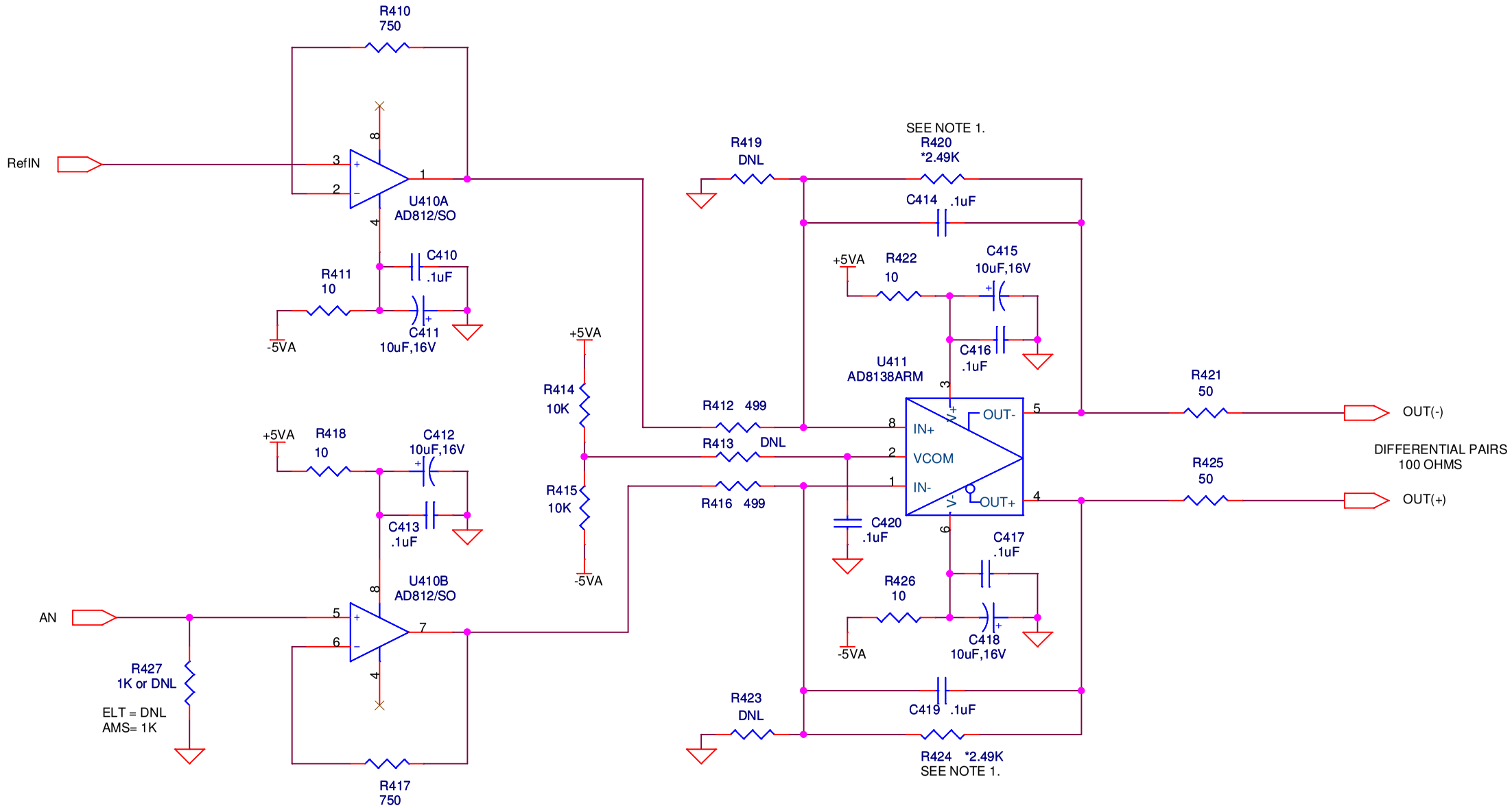
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 11 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

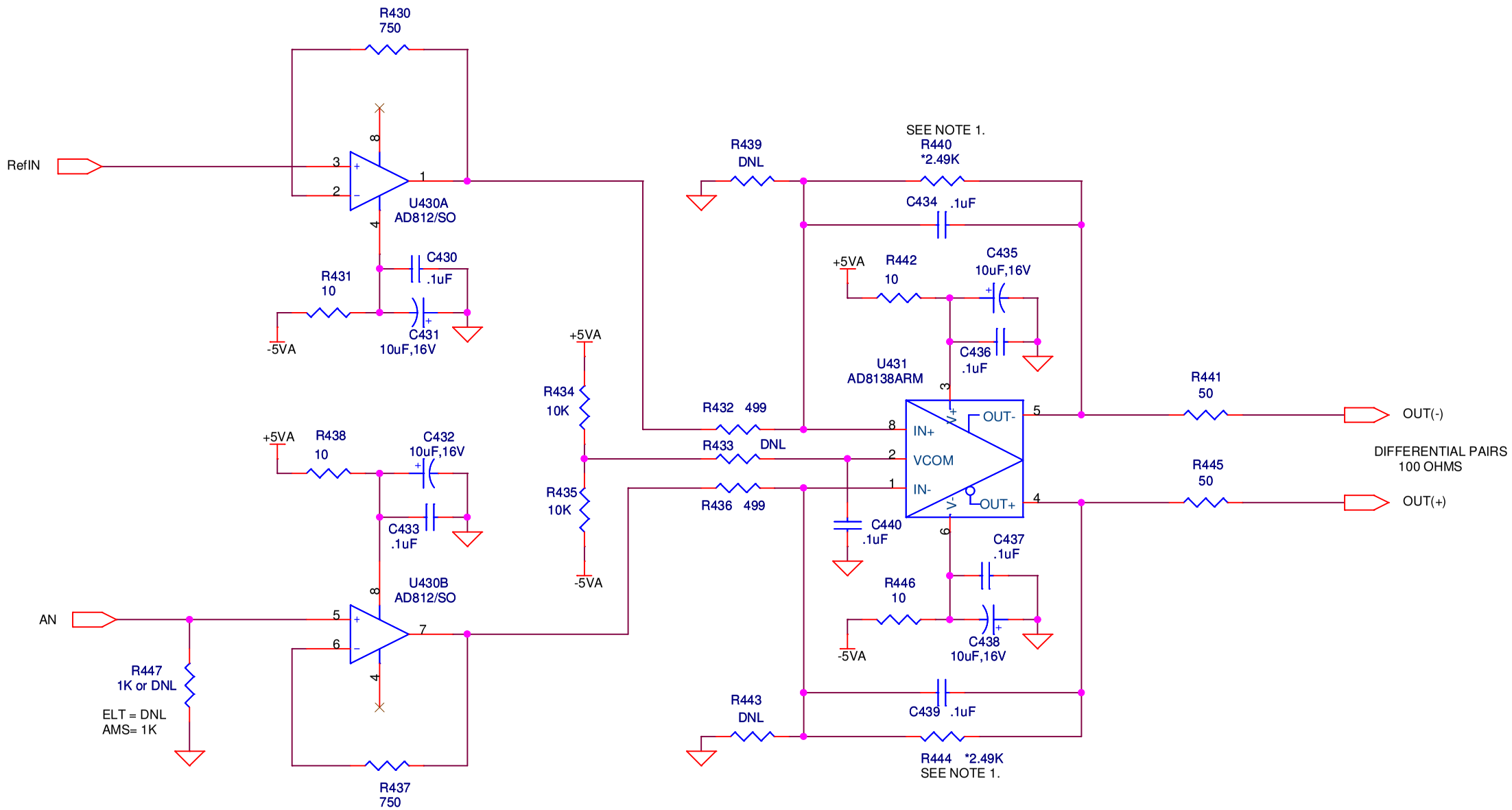
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 12 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

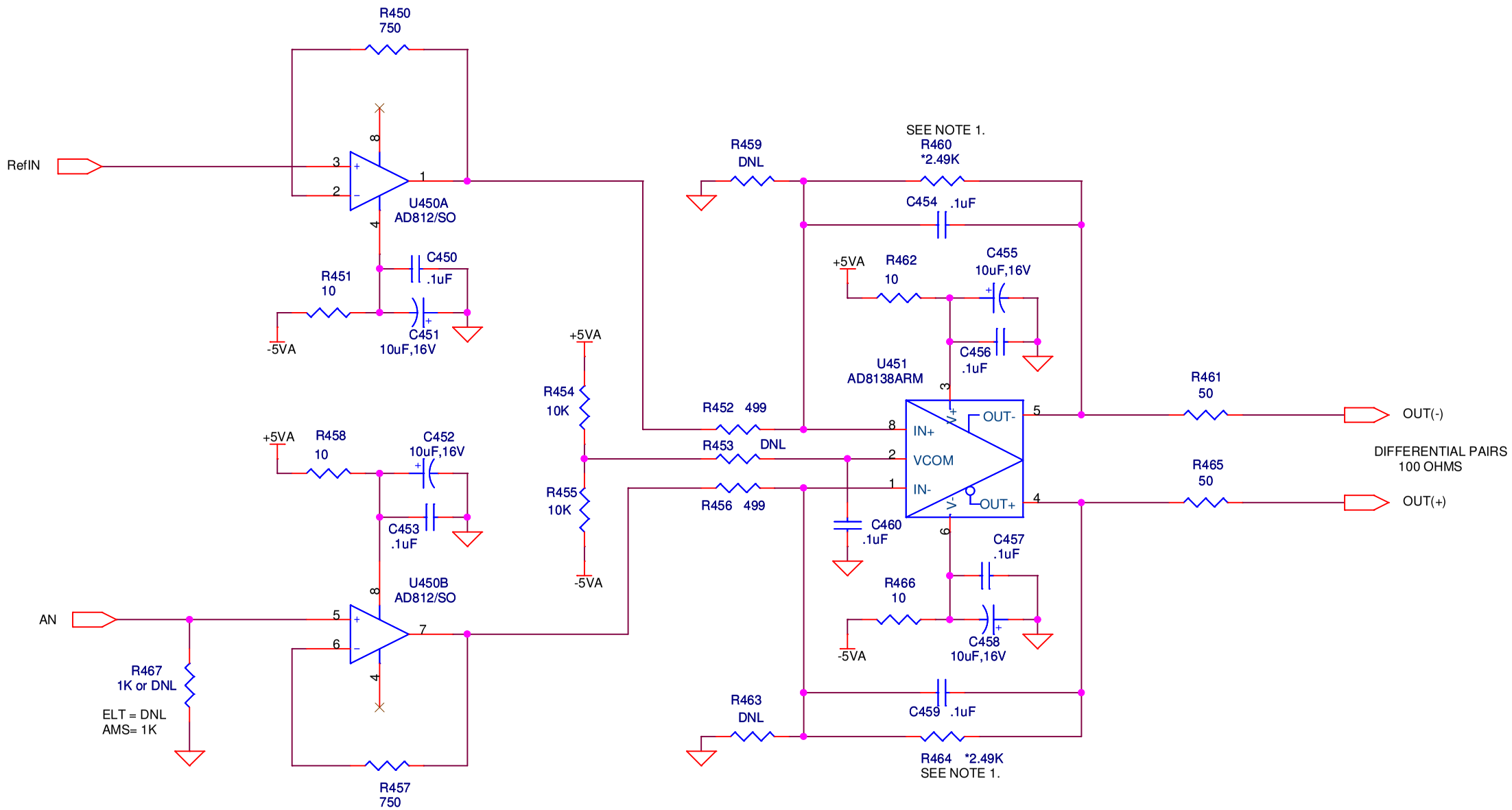
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**		
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**		
DWG NO.: **channel**	Size C	Modify Date: Friday, March 27, 2009	Sheet 13 of 37 Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

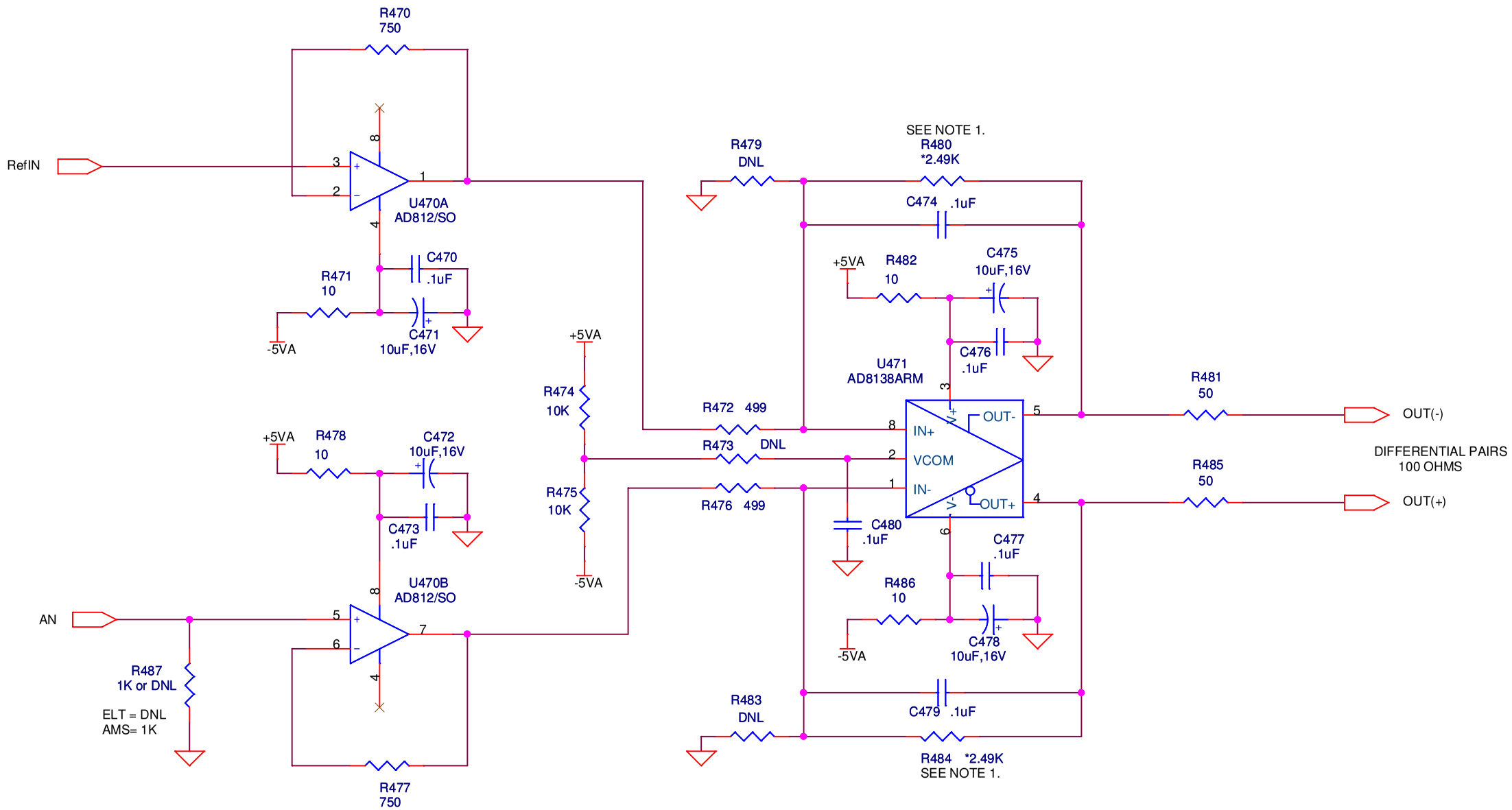
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 14 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

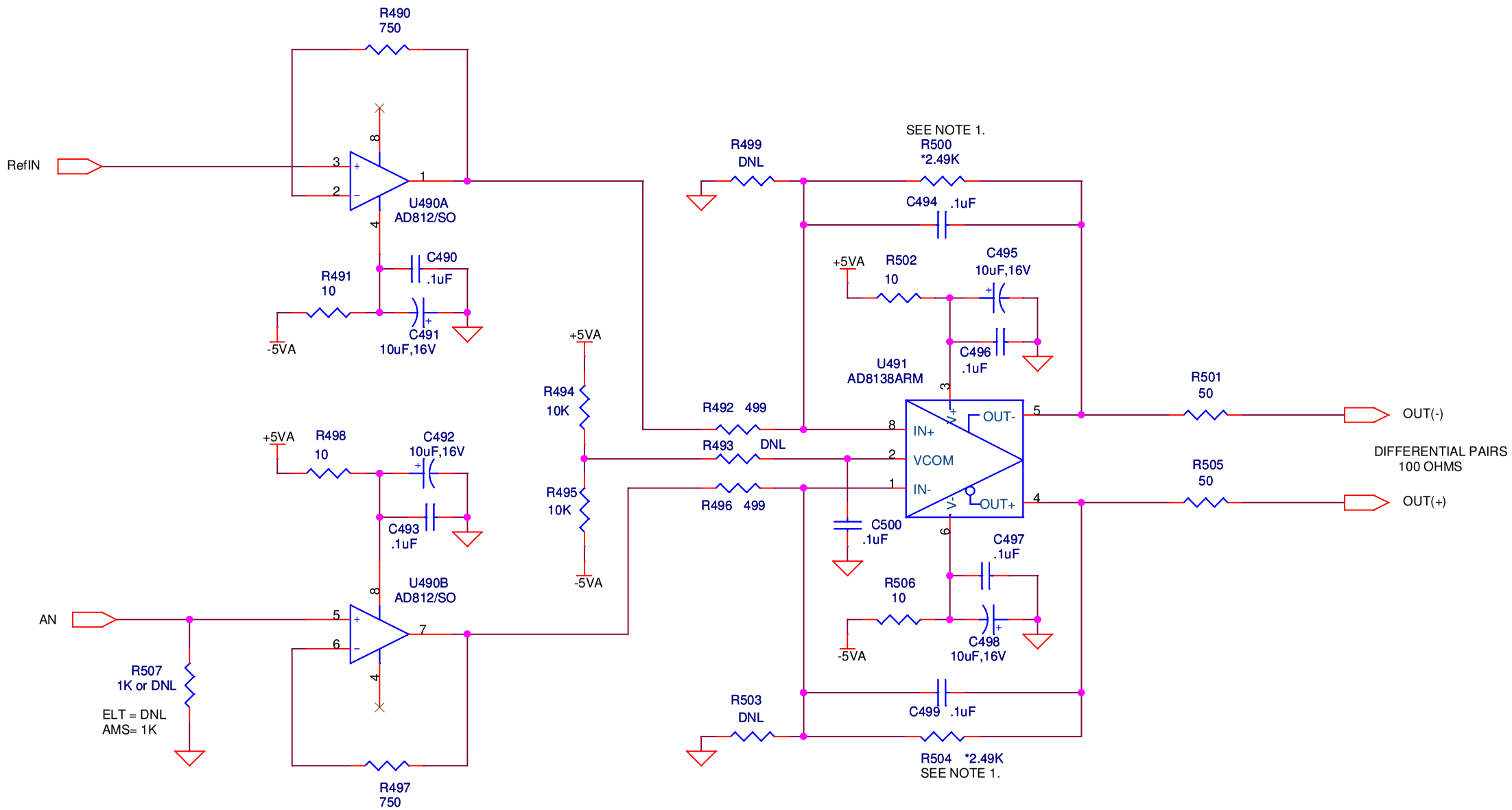
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**		
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**		
DWG NO.: **channel**	Size C	Modify Date: Friday, March 27, 2009	Sheet 15 of 37 / Rev 0



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

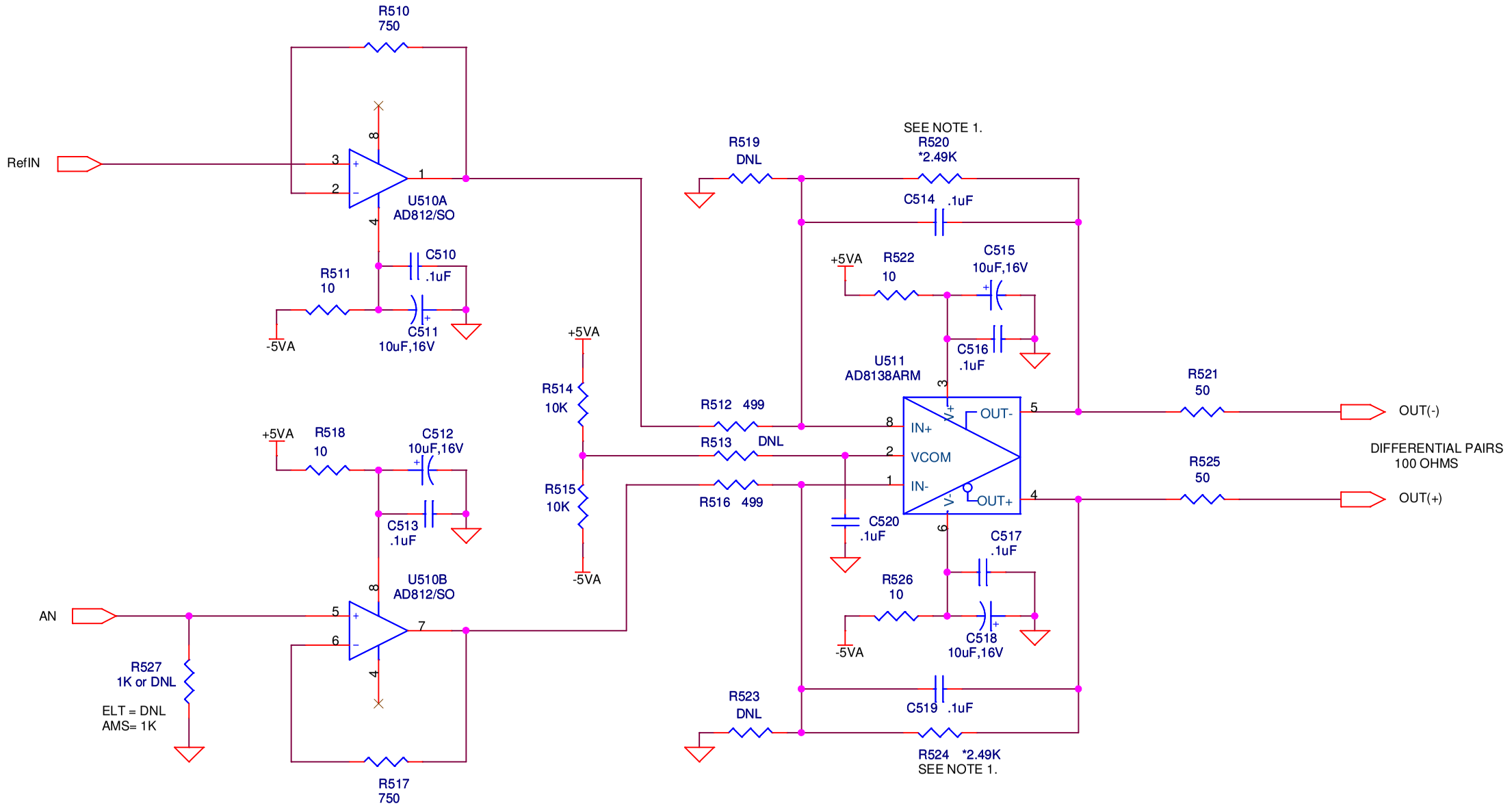
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 16 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 17 of 37 | Rev **0**



NOTES:

1. *2.49K VALUES (2 PLACES PER CHANNEL) IS FOR LIMITING THE BANDWIDTH TO 70MHz.

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SINGLE CHANNEL (1 OF 16)**	
Designer: **STIRKKINEN**	Project: **TEAM - BIAS BOARD**	
DWG NO.: **channel**	Size C | Modify Date: Friday, March 27, 2009	Sheet 18 of 37 | Rev **0**

Revisions:	

LBNL
Electronics Engineering Division
One Cyclotron Road
Berkeley, California 94720

U:\PROJECTS\CESTEAM\PCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN

Title: **13 DAC CIRCUITS SCHEMATIC**

Project: **TEAM - BIAS BOARD**

Engineer:	D. DOERING
Designer:	STRKKINEN
DWG NO.:	DAC-13
Size: C	Modify Date: Friday, March 27, 2009
Sheet 19 of 37	Rev 0

SDOUT

SDIN

SCLK

+VREF

VREFIN

TP600 1A

TP601 1A

U600 AD8602/SOIC8

OUT
GND
TRIM
TEMP
IN

R600 10K

R602 5K

C600 .1UF

C601 .1UF

U601 OPA277/SOIC8

R601 10K

+VCC
-VEE

TP602 1A

+VDD
DGND
+VCC
-VEE
AGND

JP600 JP601 JP602 JP603 JP604 JP605 JP606 JP607 JP608 JP609 JP610 JP611 JP612 JP613 JP614 JP615

VREF1 VREF2 VREF3 VREF4 VREF5 VREF6 VREF7 VREF8

JP616 JP617 JP618 JP619 JP620 JP621 JP622 JP623 JP624 JP625

VREF9 VREF10 VREF11 VREF12 VREF13

DAC1 DAC2 DAC3 DAC4 DAC5 DAC6 DAC7 DAC8 DAC9 DAC10 DAC11 DAC12 DAC13 dac

APS

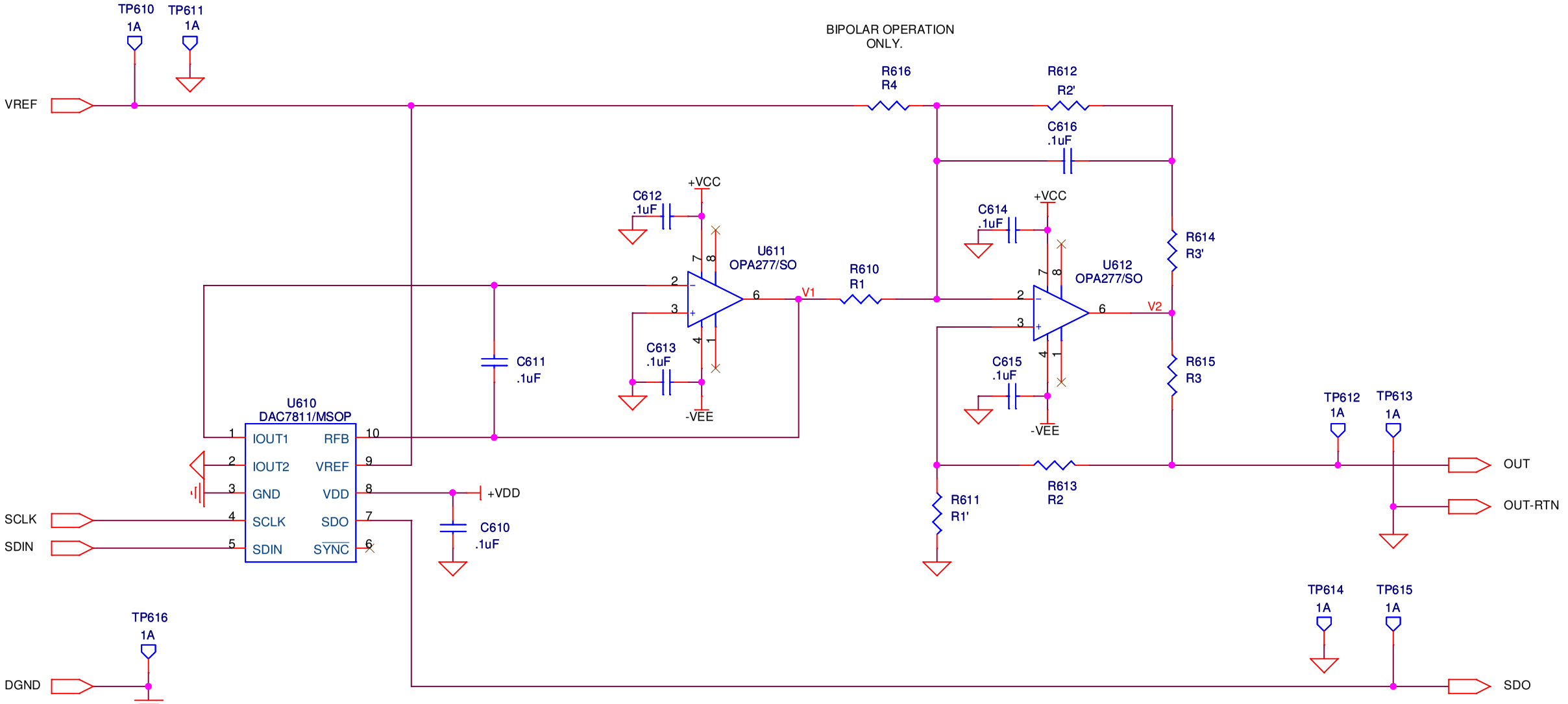
PSEUDA DIFF REFP

TEMP R

SDO SCLK SDIN VREF DGND +VDD +VCC -VEE AGND OUT OUT-RTN

OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7 OUT8 OUT9 OUT10 OUT11 OUT12 OUT13

OUT-RTN1 OUT-RTN2 OUT-RTN3 OUT-RTN4 OUT-RTN5 OUT-RTN6 OUT-RTN7 OUT-RTN8 OUT-RTN9 OUT-RTN10 OUT-RTN11 OUT-RTN12 OUT-RTN13



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

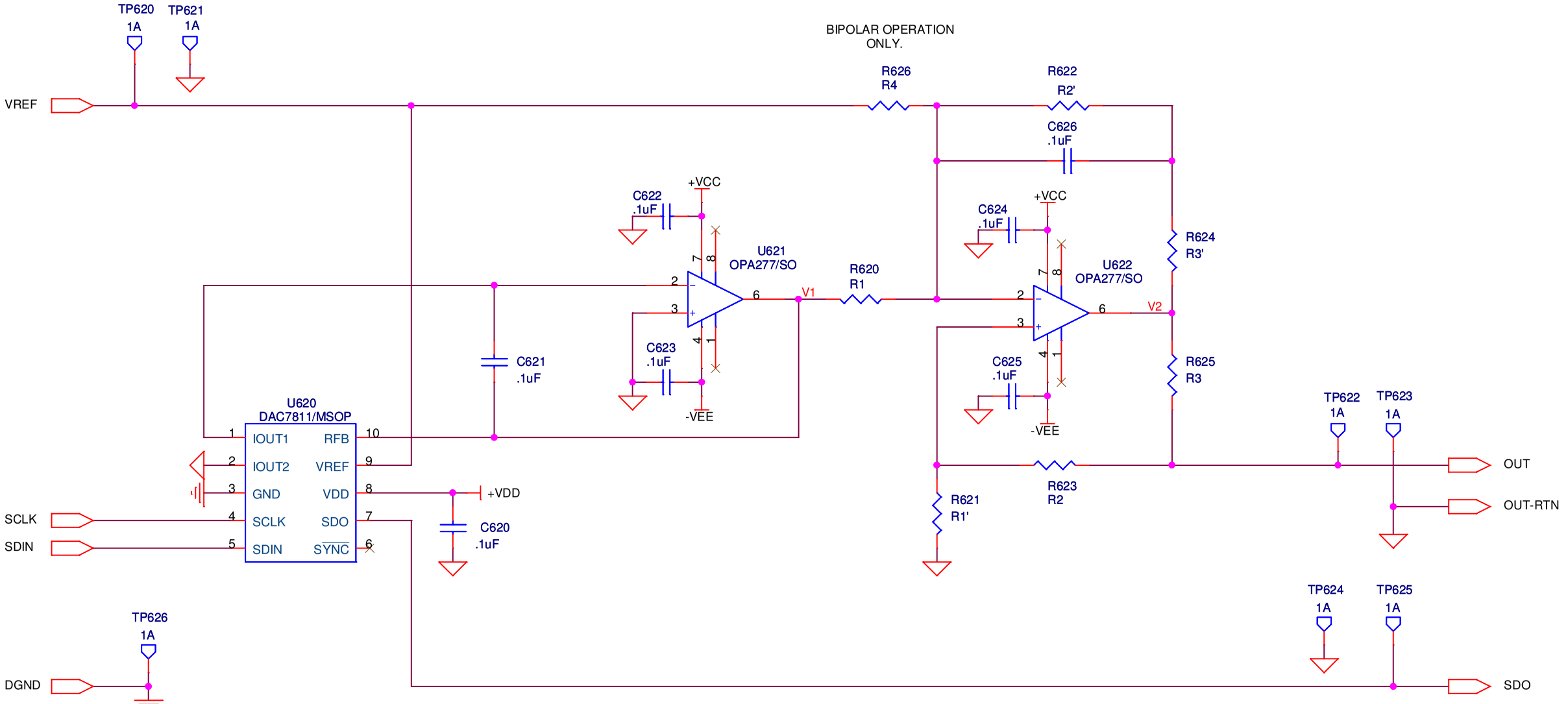
VOLTAGE OUTPUT BIPOLAR:

R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

$I_{out\,max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 20 of 37 Rev 0



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

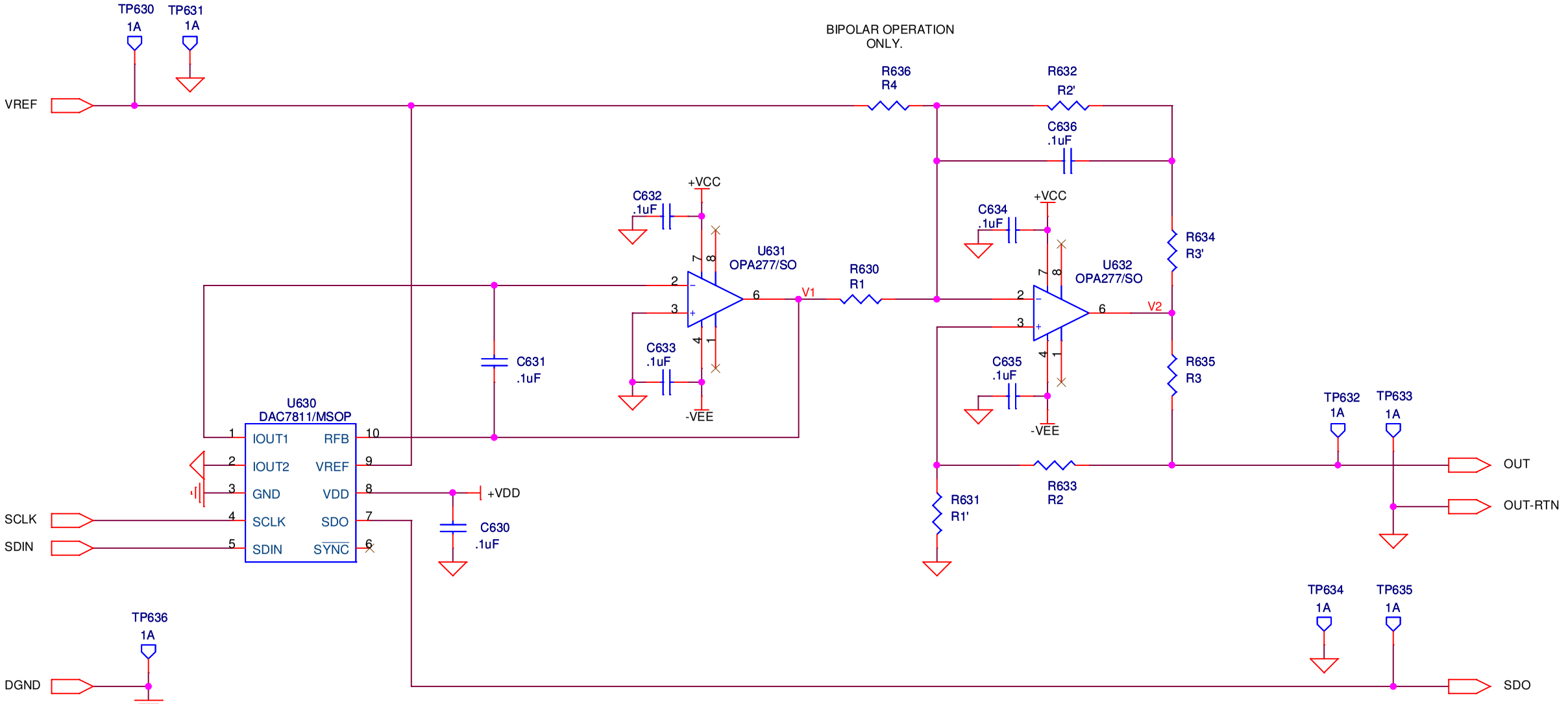
VOLTAGE OUTPUT BIPOLAR:

R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

$Iout_{max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 21 of 37 Rev 0



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

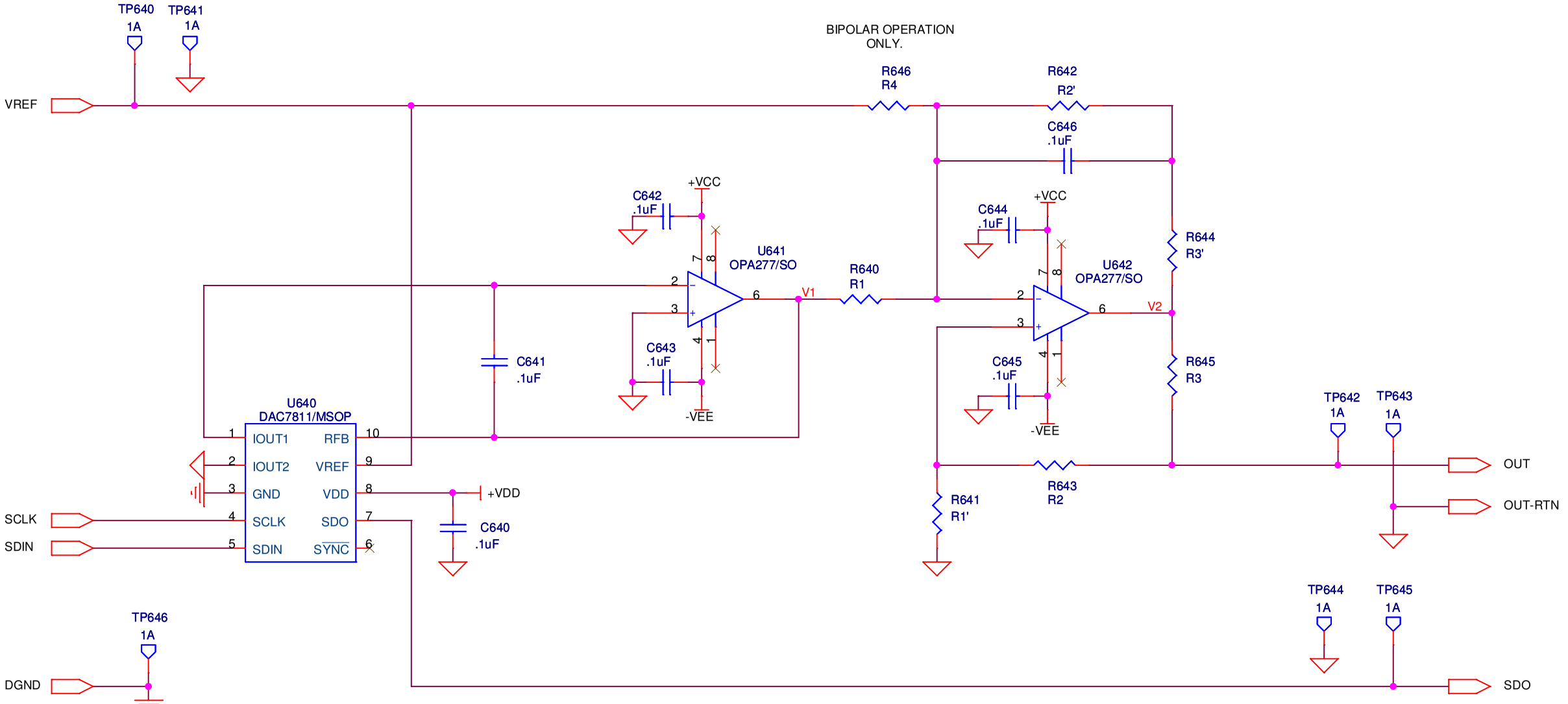
VOLTAGE OUTPUT BIPOLAR:

R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

$I_{out\,max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 22 of 37 Rev 0



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

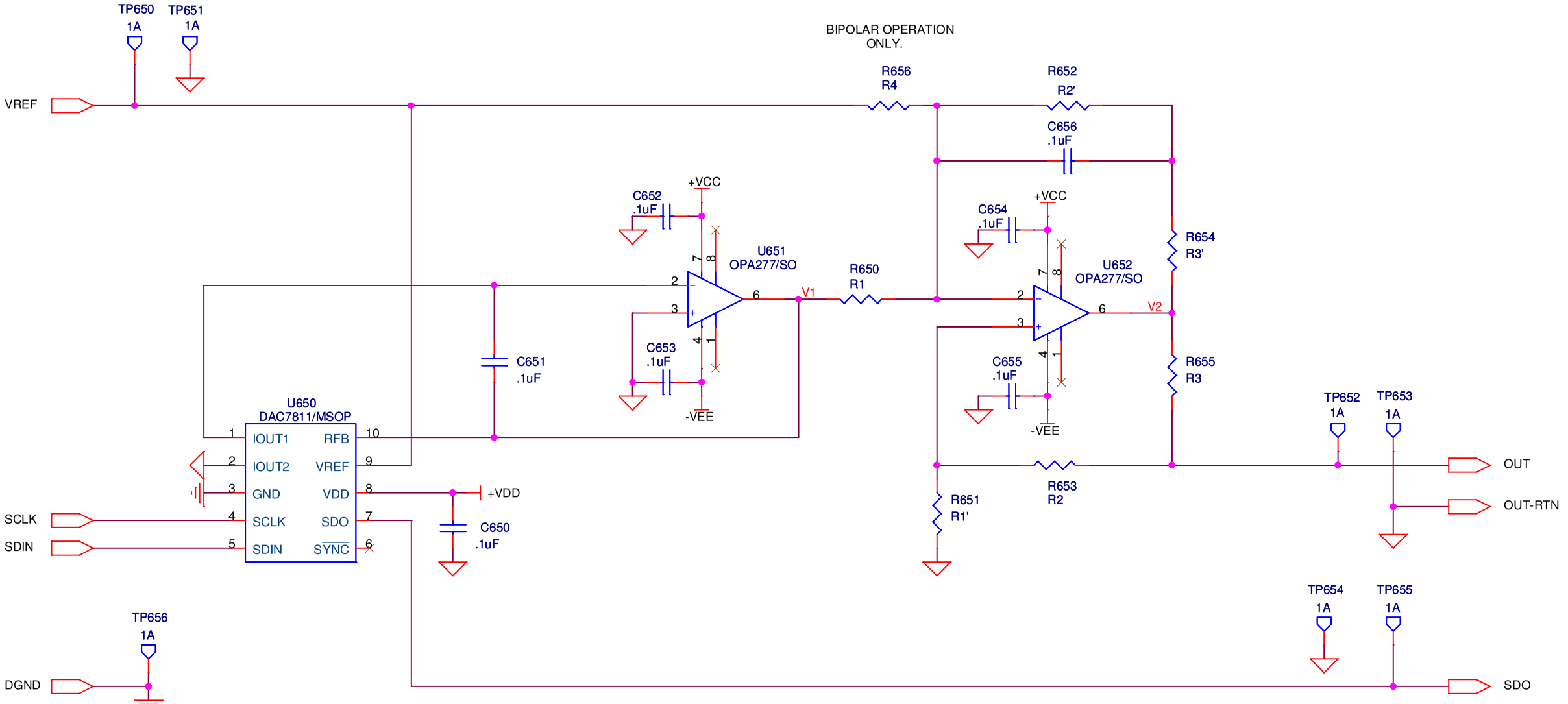
VOLTAGE OUTPUT BIPOLAR:

R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

$Iout_{max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 23 of 37 Rev 0



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

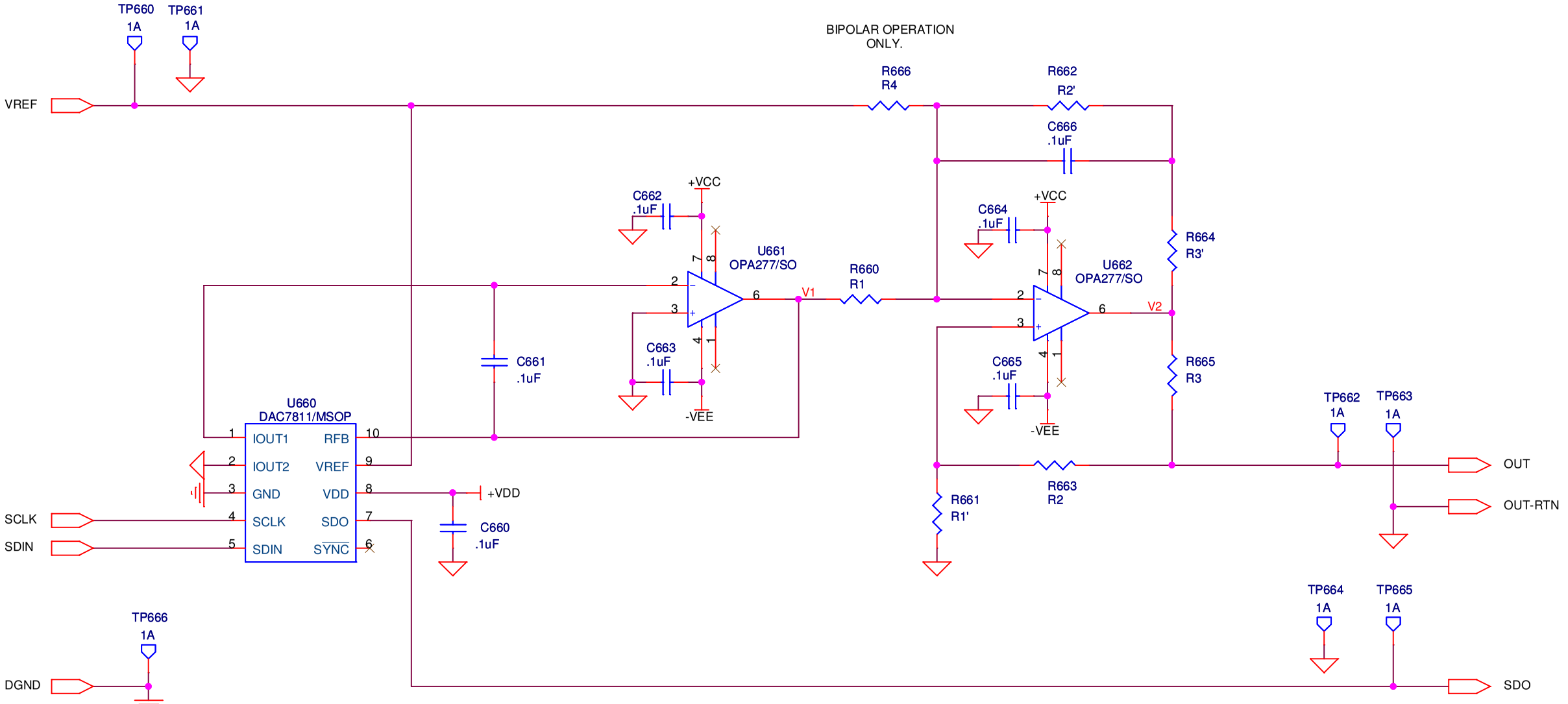
VOLTAGE OUTPUT BIPOLAR:

R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

$Iout_{max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 24 of 37 Rev 0



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

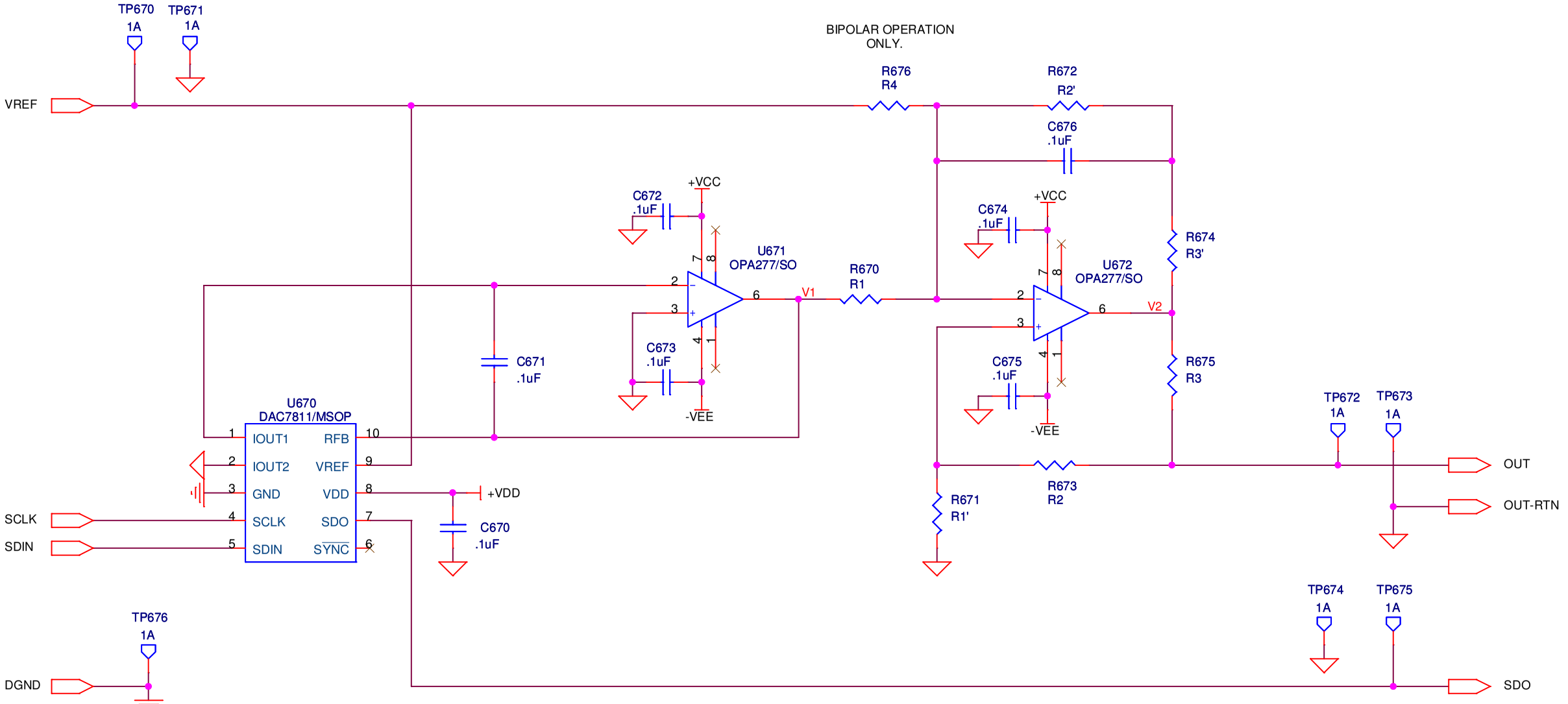
VOLTAGE OUTPUT BIPOLAR:

R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

$Iout_{max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 25 of 37 Rev 0



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

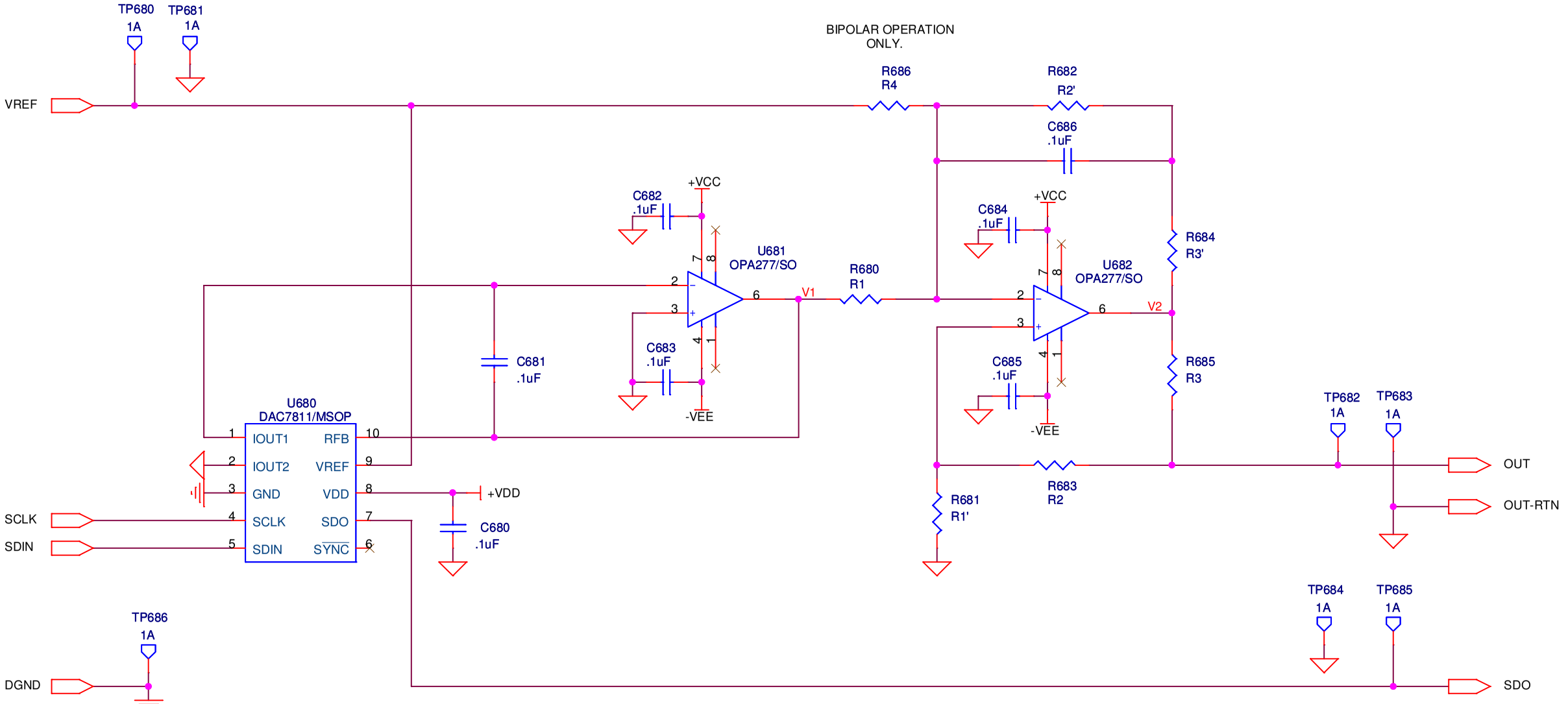
VOLTAGE OUTPUT BIPOLAR:

R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

$Iout_{max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 26 of 37 Rev 0



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

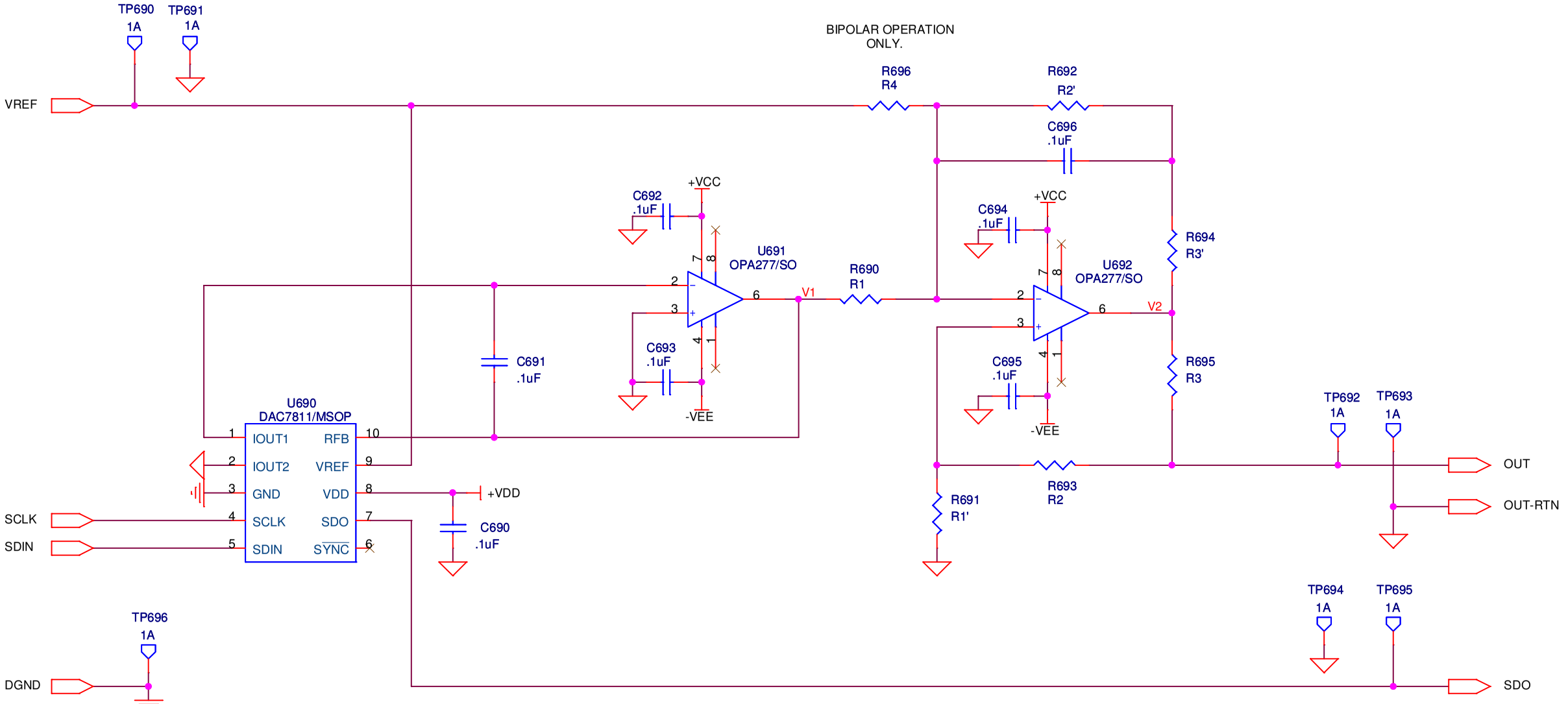
VOLTAGE OUTPUT BIPOLAR:

R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

$I_{out\,max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 27 of 37 Rev 0



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

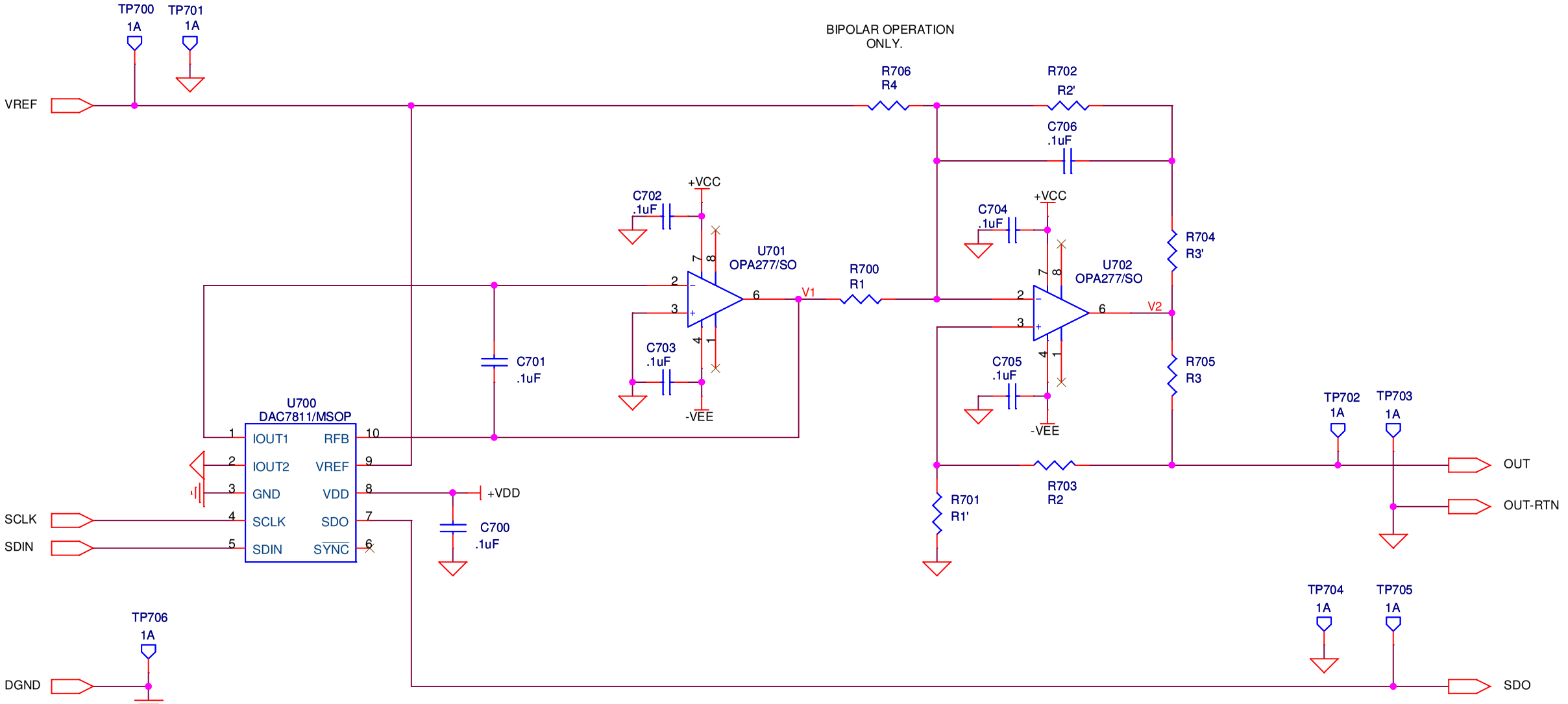
VOLTAGE OUTPUT BIPOLAR:

R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

$Iout_{max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 28 of 37 Rev 0



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

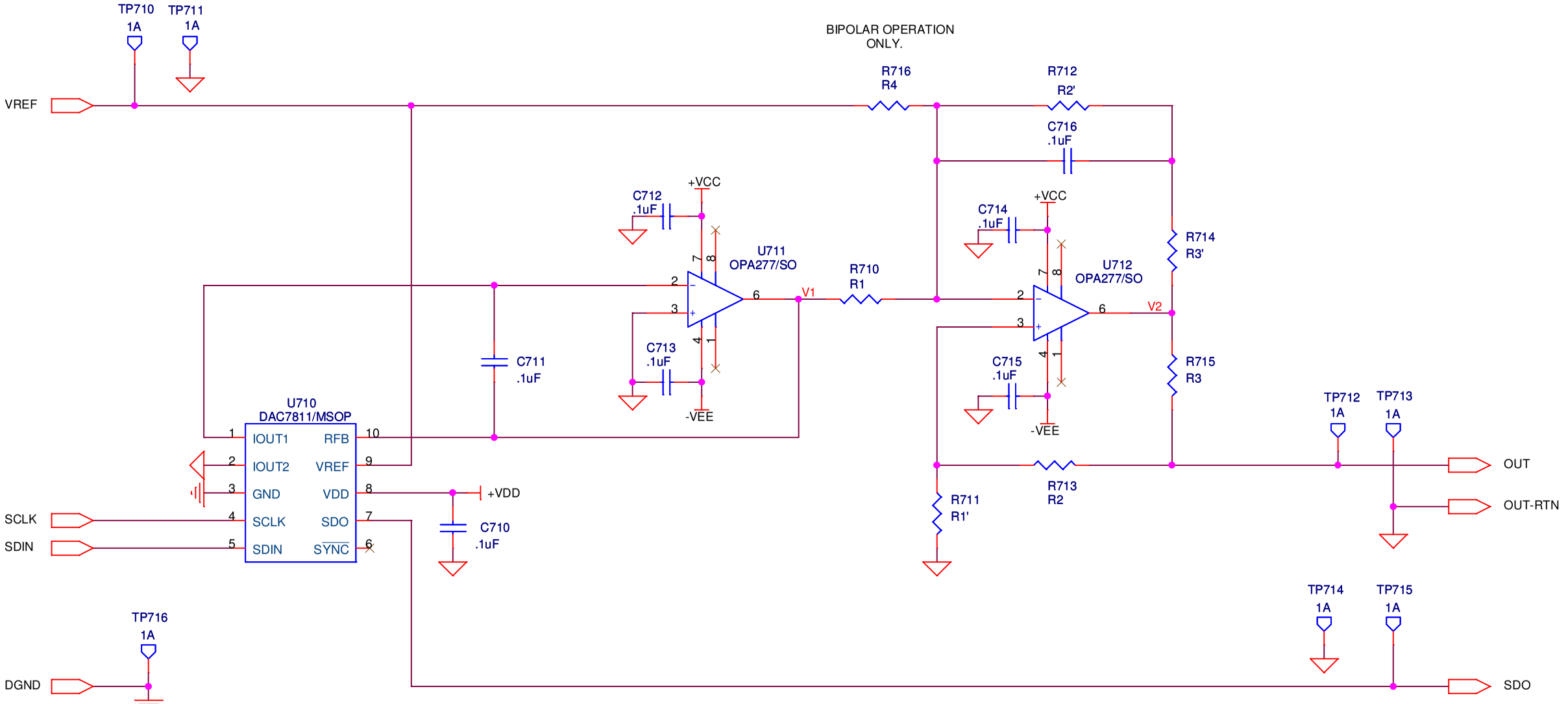
VOLTAGE OUTPUT BIPOLAR:

R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

$Iout_{max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 29 of 37 Rev 0



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

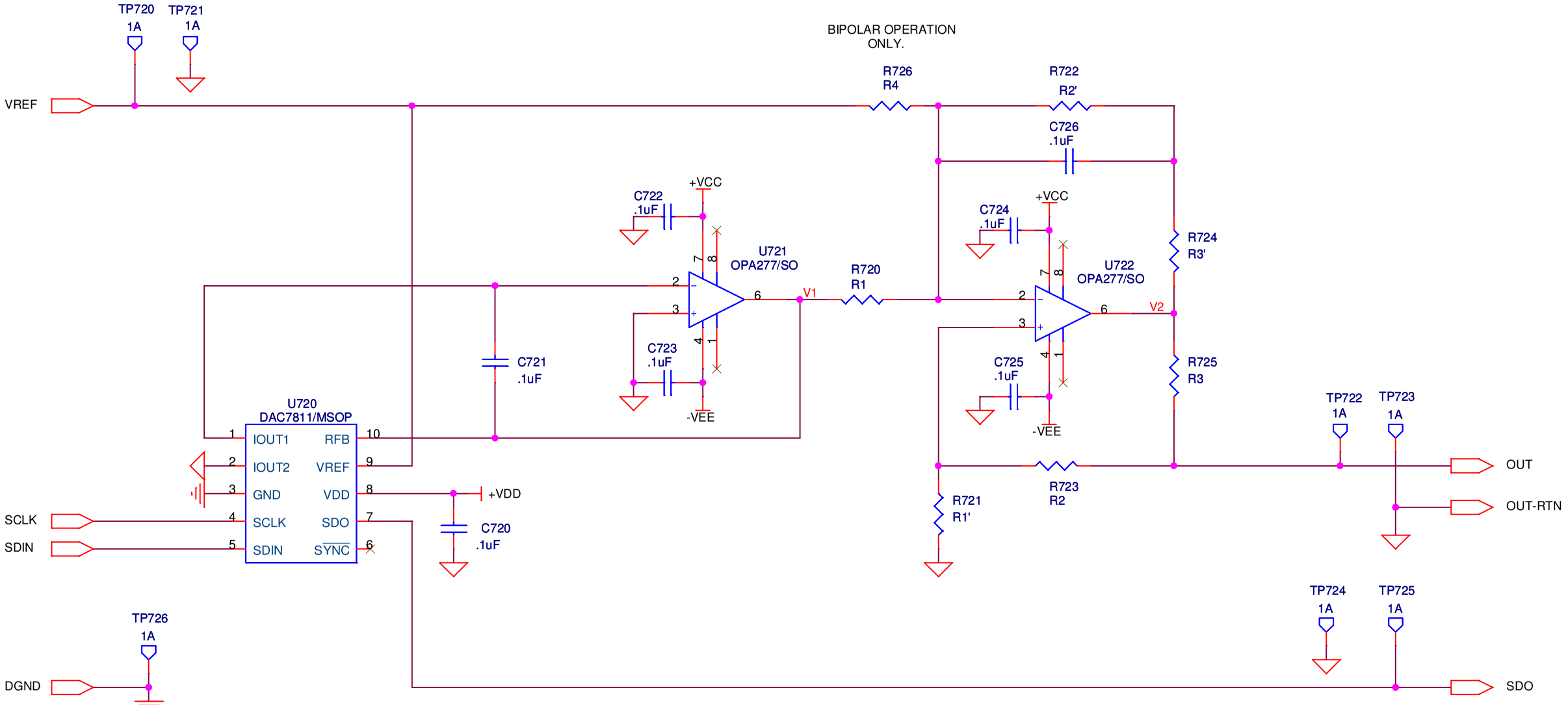
VOLTAGE OUTPUT BIPOLAR:

R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

$Iout_{max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 30 of 37 Rev 0



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

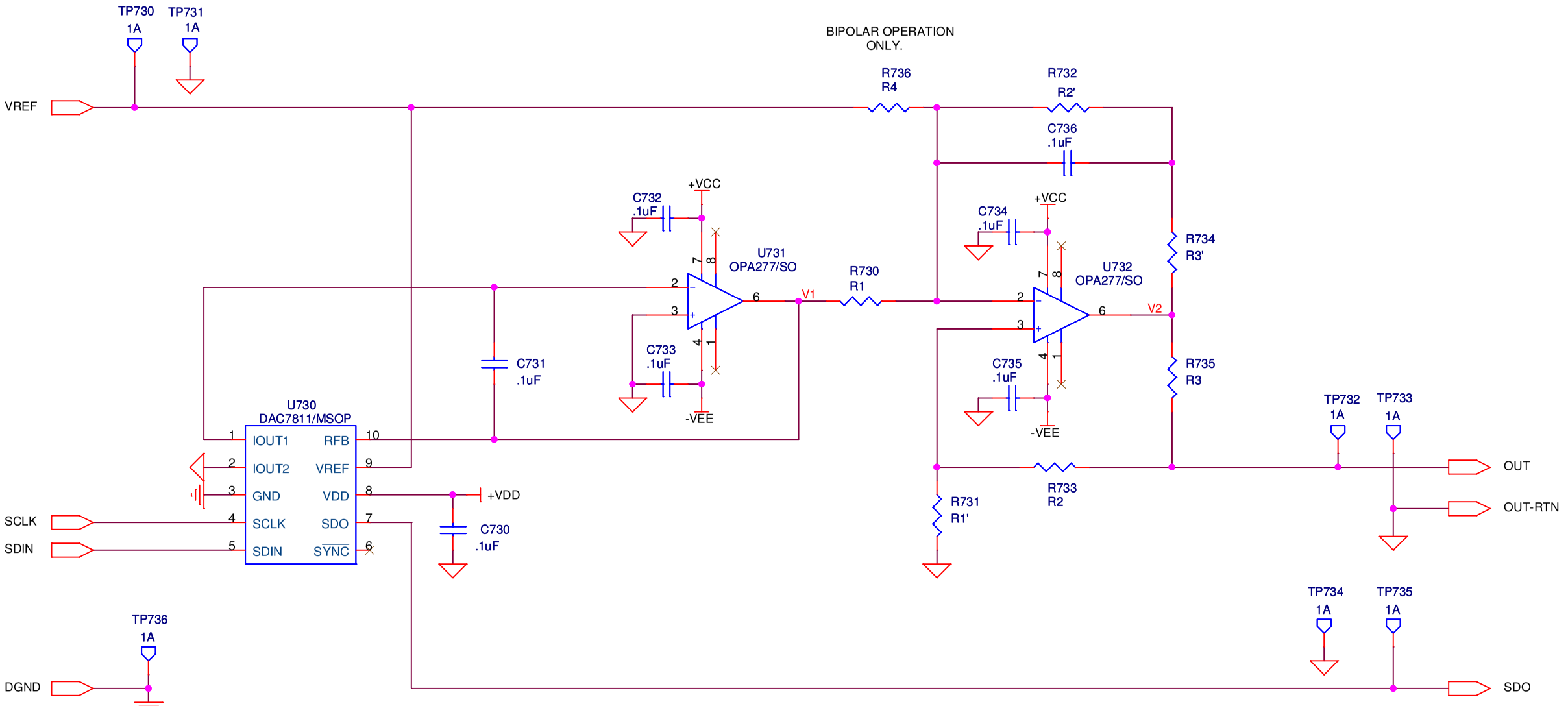
VOLTAGE OUTPUT BIPOLAR:

R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

$Iout_{max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 31 of 37 Rev 0



12 BIT CURRENT DAC

THIS DAC CHANNEL CAN BE CONFIGURED FOR VOLTAGE ON CURRENT OUTPUT DEPENDING ON THE VALUES OF THE RESISTORS LOADED. SEE BELOW FOR SUGGESTED VALUES.

CURRENT OUTPUT:

R1 =R1' IS 150K
R2 = R2' IS 15K
R3 = R3' IS 50 OHMS
R4 = DO NOT LOAD (DNL)

I_{Omax} = Vref x 0.002
Vref = +/-5V
I_{Omax} = +/-10mA

OR

R3 = R3' IS 500 OHMS
I_{Omax} = +/-1mA
COMPLIANCE = +/-VCC
-1.2V = +/-6.8V

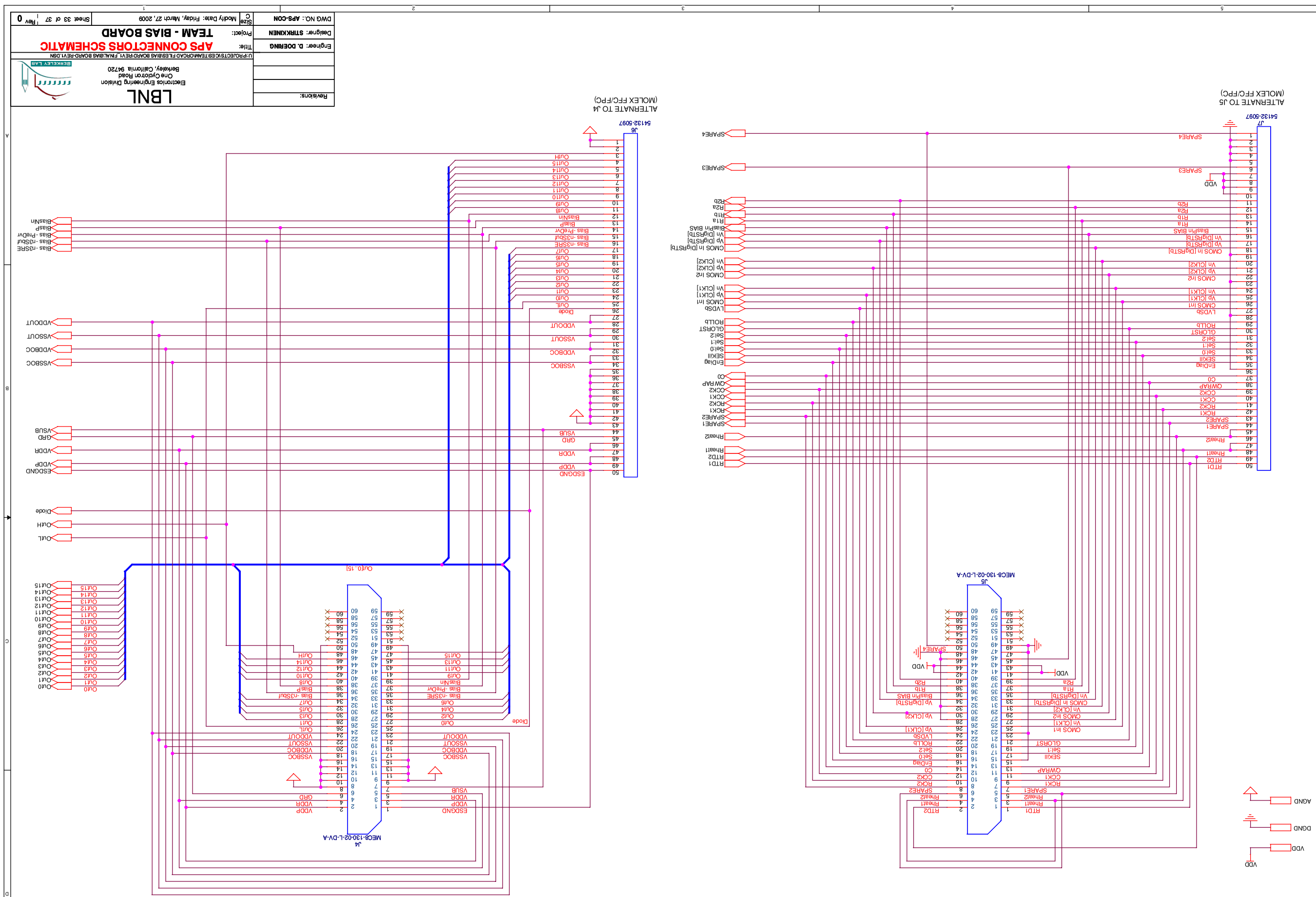
VOLTAGE OUTPUT BIPOLAR:

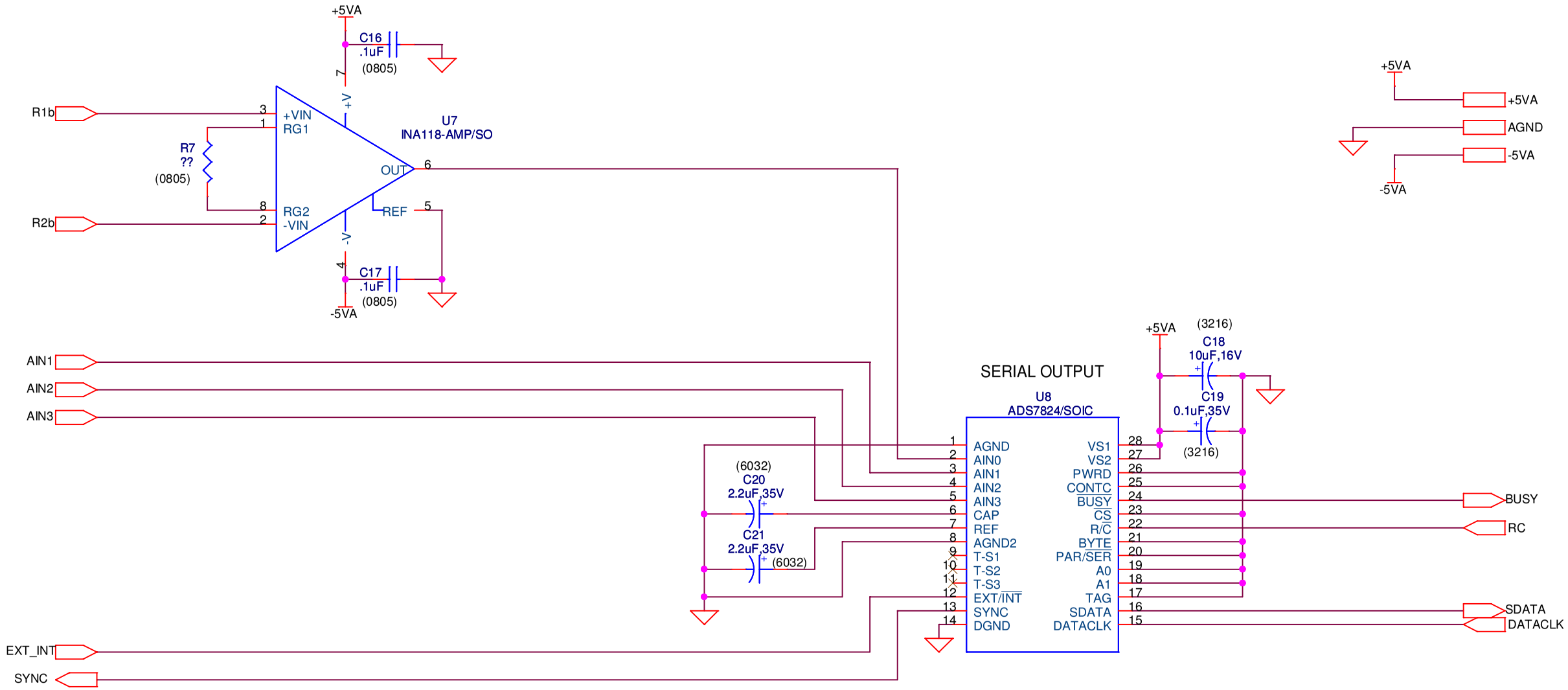
R1 IS 5K
R2' = R4 IS 10K
R1' = R2 = R3' = R3 IS 0 OHMS

Vref = +5V
Vout = +/-5V

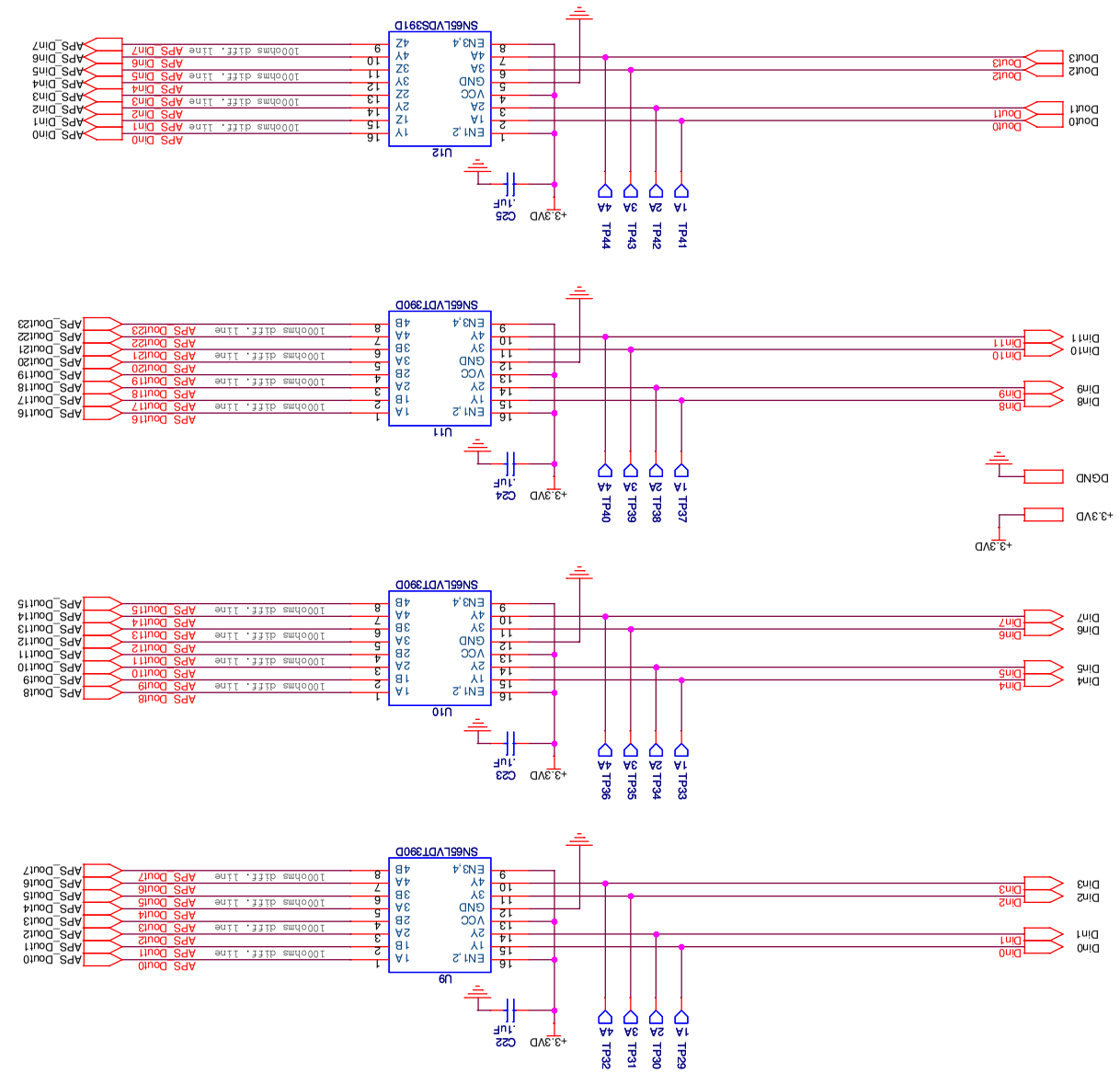
$Iout_{max}$ = 35mA

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720		
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN		
Engineer: D. DOERING	Title: DAC CIRCUIT (1 OF 13)		
Designer: STIRKKINEN	Project: TEAM - BIAS BOARD		
DWG NO.: DAC	Size B	Modify Date: Friday, March 27, 2009	Sheet 32 of 37 Rev 0


ALTERNATE TO J4
(MOLEX FFC/FPC)
5432-5097
J6
1 SPARE4
2
3 OUtH
4 OUt15
5 OUt14
6 OUt13
7 OUt12
8 OUt11
9 OUt10
10 OUt9
11 OUt8
12 BiasNIn
13 BiasP
14 Bias -PreDvr
15 Bias -n3Sduf
16 Bias -n3SRE
17 OUt7
18 OUt6
19 OUt5
20 OUt4
21 OUt3
22 OUt2
23 OUt1
24 OUt0
25 OUtL
26 Diode
27
28 VDDOUT
29
30 VSSOUT
31
32 VDDBOC
33
34 VSSBOC
35
36
37
38
39
40
41
42
43
44 VSUB
45 GRD
46
47 VDDR
48
49 VDDP
50 ESDGND
OUt[0..15]
J4
MEC8-130-02-L-DV-A
ESDGND
VDDP
VDDR
GRD
VSUB
VDDBOC
VSSBOC
VDDOUT
VSSOUT
VDDBOC
VSSBOC
OUt0
OUt1
OUt2
OUt3
OUt4
OUt5
OUt6
OUt7
OUt8
OUt9
OUt10
OUt11
OUt12
OUt13
OUt14
OUt15
OUtL
OUtH
Diode
Bias -n3SRE
Bias -n3Sduf
Bias -PreDvr
BiasP
BiasNIn
ALTERNATE TO J5
(MOLEX FFC/FPC)
5432-5097
J7
1 SPARE4
2
3
4
5
6 SPARE3
7 VDD
8
9
10
11 RTD1
12 RTD2
13 RTD
14 RCK2
15 RCK1
16 CCK2
17 CCK1
18 CWRAP
19 C0
20 SPARE2
21 Rheat2
22 Rheat1
23 SPARE1
24 RCK2
25 RCK1
26 CCK2
27 CCK1
28 CWRAP
29 C0
30 EnDiag
31 SEKill
32 Sel:0
33 Sel:1
34 Sel:2
35 GLORST
36 ROLLb
37 LVDSb
38 CMOS In1
39 Vp [CLK1]
40 Vn [CLK1]
41 CMOS In2
42 Vp [CLK2]
43 Vn [CLK2]
44 CMOS In [DigRSTb]
45 Vp [DigRSTb]
46 Vn [DigRSTb]
47 BiasPin BIAS
48 R1a
49 R1b
50 R2b
51 R2a
52
53
54
55
56
57
58
59 SPARE4
60
J5
MEC8-130-02-L-DV-A
RTD1
RTD2
Rheat1
Rheat2
SPARE1
RCK1
CCK1
CWRAP
SEKill
Sel:1
GLORST
CMOS In1
Vn [CLK1]
CMOS In2
Vp [CLK2]
Vn [DigRSTb]
BiasPin BIAS
R1a
R2a
VDD
SPARE4
RTD2
Rheat1
Rheat2
RCK2
CCK2
CWRAP
C0
EnDiag
Sel:0
Sel:2
LVDSb
Vp [CLK1]
CMOS In [DigRSTb]
Vp [DigRSTb]
R1b
R2b
SPARE3
SPARE4
VDD
AGND
DGND
VDD
Revisions:
LBNL
Electronics Engineering Division
One Cyclotron Road
Berkeley, California 94720
U:\PROJECTS\CES\TEAM\DRCAD FILES\BIAS BOARD\REV_F\FINAL\BIAS BOARD-REV1.DSN
Title: APS CONNECTORS SCHEMATIC
Project: TEAM - BIAS BOARD
Designer: STRKINEN
Engineer: D. DOERING
DWG NO.: APS-CON
Size C
Modify Date: Friday, March 27, 2009
Sheet 33 of 37
Rev 0



Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: **D. DOERING**	Title: **SERIAL OUT CIRCUIT**	
Designer: **STIRKKINEN**	Project: **TEAM - BAIS BOARD**	
DWG NO.: **serial out**	Size B / Modify Date: Friday, March 27, 2009	Sheet 34 of 37 / Rev **0**



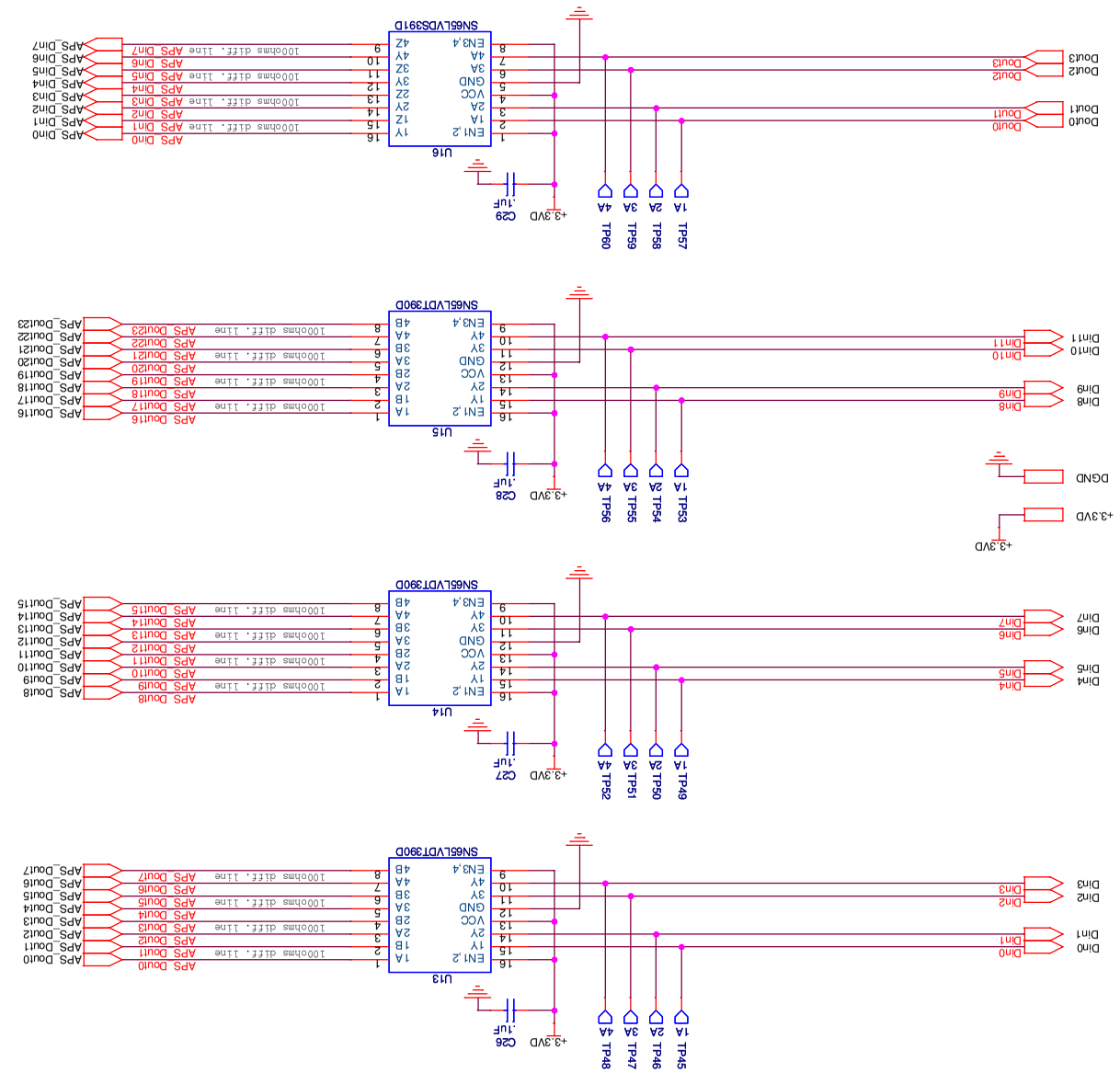
Revisions:	
Engineer: D. DOERING	
Designer: STRKKINEN	
DWG NO.: LVDS	
Size: C	Modify Date: Friday, March 27, 2009

LBNL
Electronics Engineering Division
One Cyclotron Road
Berkeley, California 94720

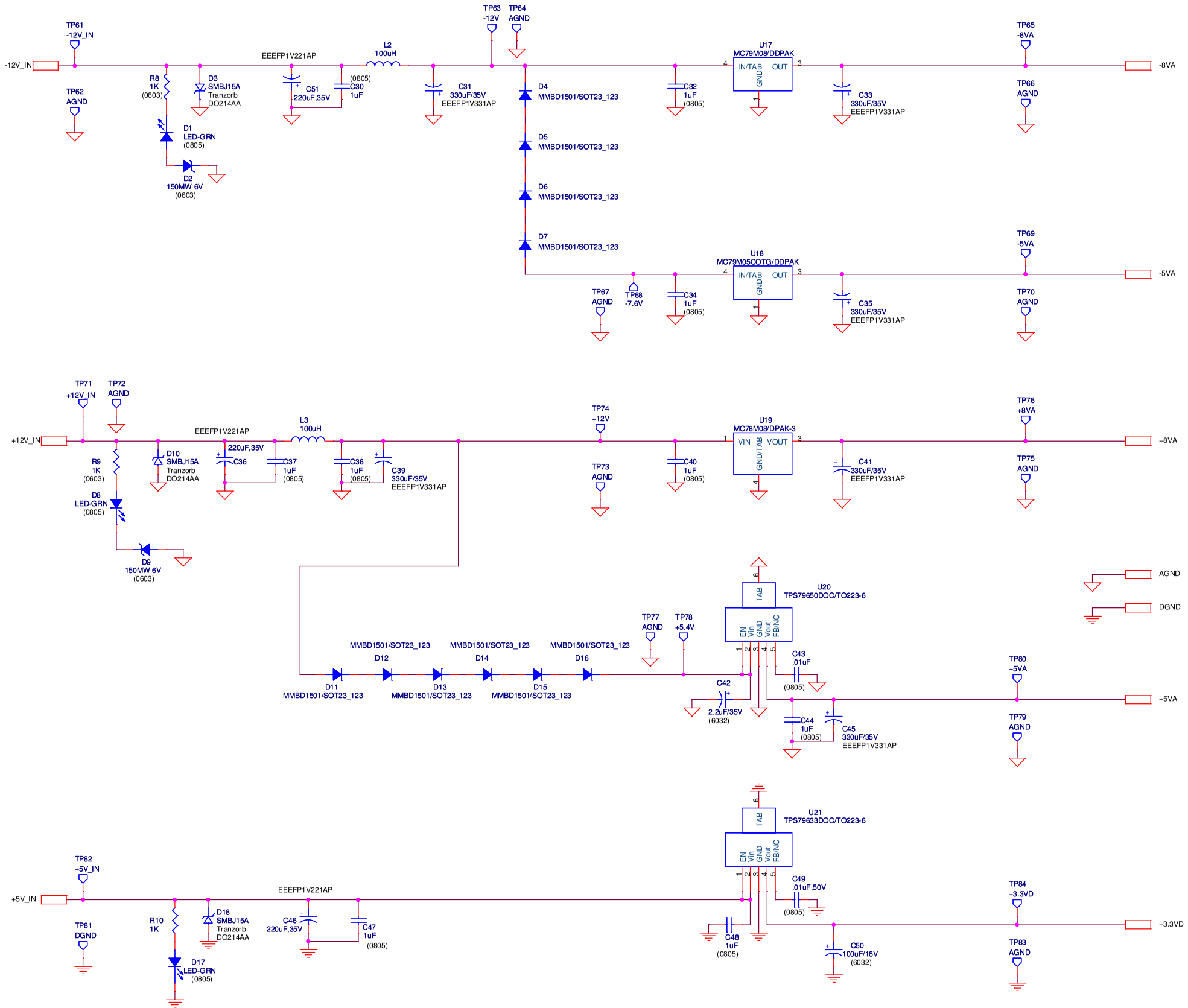
U:\PROJECTS\CES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN

Title: LVDS DRVR/RCVR SCHEMATIC (2)
Project: TEAM - BIAS BOARD

Sheet 35 of 37 | Rev 0



Revisions:	
	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720
U:\PROJECTS\CES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FINAL\BIAS BOARD-REV1.DSN	
Engineer: D. DOERING	Title: LVDS DRVR/RCVR SCHEMATIC (2)
Designer: STRKKINEN	Project: TEAM - BIAS BOARD
DWG NO.: LVDS	Size: C — Modify Date: Friday, March 27, 2009 — Sheet 36 of 37 — Rev 0



Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	U:\PROJECTS\ICES\TEAM\ORCAD FILES\BIAS BOARD\REV1_FIN AL\BIAS BOARD-REV1.DSN	
Engineer: D. DOERING	Title: POWER SUPPLY SCHEMATIC	
Designer: STIRKKINEN	Project: TEAM - BAIS BOARD	
DWG NO.: TOP-OVERALL	Size C | Modify Date: Friday, March 27, 2009	Sheet 37 of 37 | Rev 0