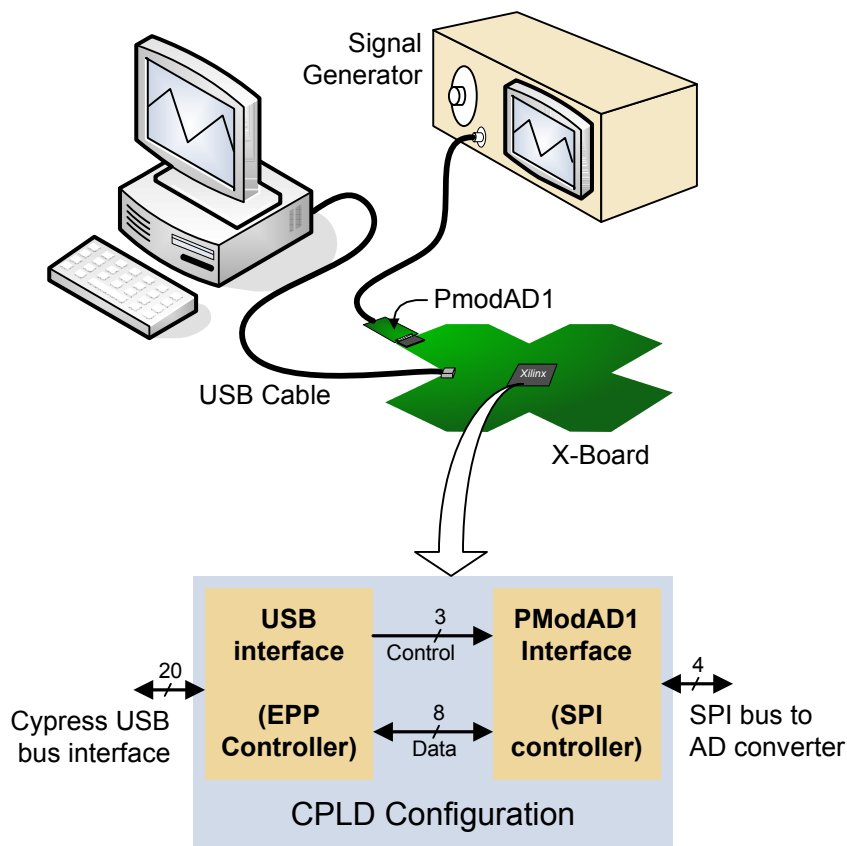


Overview

This reference design demonstrates using the PModAD1 (analog to digital converter) with the X-board to sample and acquire analog signal data.

The X-board is a CPLD demonstration board based on a Xilinx CoolRunner-2 CPLD. The PModA/D1 is a Digilent Peripheral Module board that contains two National Semiconductor 1MSPS ADCS7476 12-bit A/D converters. Each A/D converter circuit includes protection networks and anti-alias filters.

Digilent's Adept software is used to program the reference design into the CPLD, and to move sample data from the X-board to the PC. Please refer to the Reference Manuals listed below for more detailed information.



References

Digilent X-board Reference Manual Schematic
Digilent PModAD1 Reference Manual and Schematic
Digilent Adept Reference Manual
Digilent Application Note AN0040 "Digilent Asynchronous Parallel Interface"
National Semiconductor ADCS7476 Data sheet
Xilinx CoolRunner-2 Data Sheet

Set-up

This reference design requires a PC running the Xilinx ISE or WebPack tools, Digilent's Adept software, an X-board, a Digilent PModAD1, a signal source, and some hook-up wire to connect the signal source to the PModAD1.

Set the clock frequency select jumper (J11) on the X-board to select 100KHz.



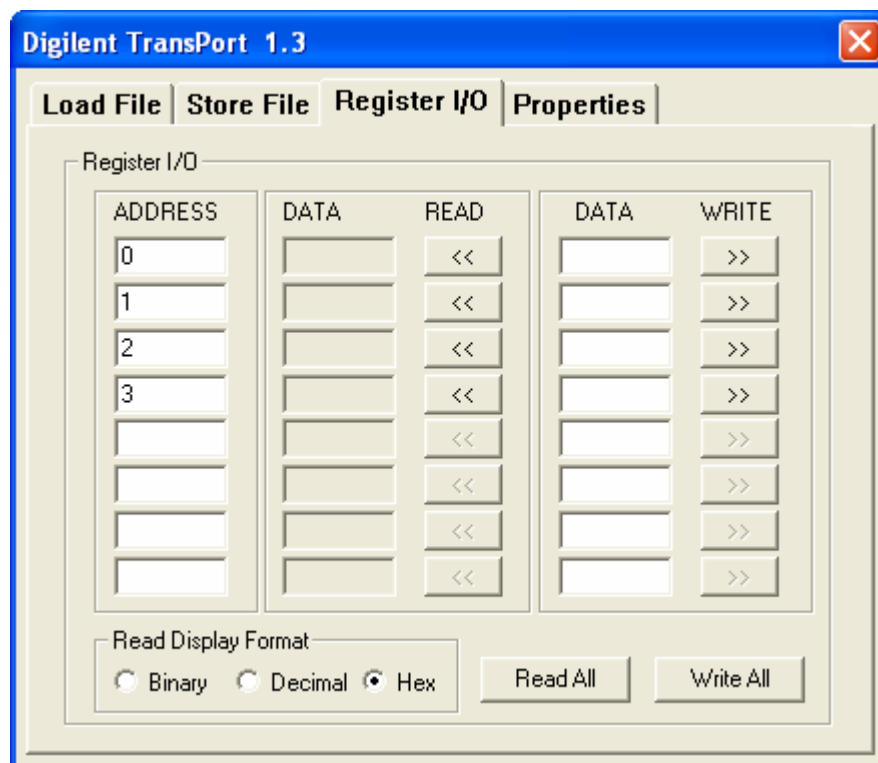
Description

This reference design is composed of two major blocks: a USB interface that implements registers in the CPLD that Adept can read and write; and a SPI controller that can read and write data from the A/D converter on the PModAD1. A simple 8-bit control bus, the Digilent asynchronous parallel interface bus (based on the Enhanced Parallel Port, or EPP, specification), is used to move data internally between these two blocks.

The USB interface block works with firmware in the USB controller to implement four read-only 8-bit registers in the CPLD. Registers can be read from the Transport application that is available as a part of Digilent's freely available Adept software (alternatively, the API's available through Adept can be used to create custom applications to access CPLD registers). Register reads are communicated from the USB interface block to the SPI controller using Digilent's asynchronous parallel interface bus. Bus timings and signal definitions closely follow the EPP specification; please see application note AN0040 available at www.digilentinc.com for a detailed description of bus timing and control.

Since the USB interface is based on 8-bit registers, and sampled data from the PModAD1 is 12 bits, Transport must perform two consecutive reads to transfer all 12 bits from each A/D channel. Reading the first register of the pair assigned to a channel will start a new conversion for that channel. The CPLD uses the read request from Transport to start a new conversion by driving the SPI bus to the A/D converter as required. The read request of the first register will not be completed until the A/D conversion is completed (about 100us). Once the conversion is complete and the first register read is complete, the remaining four bits in the second register can be read immediately. The SPI controller in the CPLD uses SPI mode 0 protocol to transfer data from the A/D converter.

To use the reference design "as is", build a project in the Xilinx tools using the VHDL and UCF files that are downloaded from the Digilent website as a part of this reference design. Attach the PModAD1 to the J1 port on the X-board, and attach a signal source to the A/D inputs. Program the CPLD on the X-board with the JED file created from the downloaded source files, and then run Digilent's Transport application (available as a part of the Adept software freely available at the Digilent website). Select the Register I/O tab, and add register addresses 1-4 to the address fields as shown. Clicking on the Read button for register 0 will start a conversion on channel A, and deliver an 8-bit data element (the lower 8 bits of the sample) to the data register window adjacent to address 0. The upper four bits of the sample can be acquired





by reading address 1. Data can be transferred from A/D channel B in the same fashion using addresses 2 and 3.

Note that user-written, custom applications can acquire sample data from the X-Board / PModAD1 hardware using the API's available as a part of Adept.

The following table summarizes the address definitions used in the reference design.

| Address | Op | Channel | Data | Comments |
|---------|------|---------|------|---|
| 0 | Read | A | LSB | Read returns the lower byte of Channel A data |
| 1 | Read | A | MSB | Read returns the upper 4 four bits of Channel A (in the 4 LSBs) |
| 2 | Read | B | LSB | Read returns the lower byte of Channel B data |
| 3 | Read | B | MSB | Read returns the upper 4 four bits of Channel B (in the 4 LSBs) |