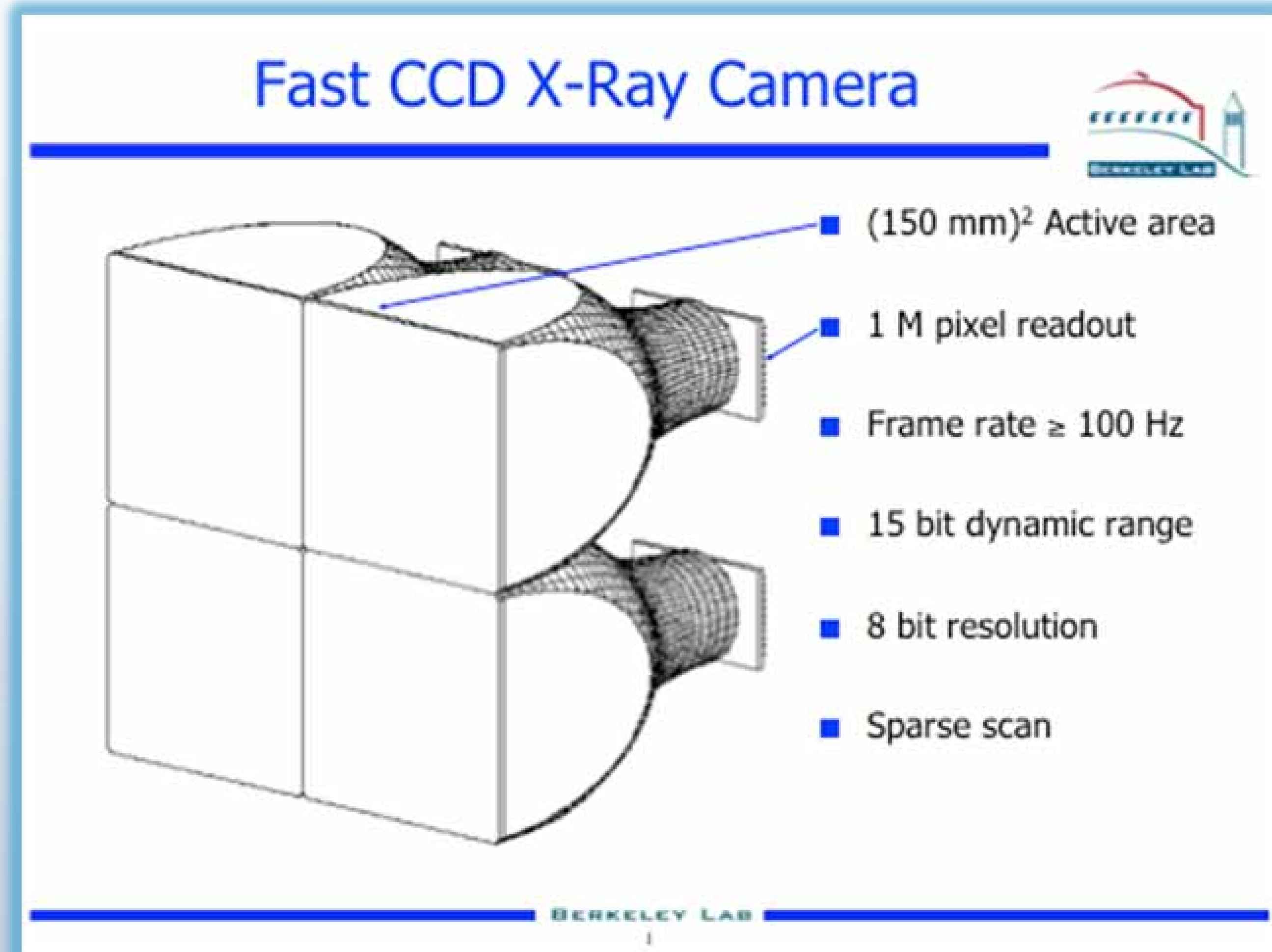
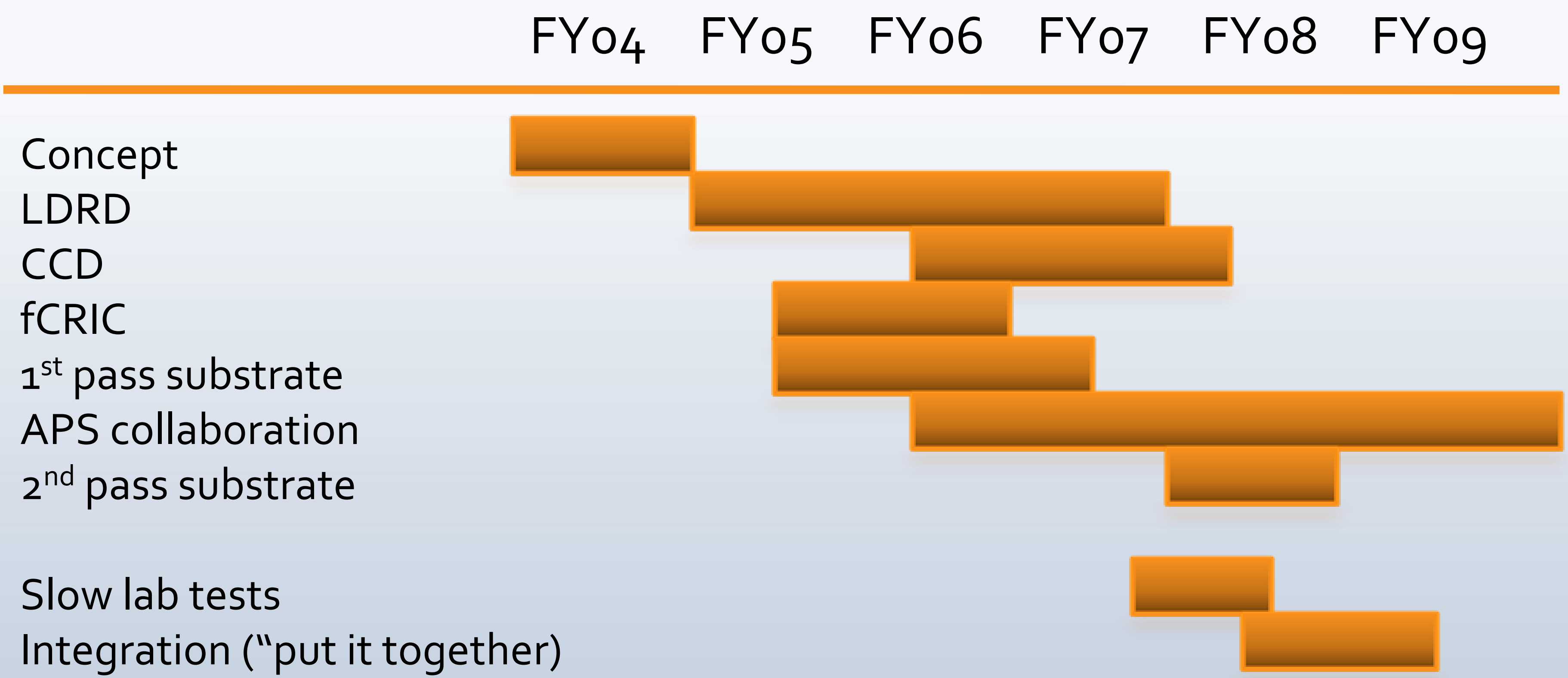
FastCCD – Status Jan. '09

- Hardware
- Performance
- Future steps

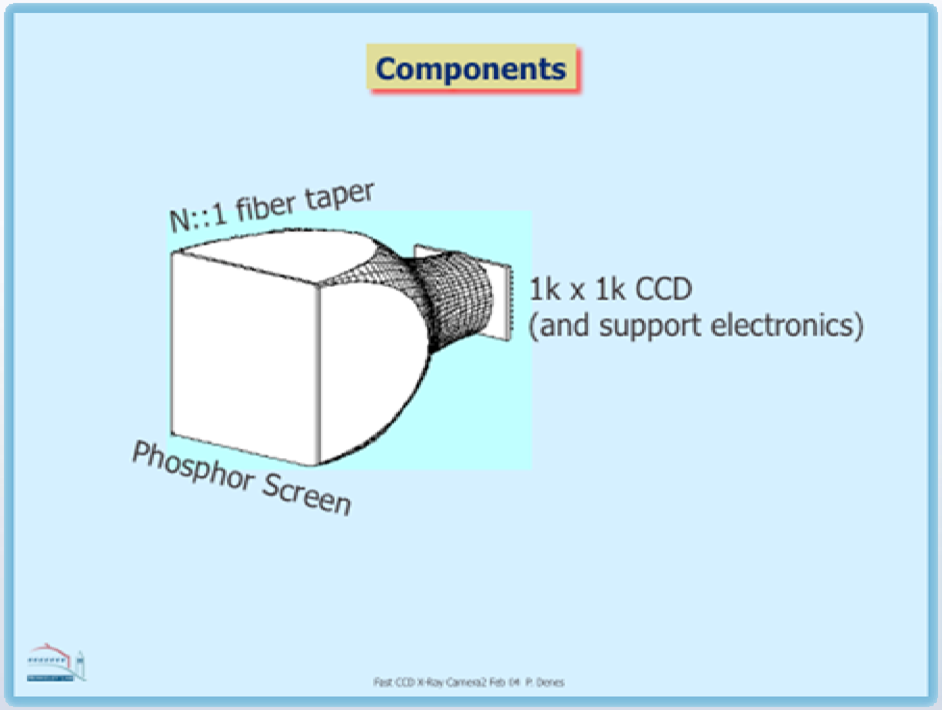


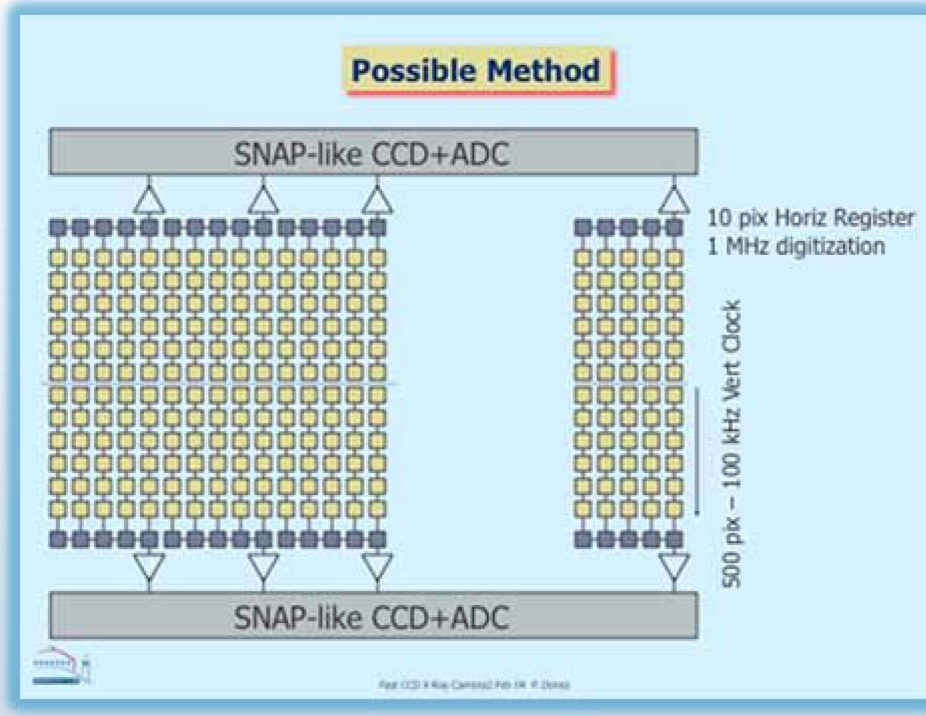
Concept – late 2003 / early 2004

TIMELINE


FY04
FY05
FY06
FY07
FY08
FY09
Concept
LDRD
CCD
fCRIC
1st pass substrate
APS collaboration
2nd pass substrate
Slow lab tests
Integration ("put it together)

Concept - continued





- 1k CCD "building block"
- 1::1 to 2.5::1 taper
- Fast phosphor

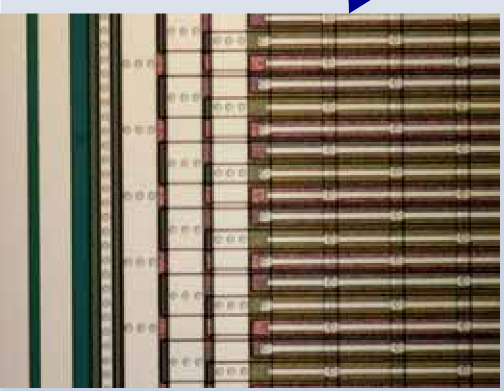
- Custom readout chip based on CRIC
- Commercial multi-port CCD

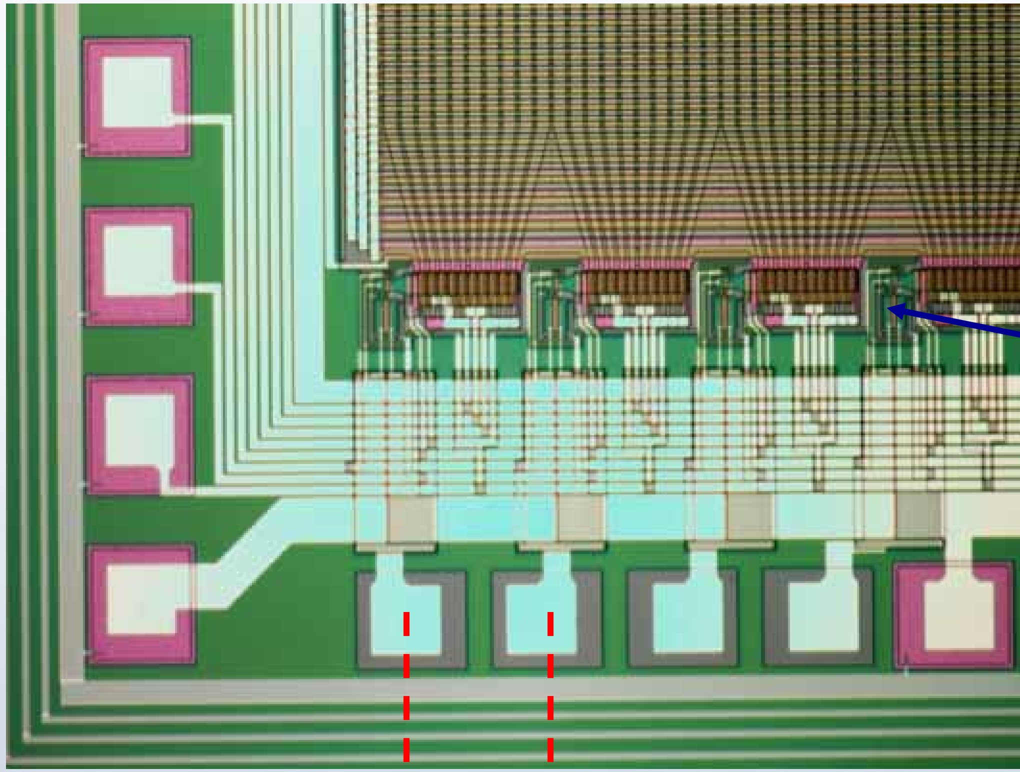
"Commercial multi-port CCD" ??

- No such CCD
- Make our own – use LBNL CCD process
  - Thick, fully-depleted Si → possibility of direct x-ray detector
- FY05 – FY07 LDRD
  - Develop fCRIC readout ASIC
  - Develop multi-port CCD
    - $-limited to 480 x 480

(almost) Column-Parallel CCD

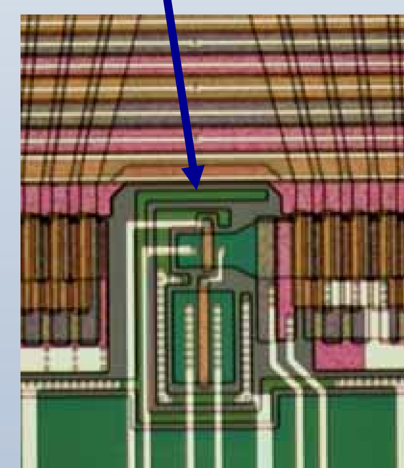
Mini-SR with taper
Metal strapping





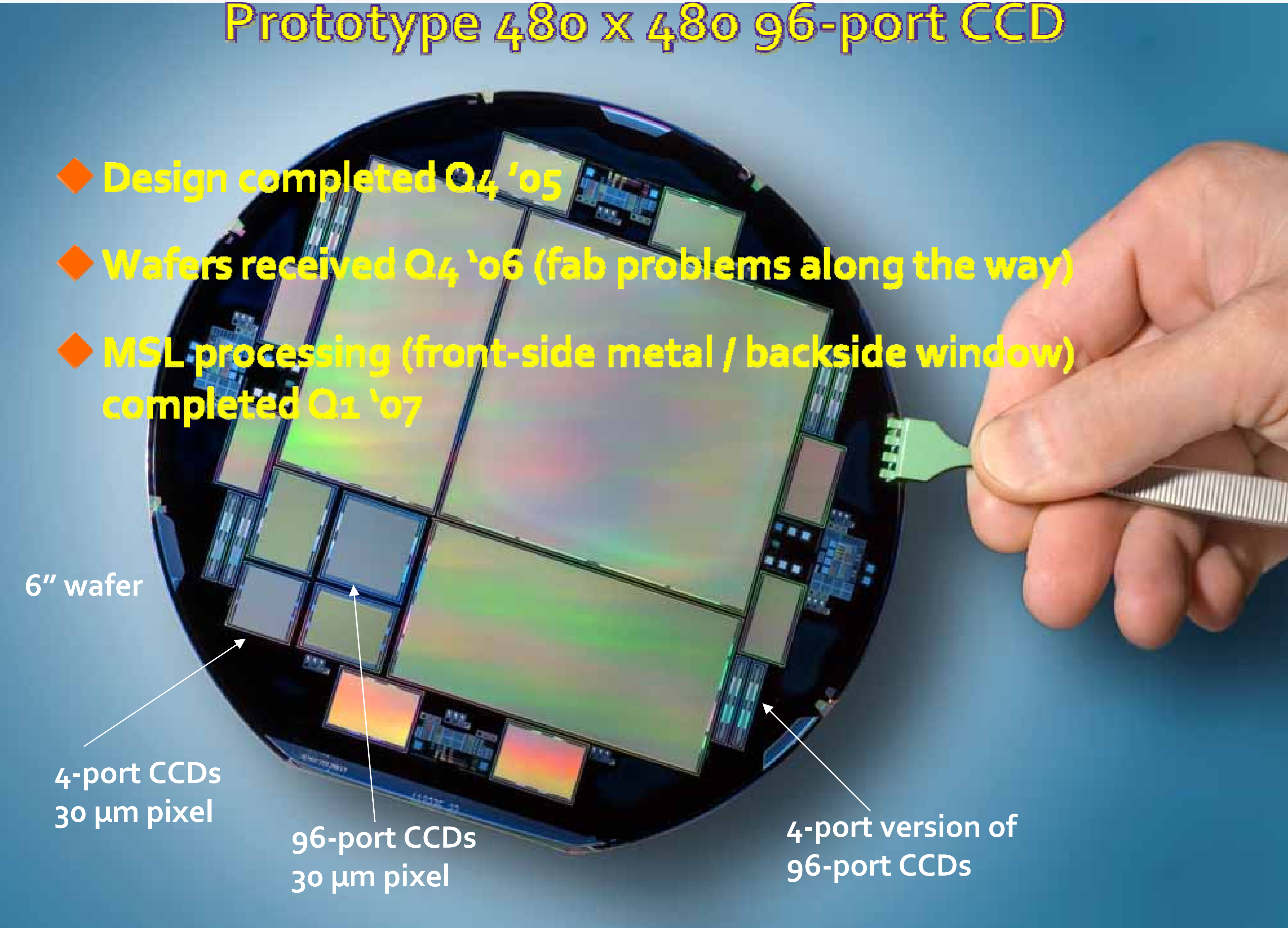
Constant
Area
Taper
Mini-shift reg.
Output stage

~300 µm pitch
bond pads
(wire-bondable)

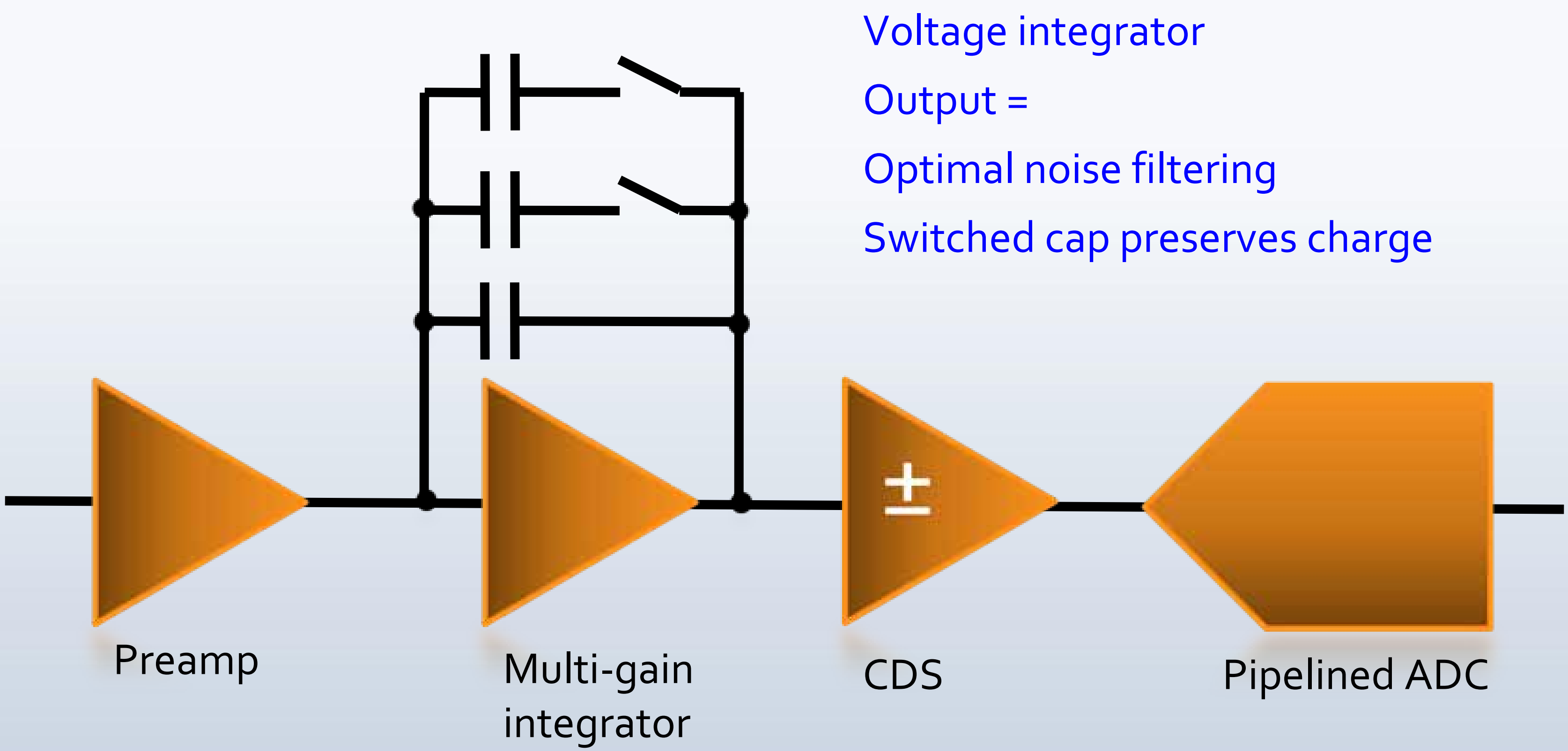


Prototype 480 x 480 96-port CCD

- Design completed Q4 '05
- Wafers received Q4 '06 (fab problems along the way)
- MSL processing (front-side metal / backside window) completed Q1 '07

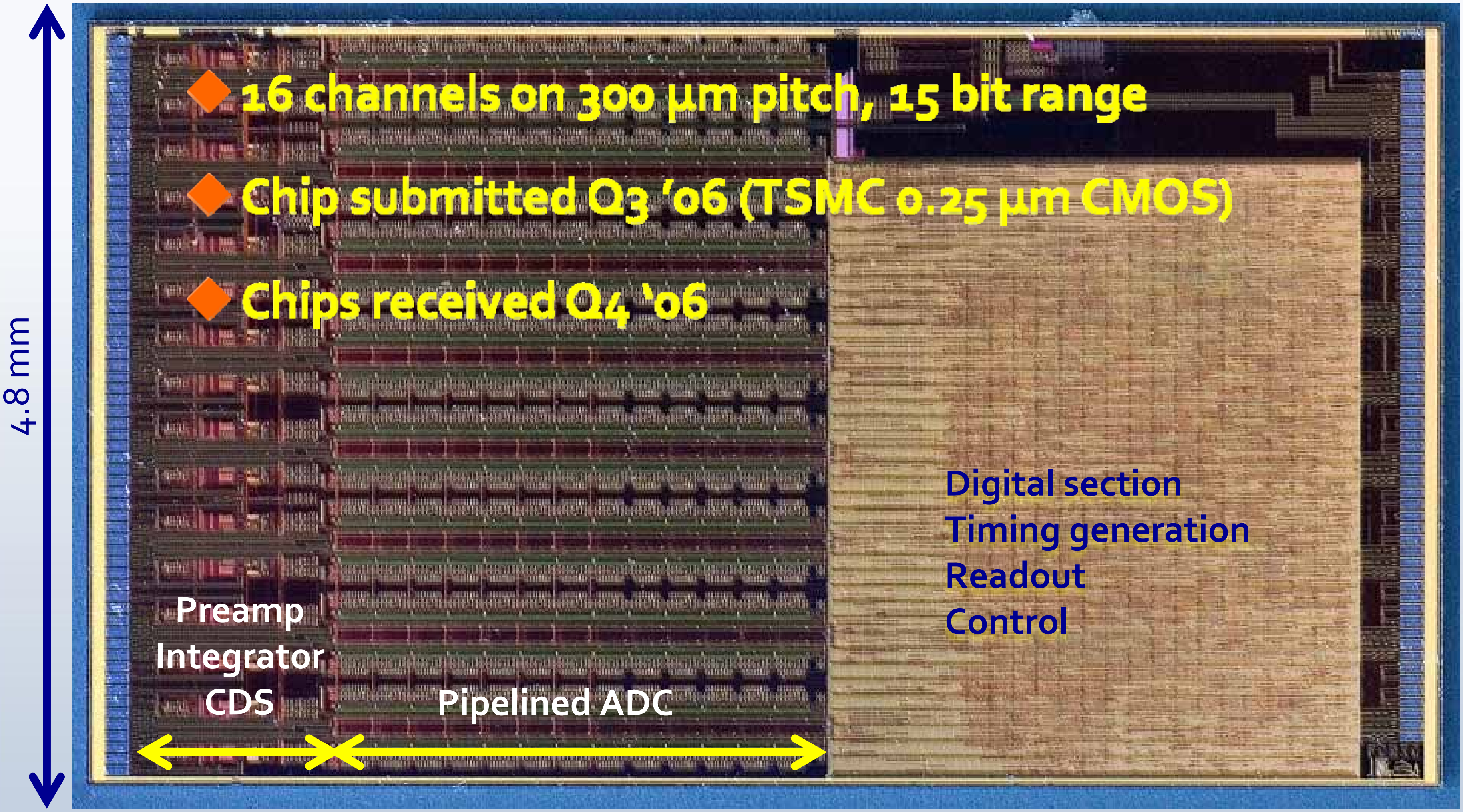


CCD Readout Based on *CRIC*



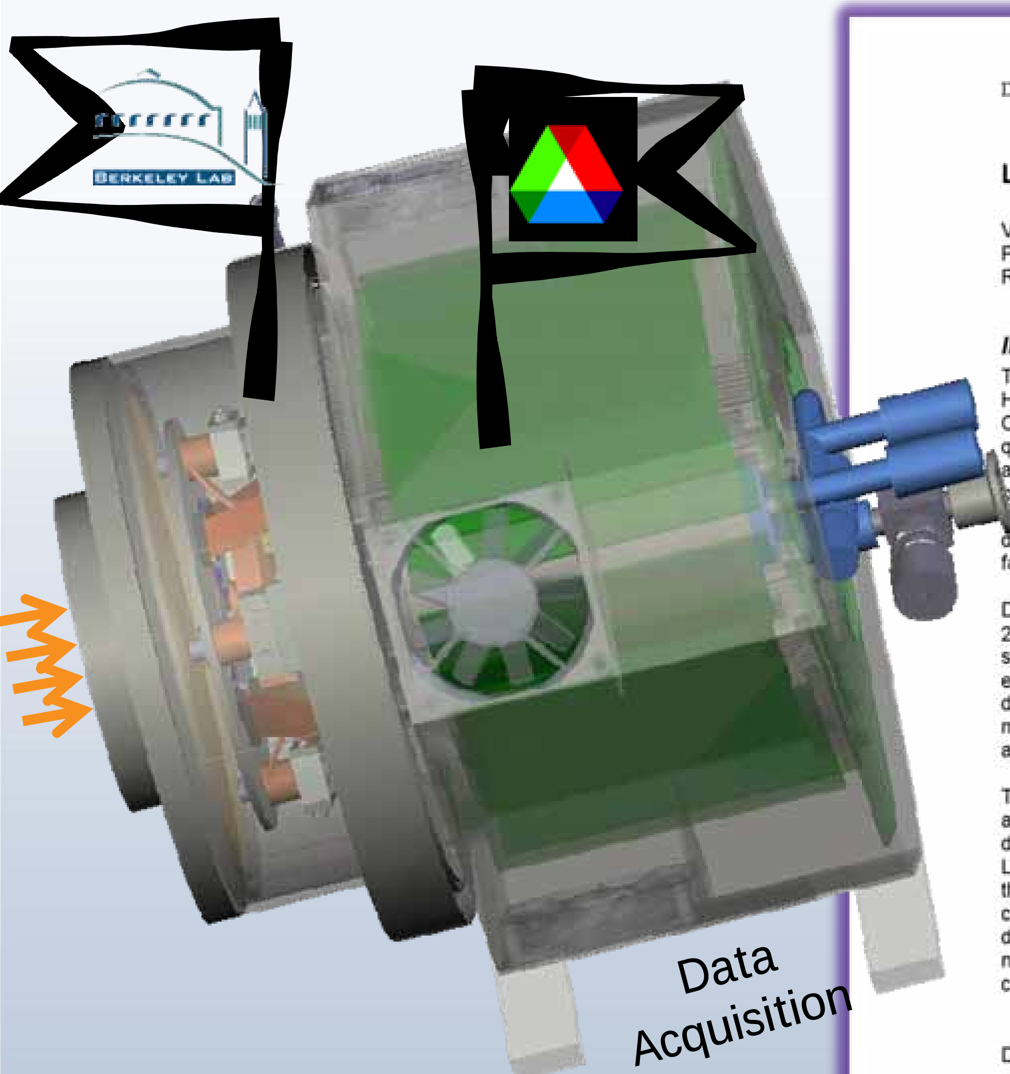
- Gain 8, 2, 1
- 12 + 1 bit ADC
- Covers 15-bit dynamic range
- Quantization error always < photostatistics

fCRIC



Custom CCD readout and ADC chip

Formalize Berkeley / Argonne Collaboration Jan. '06



DRAFT DOCUMENT January 12, 2006

LBL/APS collaboration on x-ray area detectors

Version 1.0
Prepared by: P. Denes, P. Fernandez, John Weizeorick
Reviewed by:

Introduction and Objectives

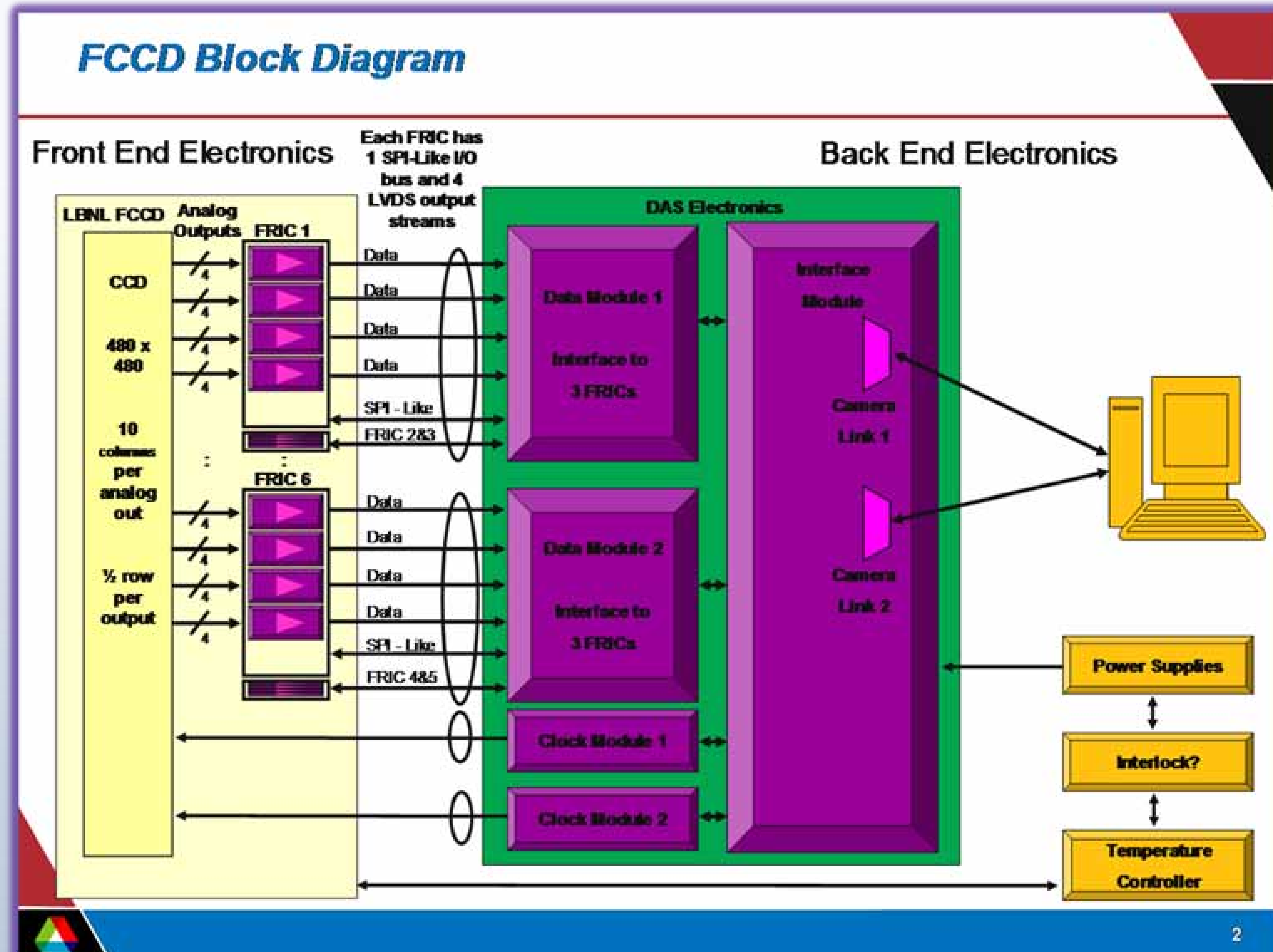
The LBL Experimental Systems and Electronics Engineering groups, headed by H. Padmore and P. Denes, respectively, have an ongoing program designing fast CCD chip for use at synchrotron beam lines. These CCDs will have low noise, quasi column-parallel readout architecture, allowing faster readout times. In addition, the thicker photo-sensitive volume will allow for the possibility of performing direct x-ray detection without a phosphor. In July 2005, S. Ross, a member of the x-ray detector team at the APS, met with H. Padmore and discussed the possibility of collaborating with LBL in the development and fabrication of x-ray detectors based on these fast readout CCD chips.

During meetings between the LBL and APS teams in October and December 2005, it became apparent that LBL and APS have complementary technical strengths. LBL has expertise in IC design and manufacturing, in addition to experience with x-ray phosphors. The APS detector group has expertise in the design and fabrication of CCD-based x-ray detectors, particularly in the opto-mechanics and data acquisition electronics. At the end of these meetings it was agreed that we would work together on developing a Fast CCD x-ray detector.

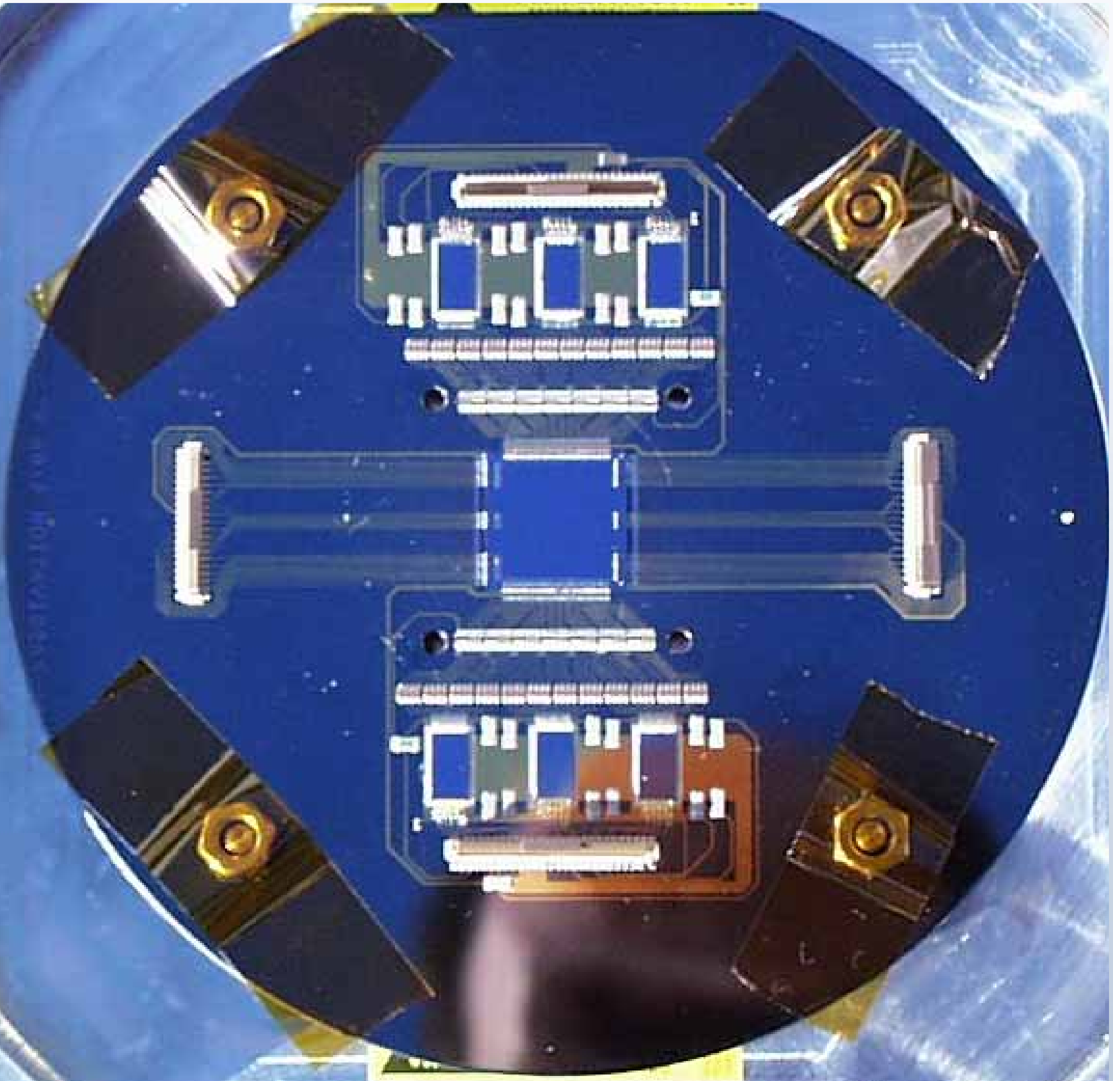
This project is divided into short, medium and long term goals (Phase I, Phase II and Future Projects). At the end of Phase I we will have at least two complete demonstration Fast CCD x-ray cameras, one for LBL and one for APS, using LBL's 480 x 480, quasi column-parallel readout CCD, which APS will deploy to the beam lines. At the end of Phase II, if it is approved, we will have at least two complete Fast CCD x-ray cameras, one for each institution, using an LBL designed 1K x 1K, quasi column-parallel readout CCD. The future projects are not defined and could include Faster/Larger FCCD devices and commercialization of the detectors that we have developed.

Details about the different phases of the project are given in the sections below.

FCCD Readout – J. Weizeorick



1st Pass "Substrate"



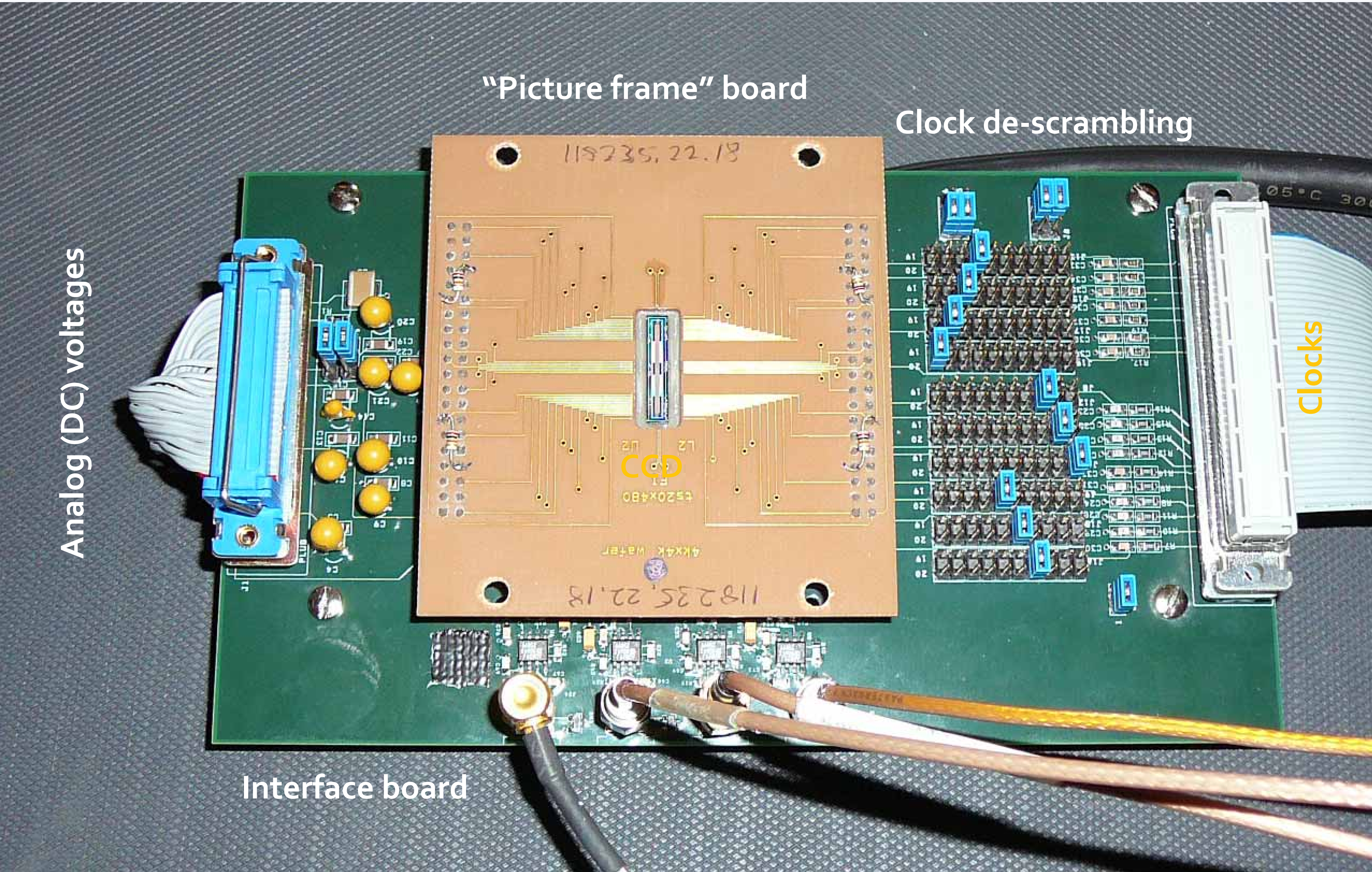
- Idea: Si is a good CTE match for Si
- Use Si substrate (3 mm thick 6" wafer)
- Develop metalization and passivation process
- 1st assembly attempt Q4 '06
- Initial idea: glue. But components too small
- Try solder: ∞ heat sink

~1.5 years ago:

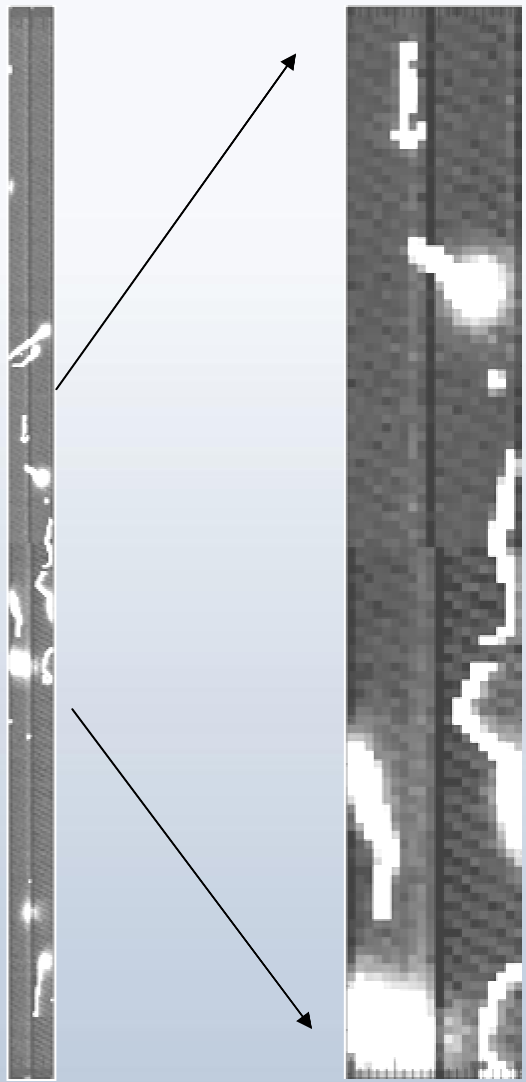
- CCDs arriving from foundry
- Readout chip fabricated and tested
  - Some warts, but minor
- Mechanical model for "substrate"
- Architecture for DAQ

- "Just do it"

Initial Tests at Low Speed with 4-port 20 x 480 CCD

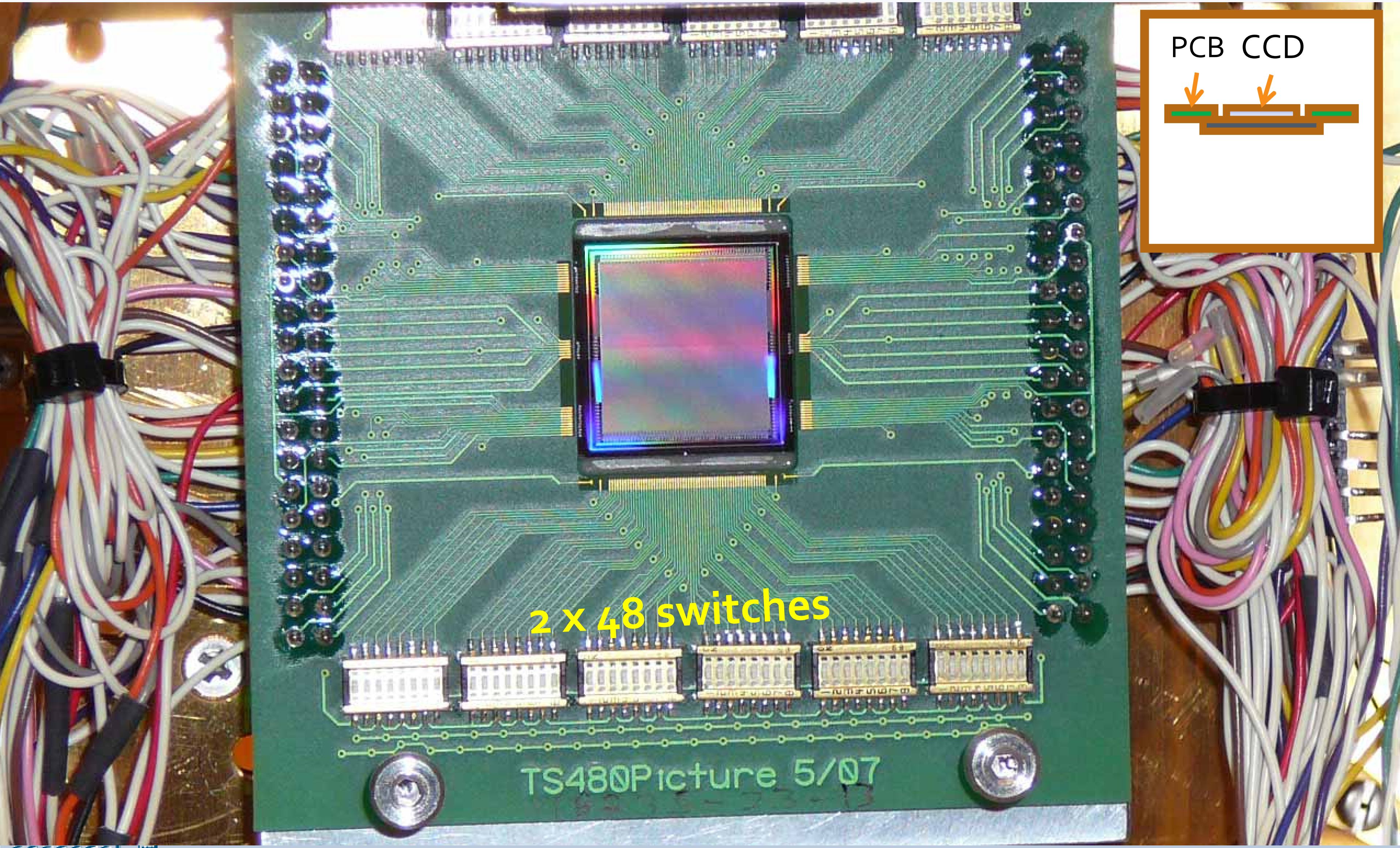


Lab Test – 20 x 480 – 30 Minute Exposure Apr. '07

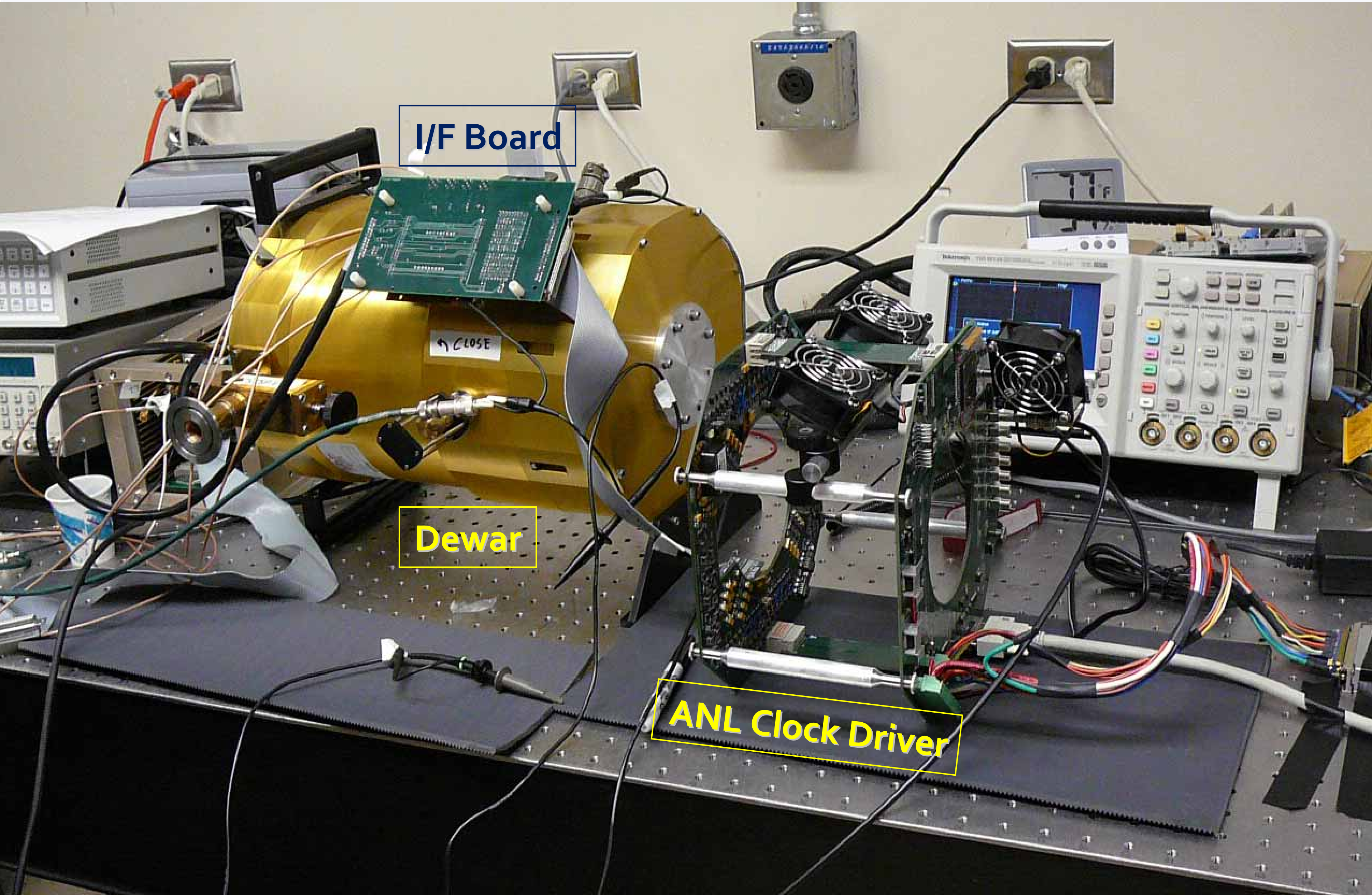


- Bill Kolbe (SNAP CCD test group)
- T = -135 C
- Slow readout ("Leach Controller" – astronomical CCD controller [http://www.astro-cam.com/], with some modifications for these high voltage, n-type CCDs)
- Cosmic rays … visible
- Dark current 5 e–/pixel/hour
  - 30 μm pixel
- Calibrate with ^{55}Fe
  - 3.5 μV/e^- (as expected)

Test Board with 480 x 480 CCD

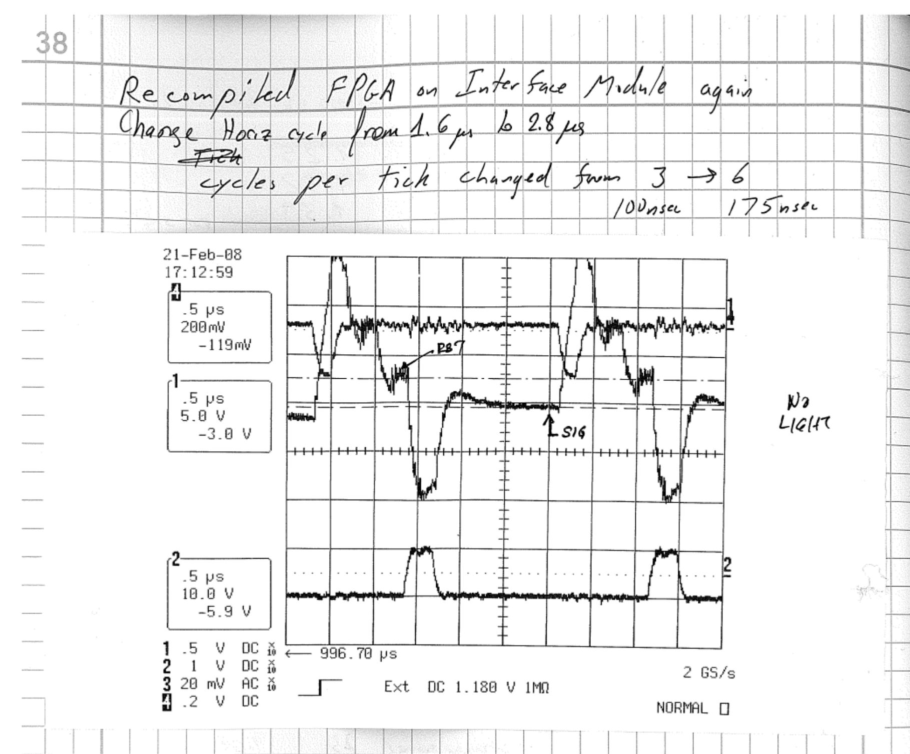


Mate ANL Clock Driver to 480 x 480 Feb. '08



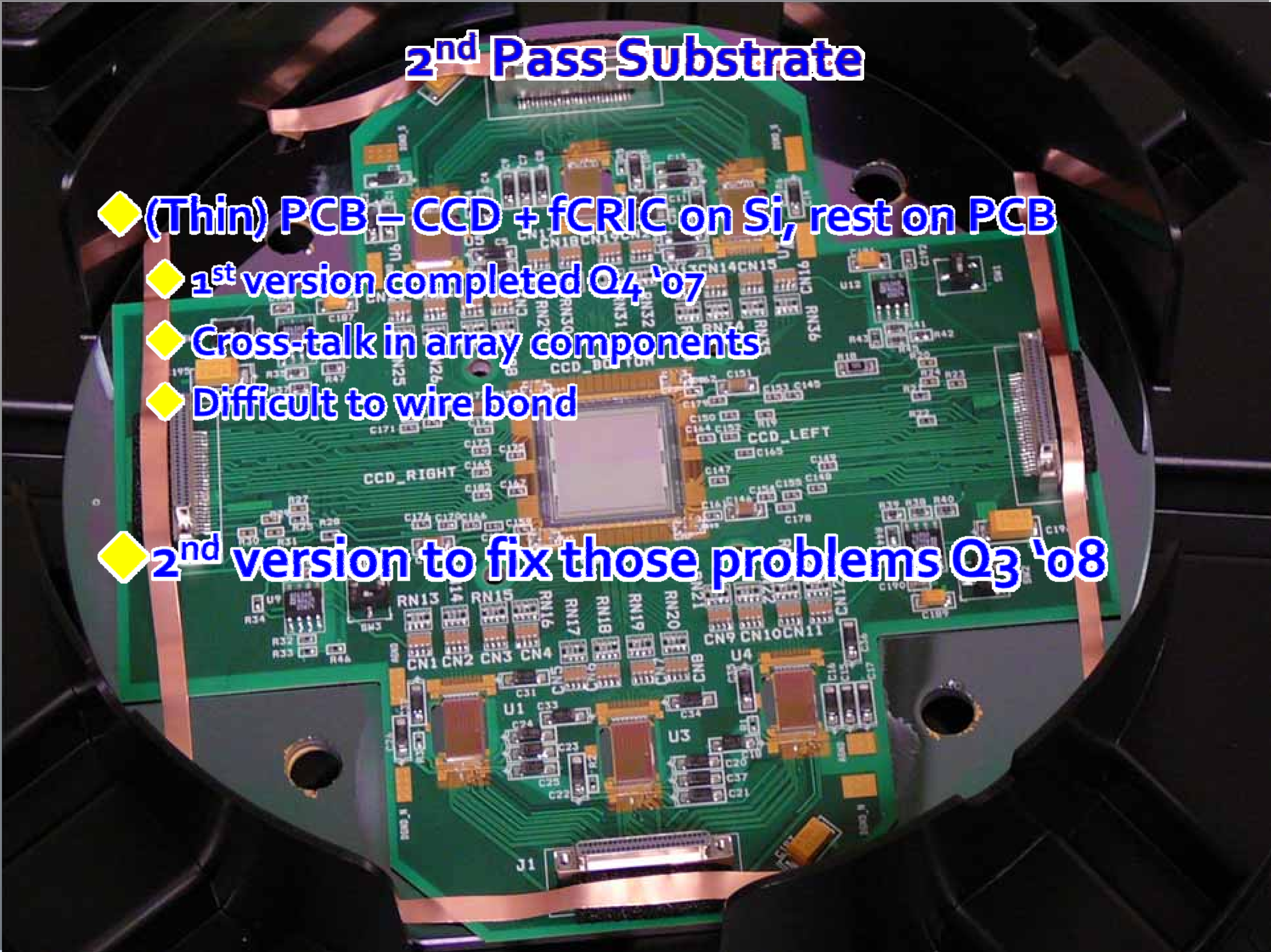
Guilty Parties

- Test clock drivers on 480 x 480 CCD in dewar
  - Figure out proper way to filter edges

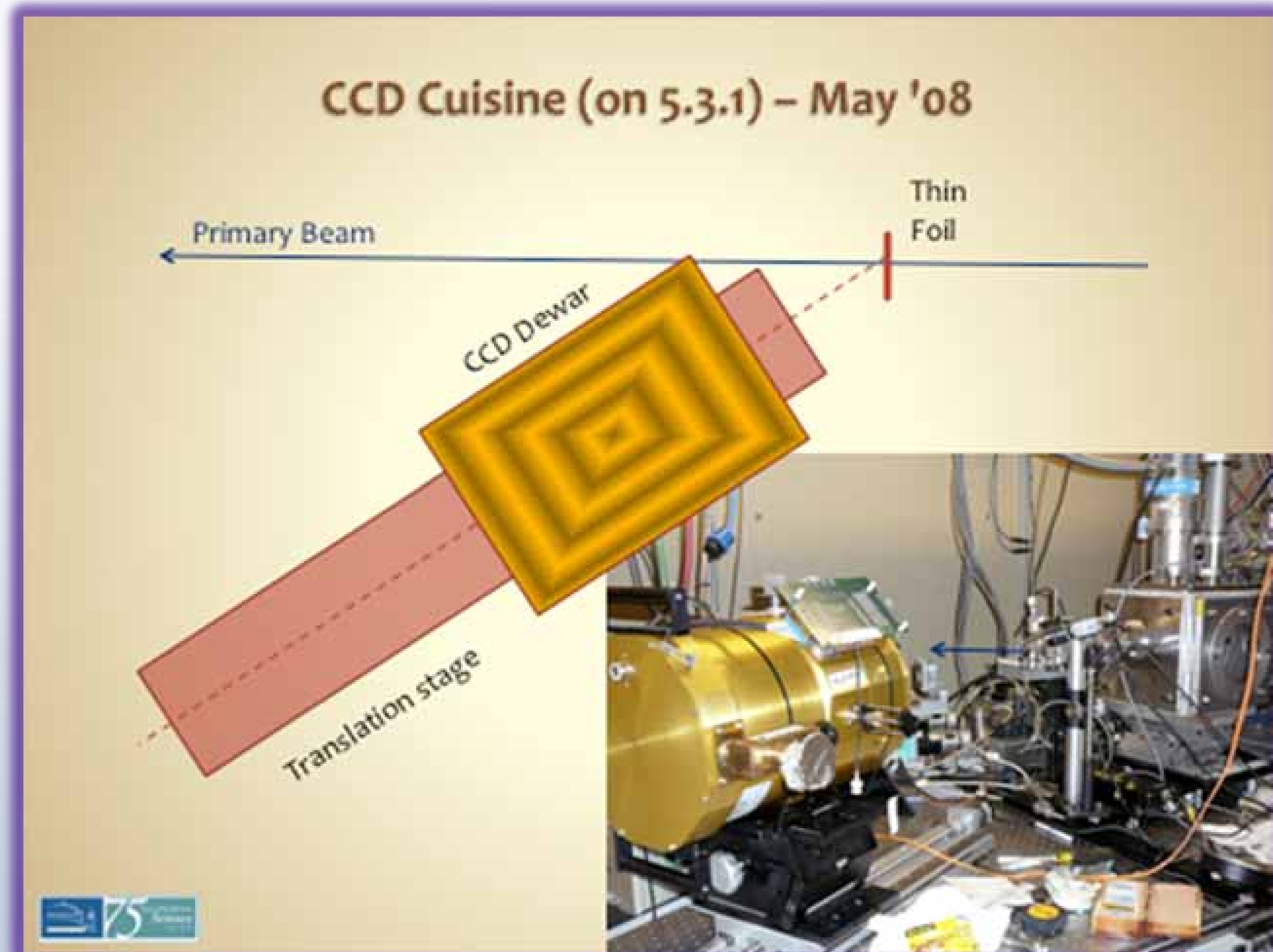


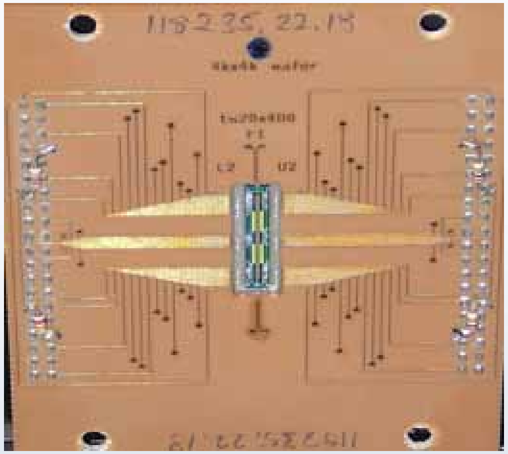
2^{nd} Pass Substrate

- (Thin) PCB – CCD + fCRIC on Si, rest on PCB
  - 1^{st} version completed Q4 '07
  - Cross-talk in array components
  - Difficult to wire bond
- 2^{nd} version to fix those problems Q3 '08



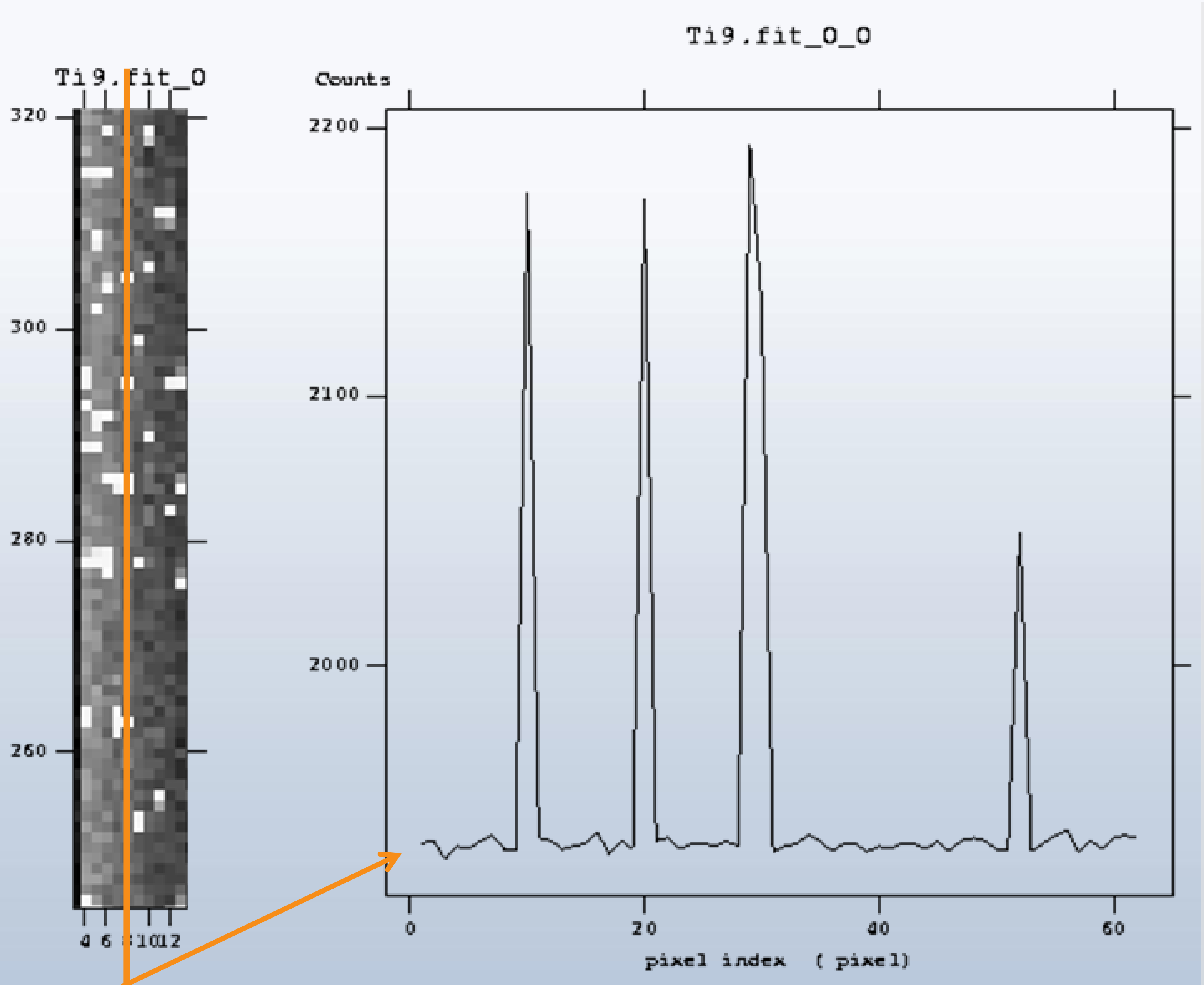
1st Beam Test on 5.3.1



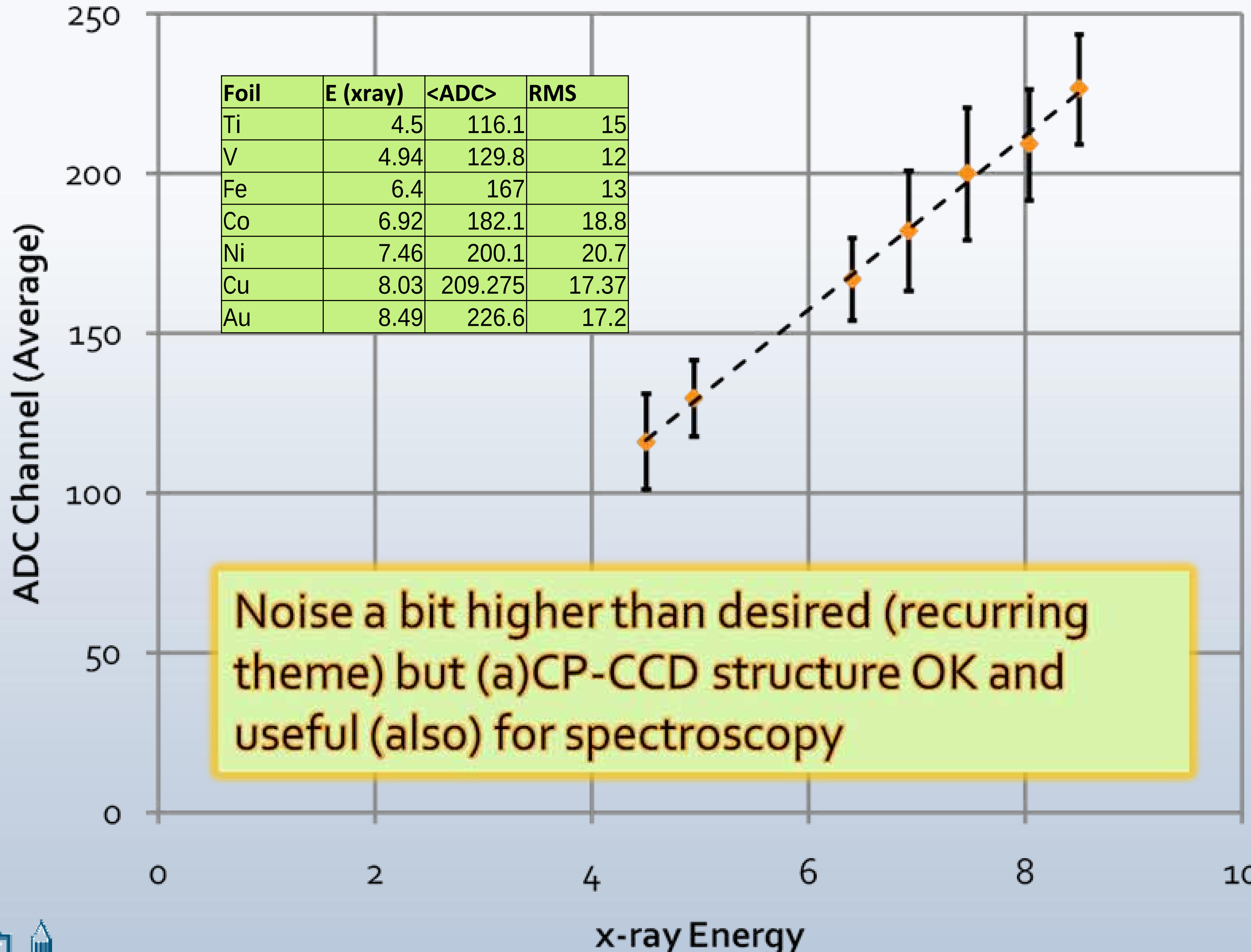


- 20 x 480 CCD
- Slow readout
- Fluorescence x-rays

See x-rays, Cluster Size ≥ 1



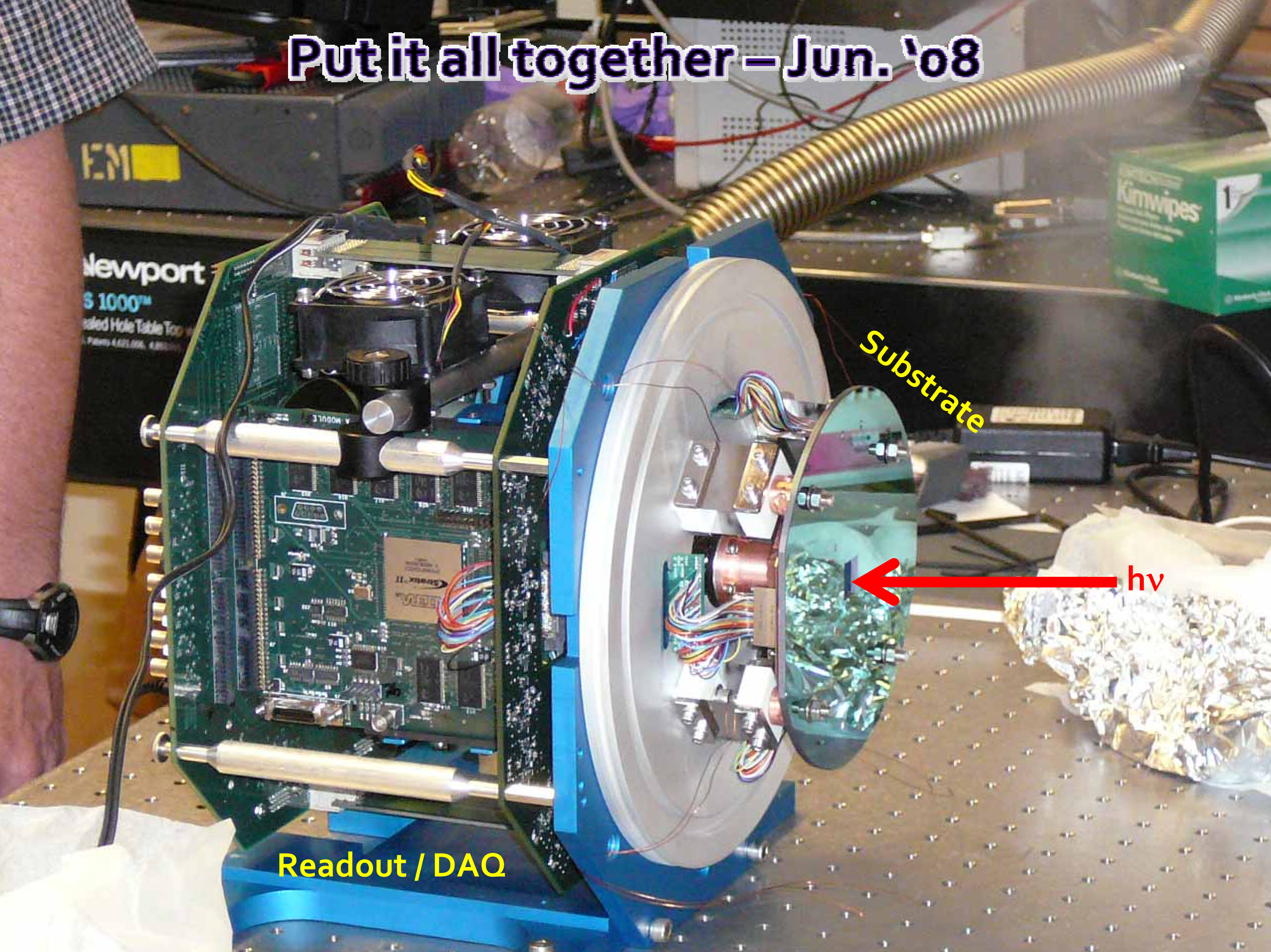
Direct Detection in Thick Si → Spectroscopic



Foil	E (xray)	<ADC>	RMS
Ti	4.5	116.1	15
V	4.94	129.8	12
Fe	6.4	167	13
Co	6.92	182.1	18.8
Ni	7.46	200.1	20.7
Cu	8.03	209.275	17.37
Au	8.49	226.6	17.2

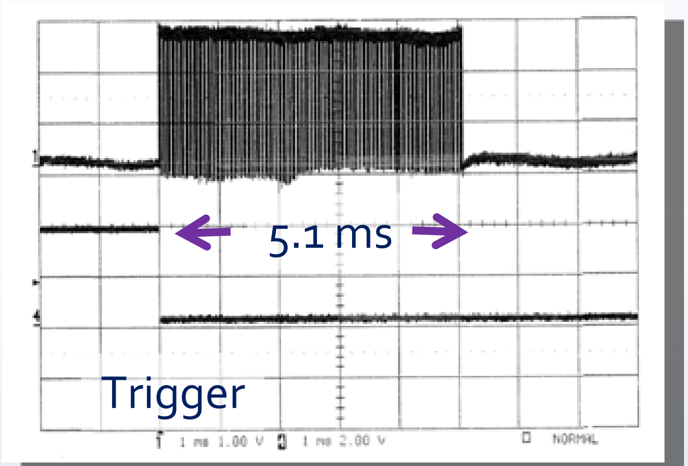
Noise a bit higher than desired (recurring theme) but (a)CP-CCD structure OK and useful (also) for spectroscopy

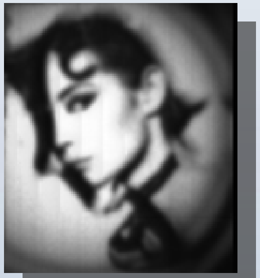
Put it all together – Jun. '08

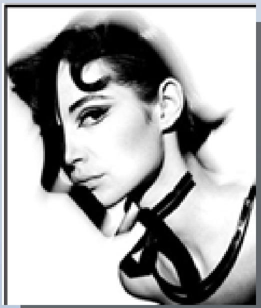


First Images with Fast Readout

- Synchronize fCRIC clock with CCD clock
- Verify 5 ms readout
- Start to optically characterize CCD
- (although there are still various problems at this point)





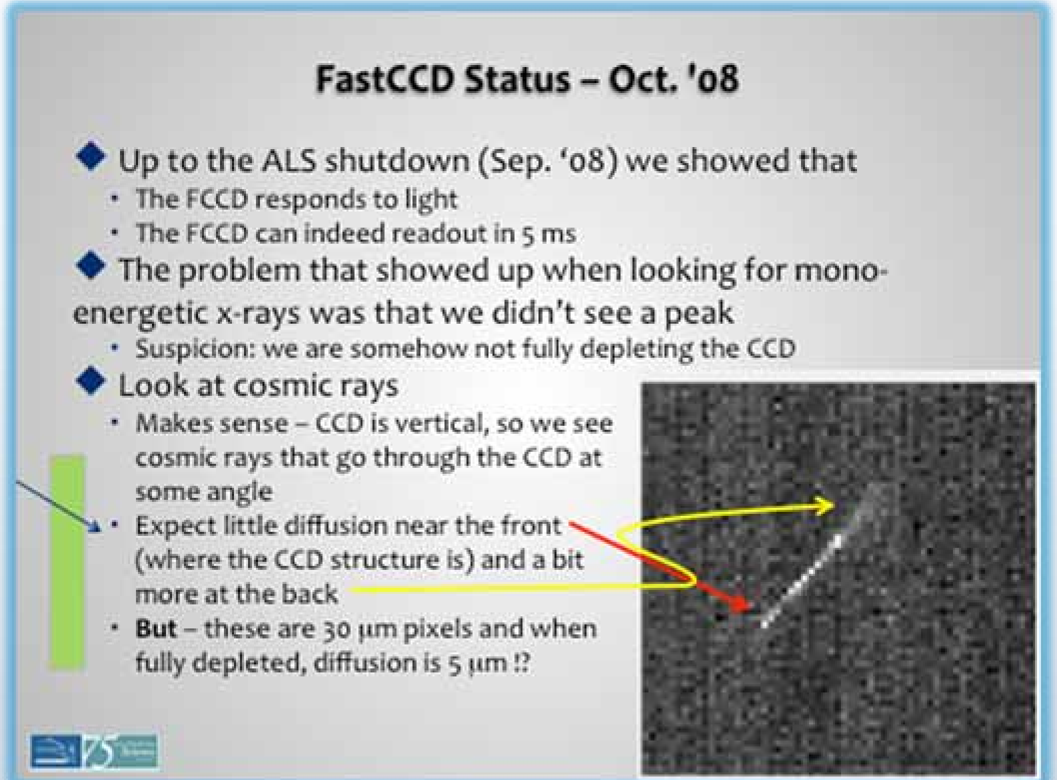


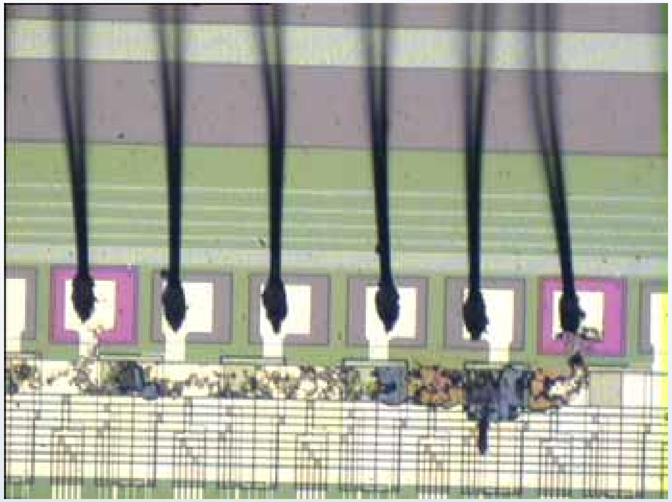
Footnote

- fCRIC always reads "fast"
- System clock f_{SYS}
- fCRIC digitization cycle $T_{ADC} = N/f_{SYS}$, $N < 256$
- CCD horizontal cycle $T_{HOR} = 16\ P \times 25$ ns
  - P is an (integer) pre-scaling factor
- Maximum speed: $T_{ADC} = T_{HOR}$
  - $N = f_{SYS} \times 25\ \text{ns} \times 16\ P$
- The "link" between CCD and fCRIC timing is CONVERT
- GAIN (in fCRIC) set by integration time
  - Which we fix at 400 ns, independent of TADC

FCCD on 5.3.1 Aug. '08

Learning Curve

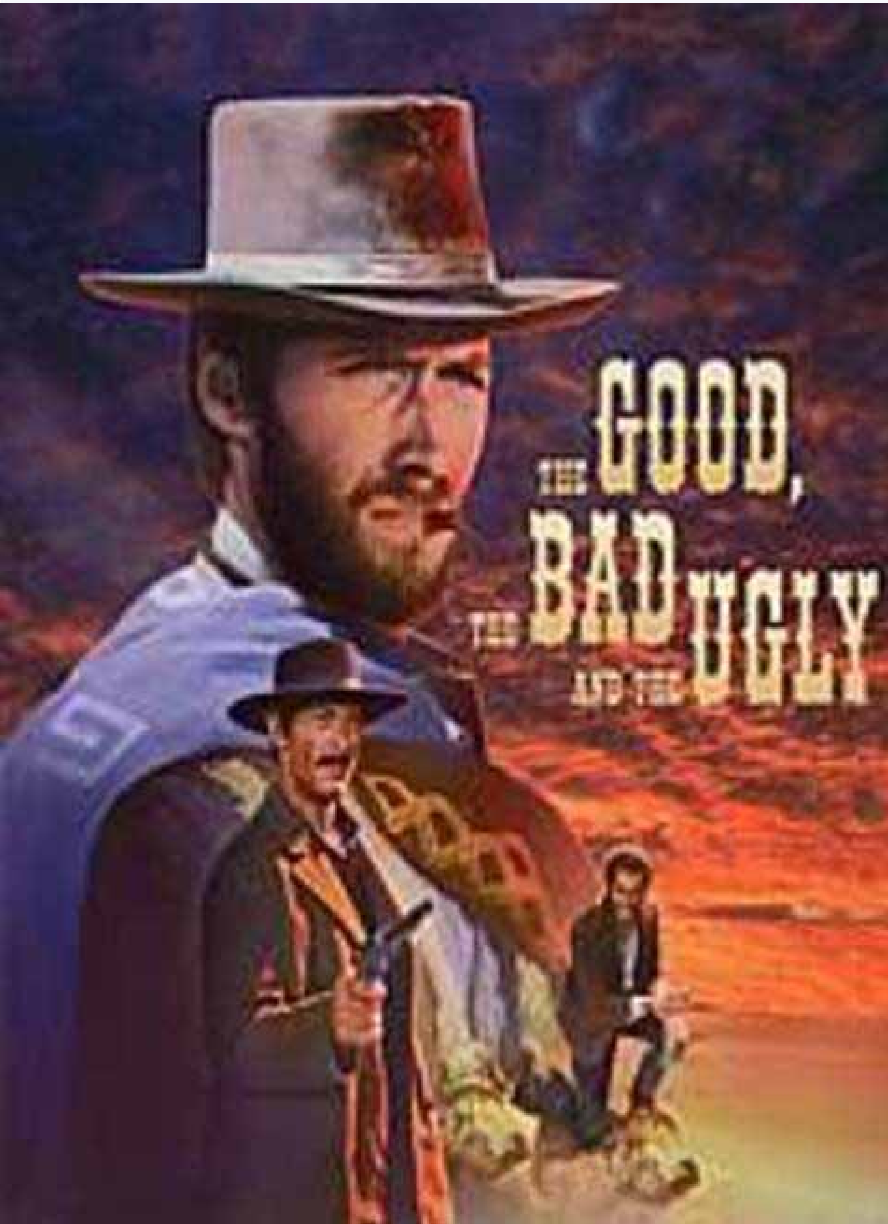




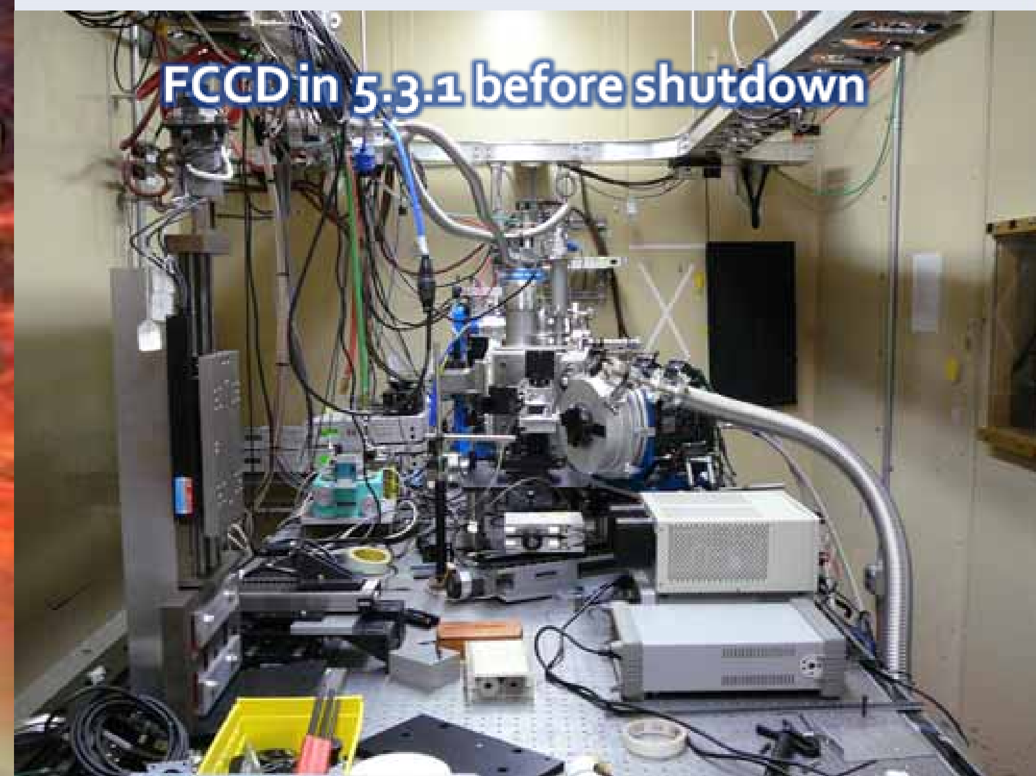
Some "details" (and some fried CCDs)

- Lots of characterization and learning
  - → New CCD substrate (to overcome) crosstalk
  - → New ANL readout boards

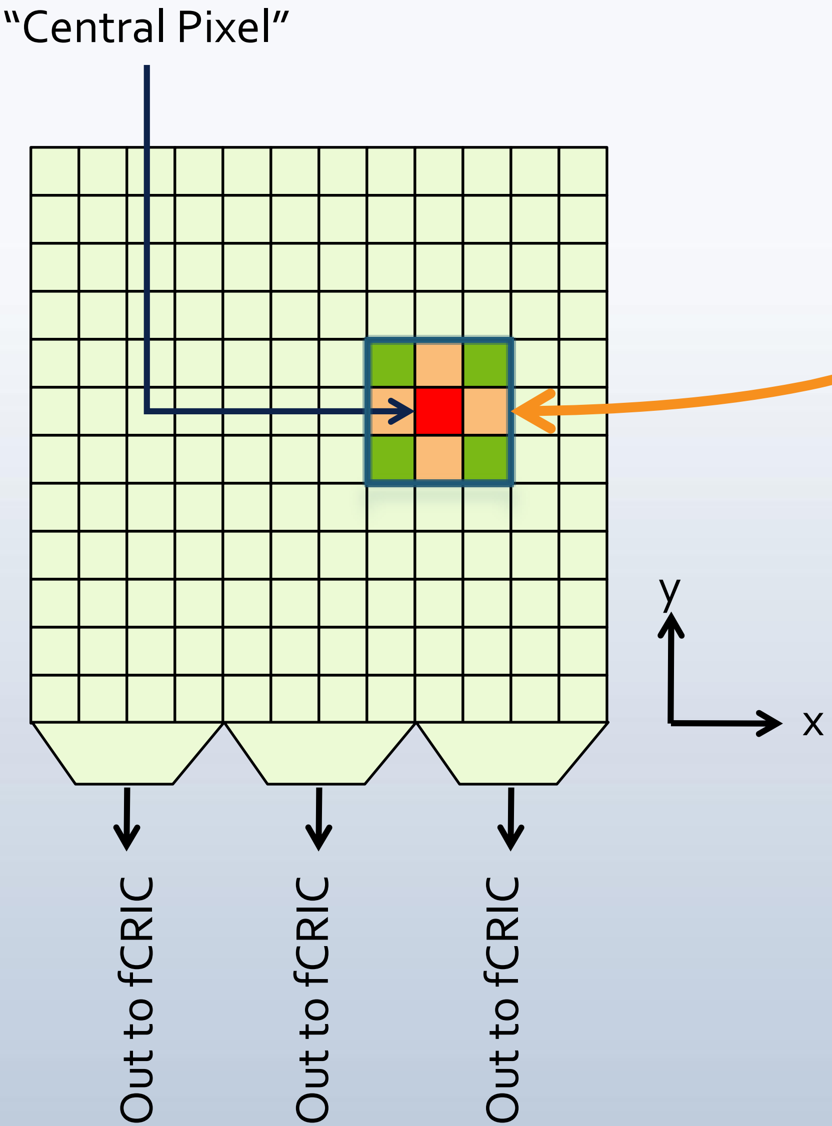
For a Fistful of Photons



- Build a new substrate with fresh CCD and fCRICs for delivery to APS
- Lab characterization (Nov. '08)
- Test on 5.3.1 (Dec. '08)
- Test this week at APS (Jan. 08)



Nomenclature



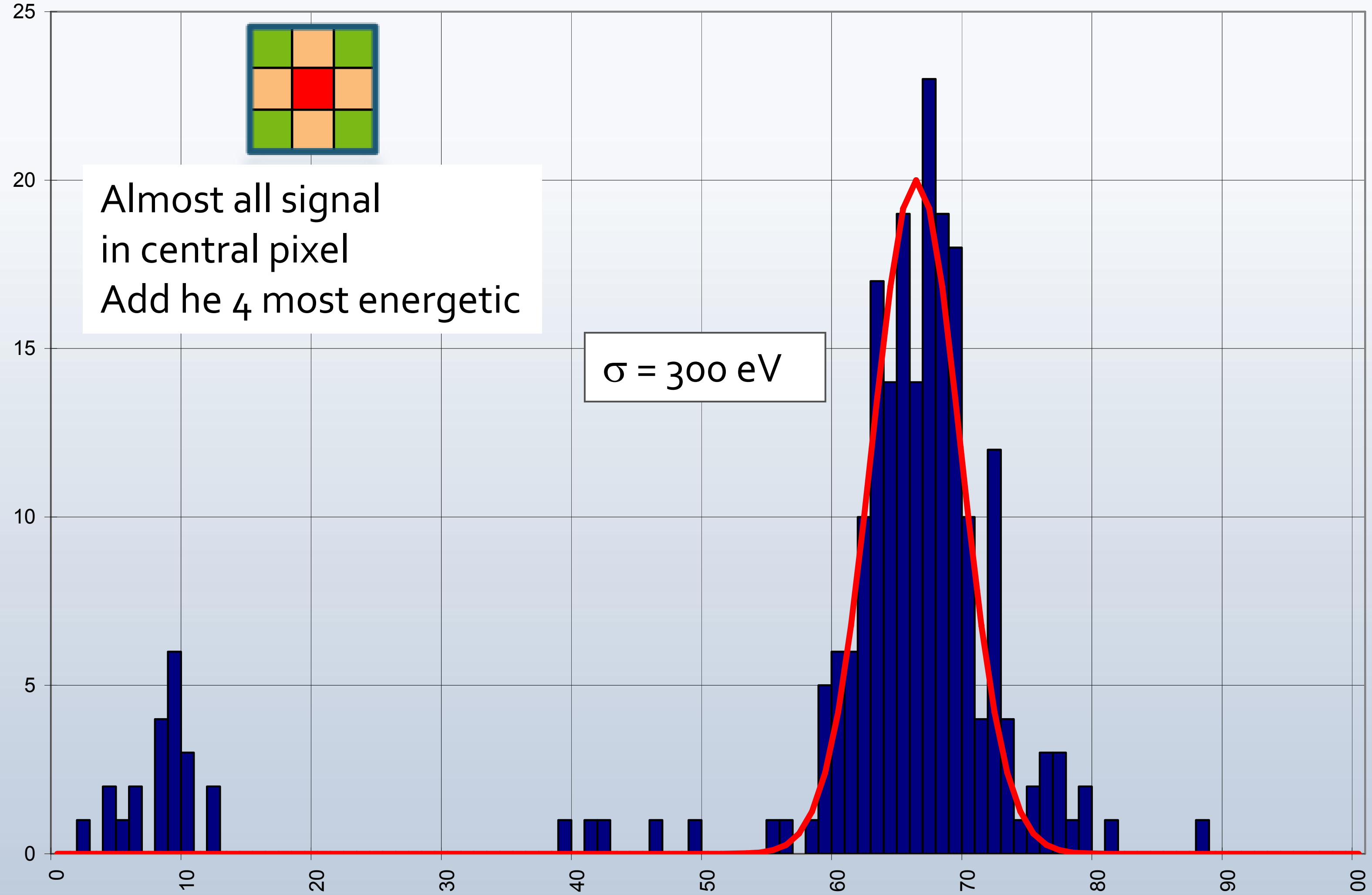
- $V(x,y)$ = value of pixel at (x,y)
- If $V(x,y) – V(x,y-1) > \text{THRESH}$ then Pixel(x,y) is *a seed pixel* (for a *seed* in a 3 x 3 matrix)
- Use (local) column average

  as the pedestal
-
- Within the 3 x 3 matrix, let P_i be the

  i^{th} most energetic pixel
- Sum the *k* most energetic pixels

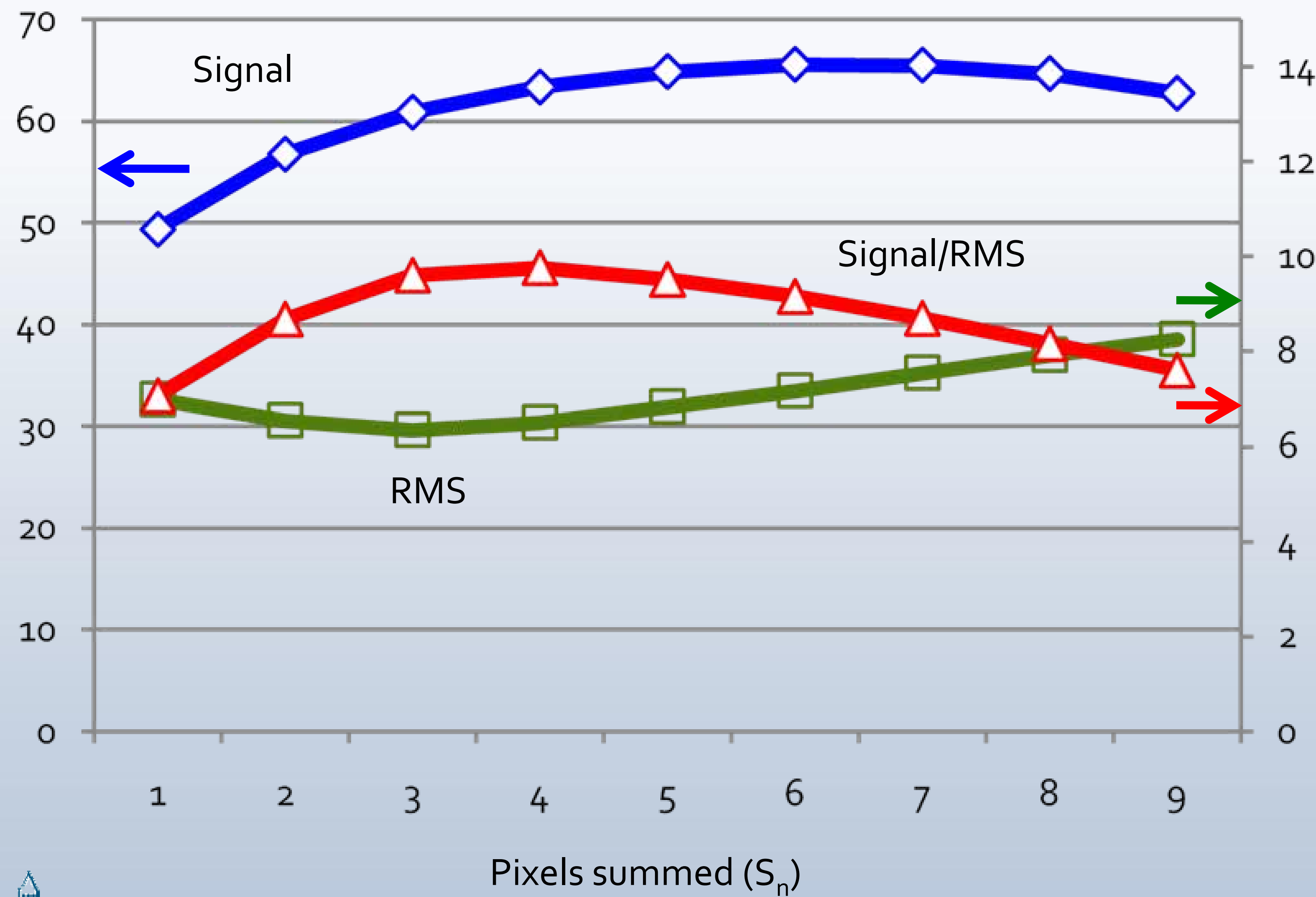
^{55}Fe – S4 for S1/S2 ≥ 95%

90 eV/ADU



Old substrate, Forced x2

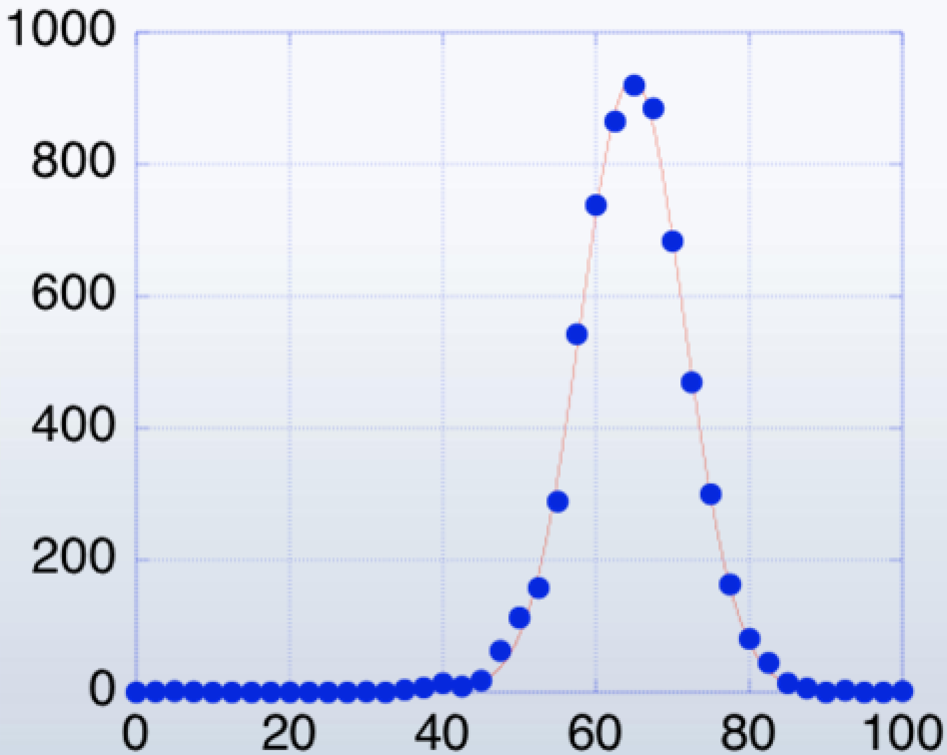
Signal and RMS vs. *N*



Old substrate ^{55}Fe

P. Denes 01/09

Conversion Gain



Histogram S6 (no cuts)

- 5900 eV (1640 e^-)
- Peak at 64.8 ADU
  - ~90 eV/ADU
  - ~25 e^-/ADU
- σ=6.7 ADU
- Noise ~1.4 ADU/pixel

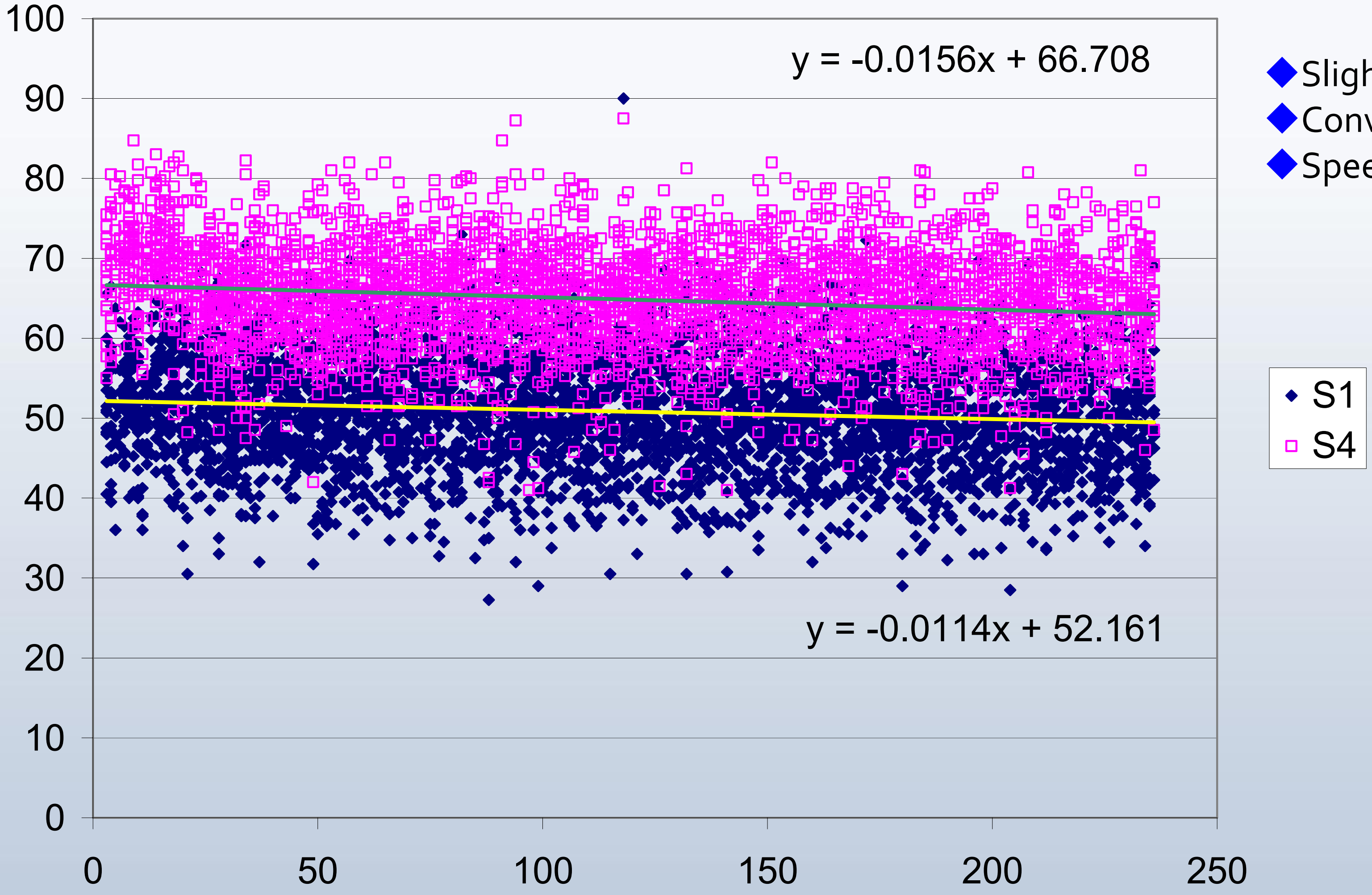
→ ~3.5 ADU for 6 pixels

Cross-check

- fCRIC = 0.5V FS (12 bits)
- x2 → 61 μV/ADU or 2.4 μV/e^-
- Leach controller: CCD = 3.5 μV/e^-

Old substrate ^{55}Fe, Forced x2

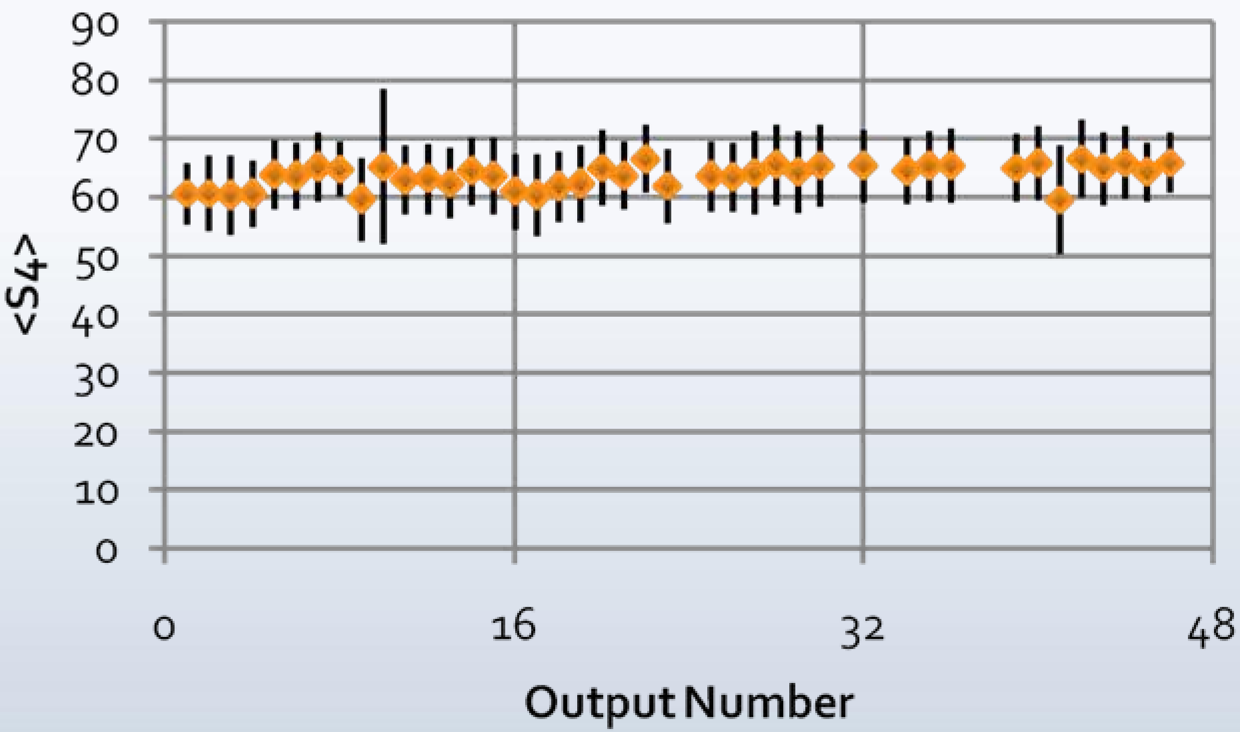
CTE?



- Slight y dependence
- Conversion gain
- Speed/clocking

Old substrate ^{55}Fe, Forced x2

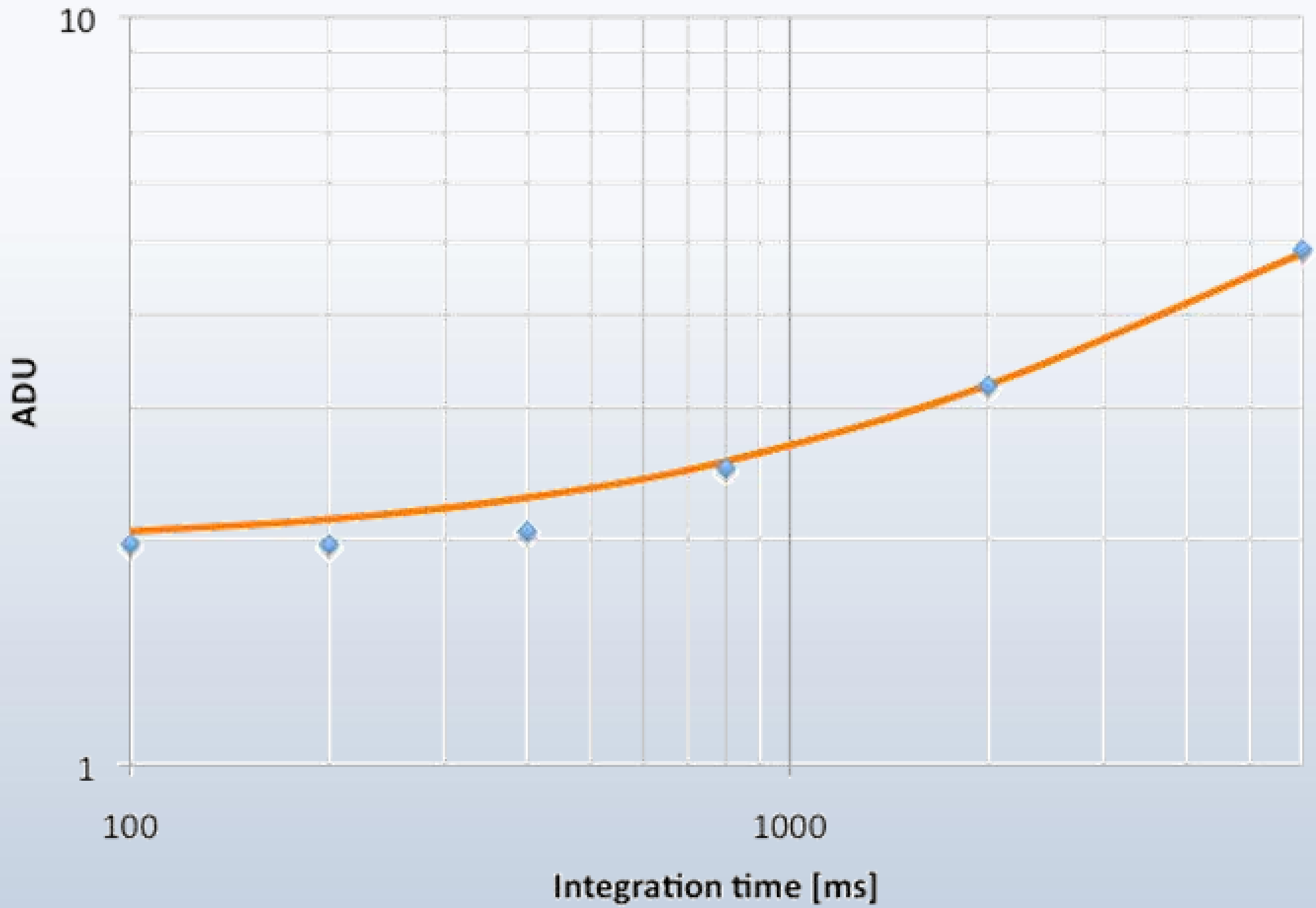
Uniformity of Outputs



S4 = 63.7 ± 2.0 (3%) → 3% gain variation in outputs (not bad!)

Old substrate ^{55}Fe, Forced x2

Noise (average RMS) vs. Integration Time



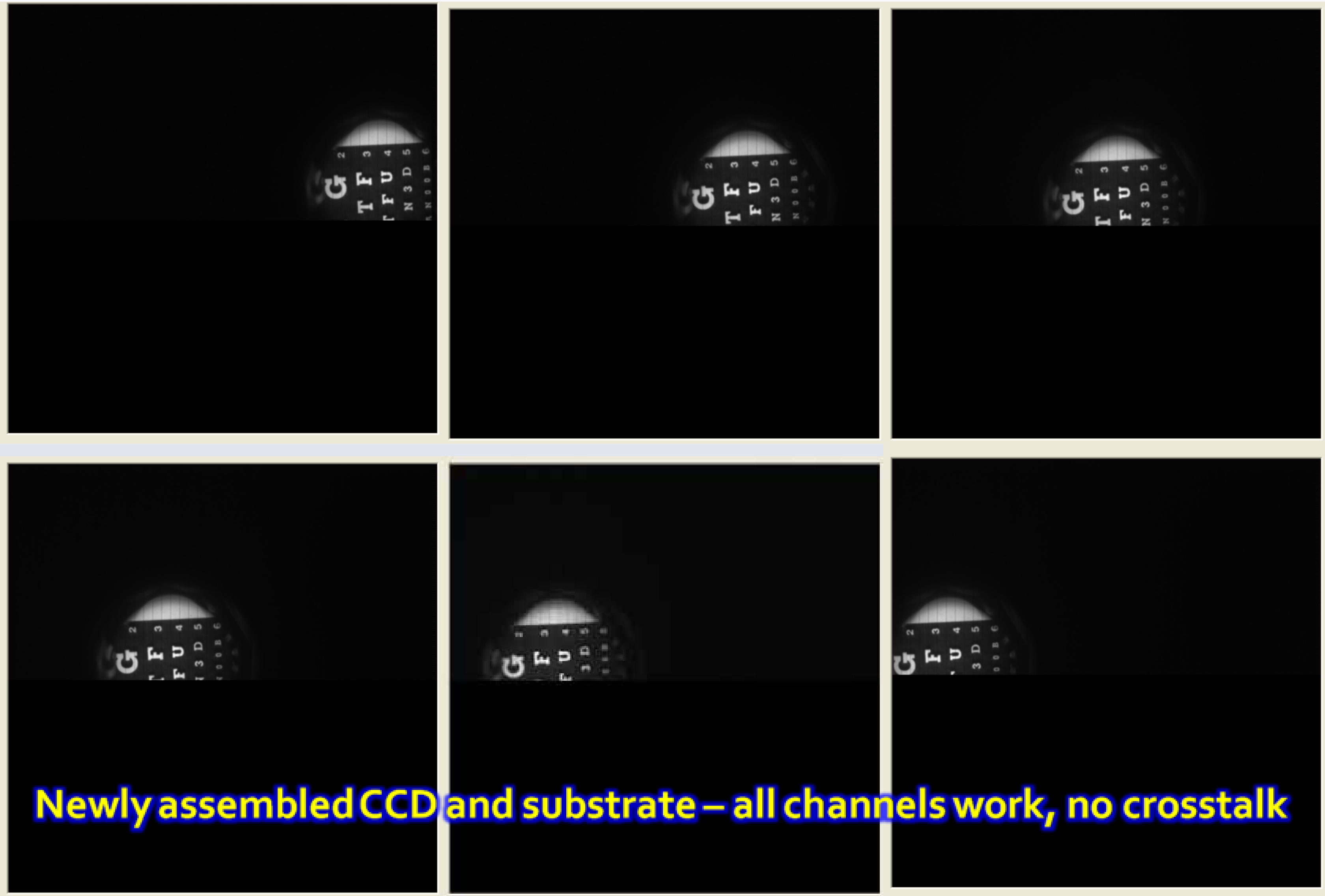
A ~ 2 ADU
B ~ 0.057 ADU /√ms

Divide both by √2 (difference of two measurements)

Average of differences on previous plot
Fit to

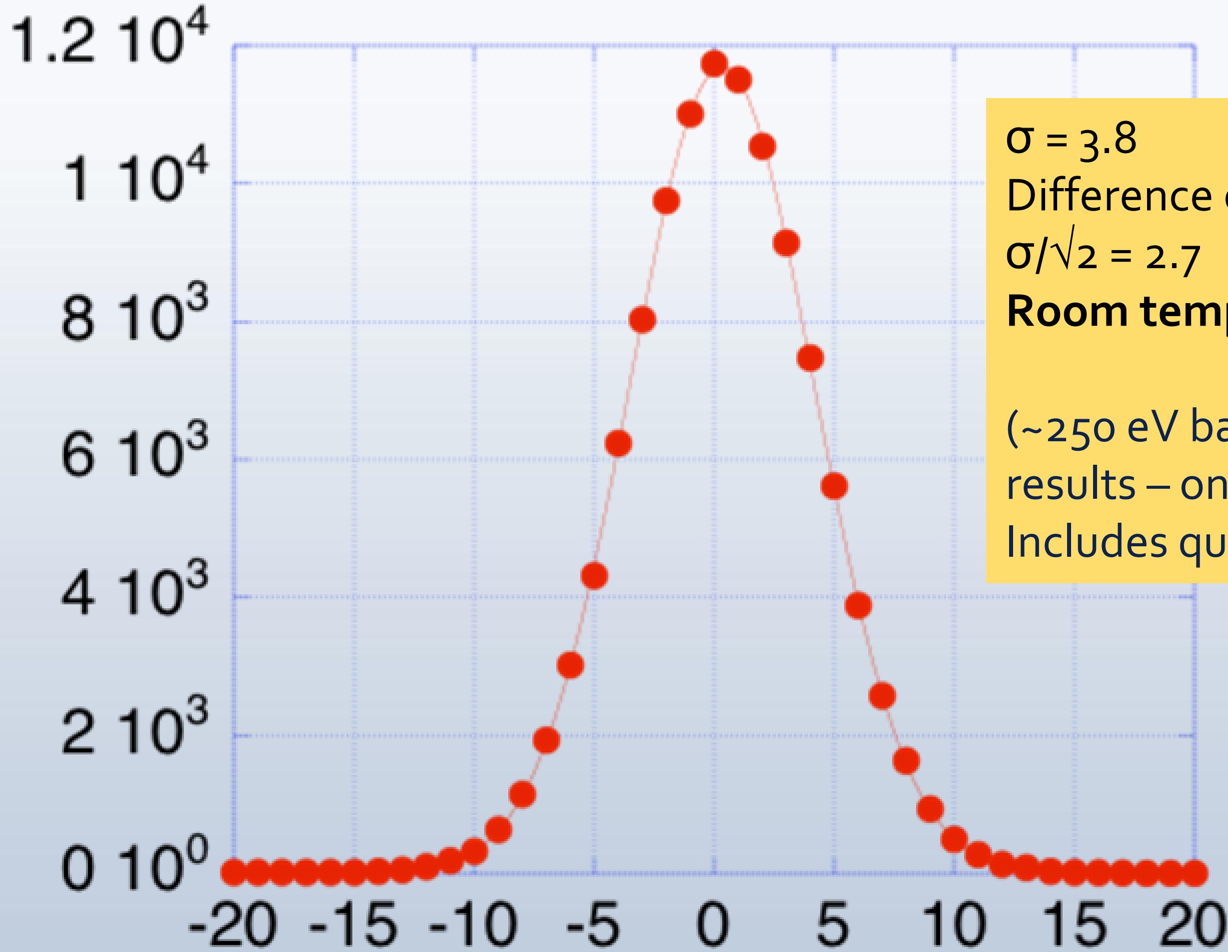
Old substrate, Forced x2

New Substrate - Scan optical image across CCD



Newly assembled CCD and substrate – all channels work, no crosstalk

Pedestal (difference of 2 dark images)



σ = 3.8
Difference of two images →
σ/√2 = 2.7
Room temperature

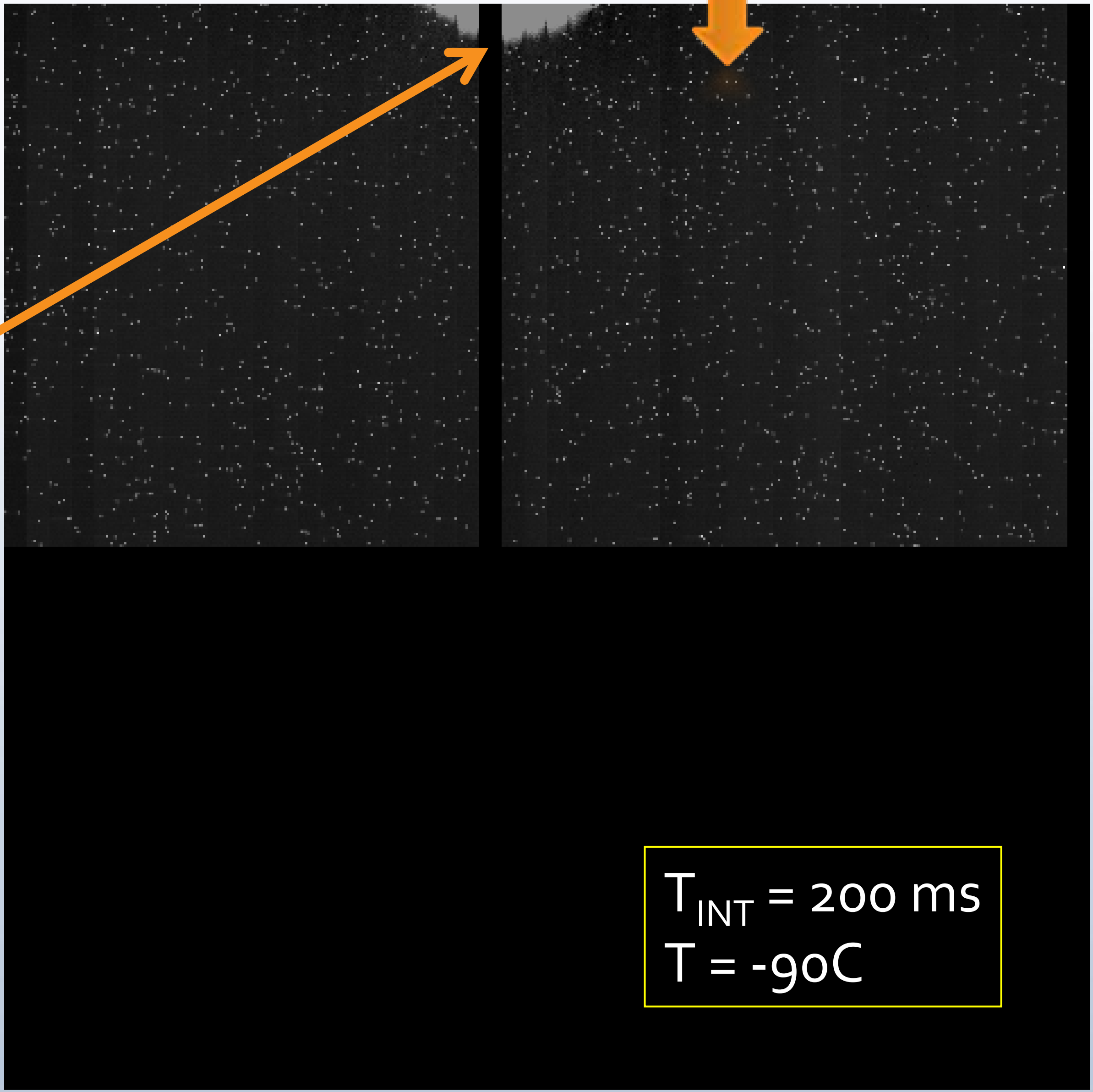
(~250 eV based on previous results – on Forced X2, so Includes quantization error)

Comments (1)

- Every channel works
  - Each CCD output
  - Each fCRIC input
- By eye, gain uniformity is not bad
- Crosstalk problem gone
  - New board layout eliminated the problem
- New/Old substrate noise the same
  - Some power supply "issues" – will be fixed with new ANL readout boards

Yes, it sees xrays

- Installed on 5.3.1
- Fluorescence photons from Nb
- "Features" (see next page)
- Running (fast) 1.6 μs horizontal cycle
  - But slow vertical clocks (otherwise lose synchronization)



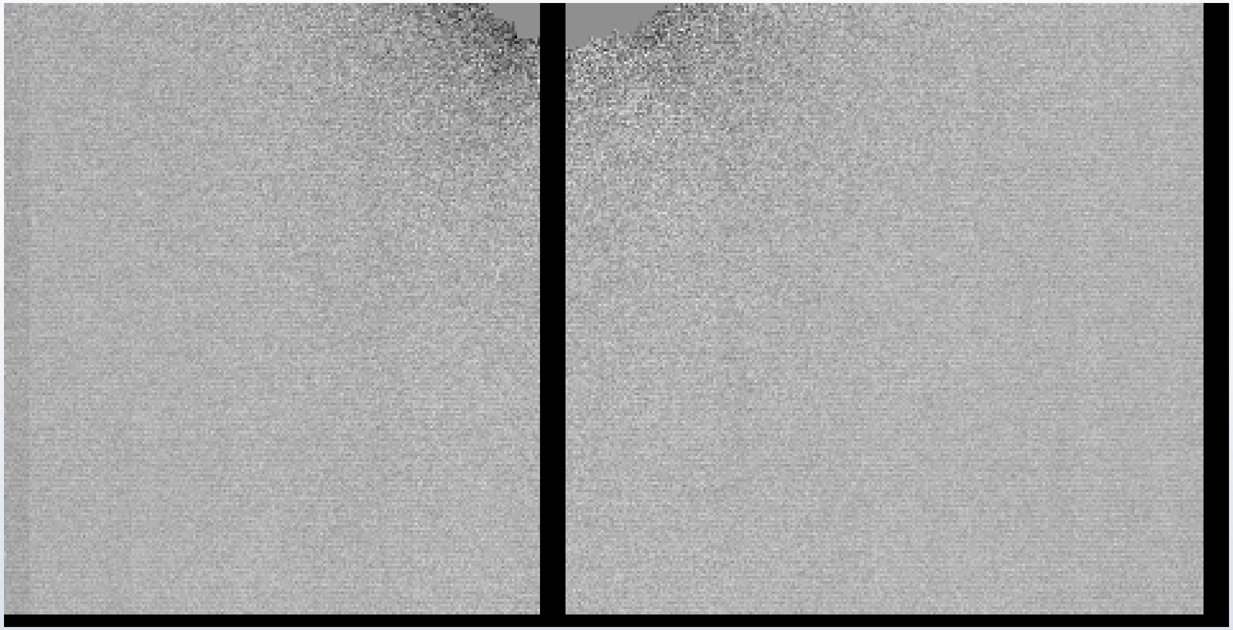
New substrate, Forced x8

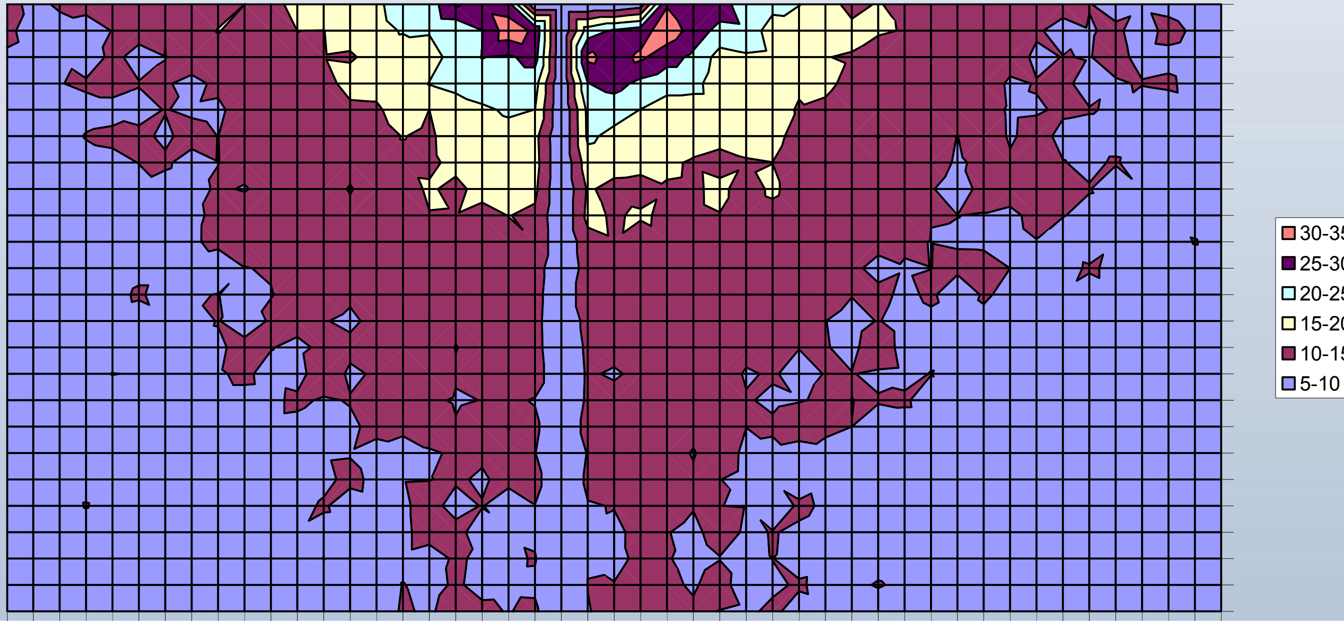
Notes

- Only ½ the CCD could be read out
  - Fixed this week (firmware upgrade)
- Dead channel
  - Fixed before shipping – bad resistor
- Slow vertical clock needed
  - Fixed this week (firmware upgrade)
- "Glow" (IR photons from output stage)
  - Still have some of this – annoying, not fatal

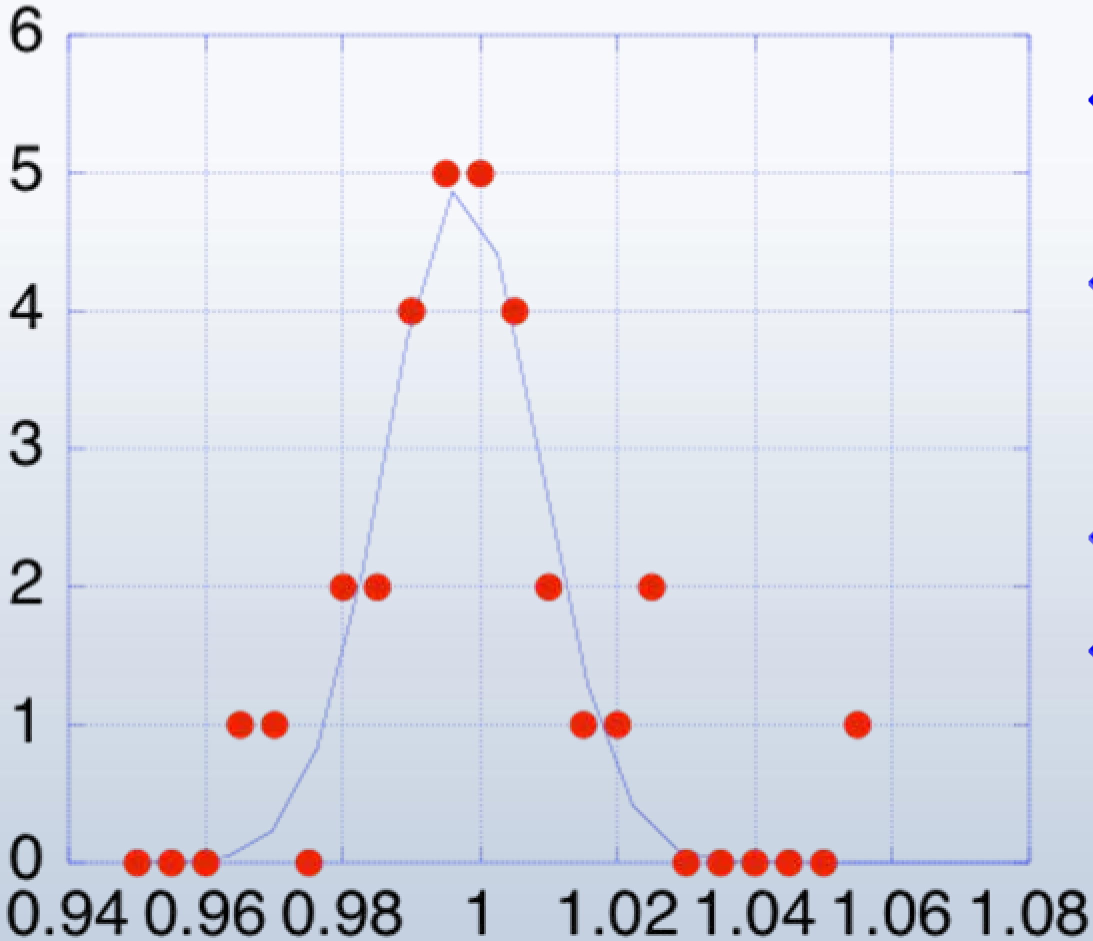
Noise (in 10x10 pixel blocks)

- Glow → noise increase (shot noise)
- Long (200 ms) integration here
- ~factor 2





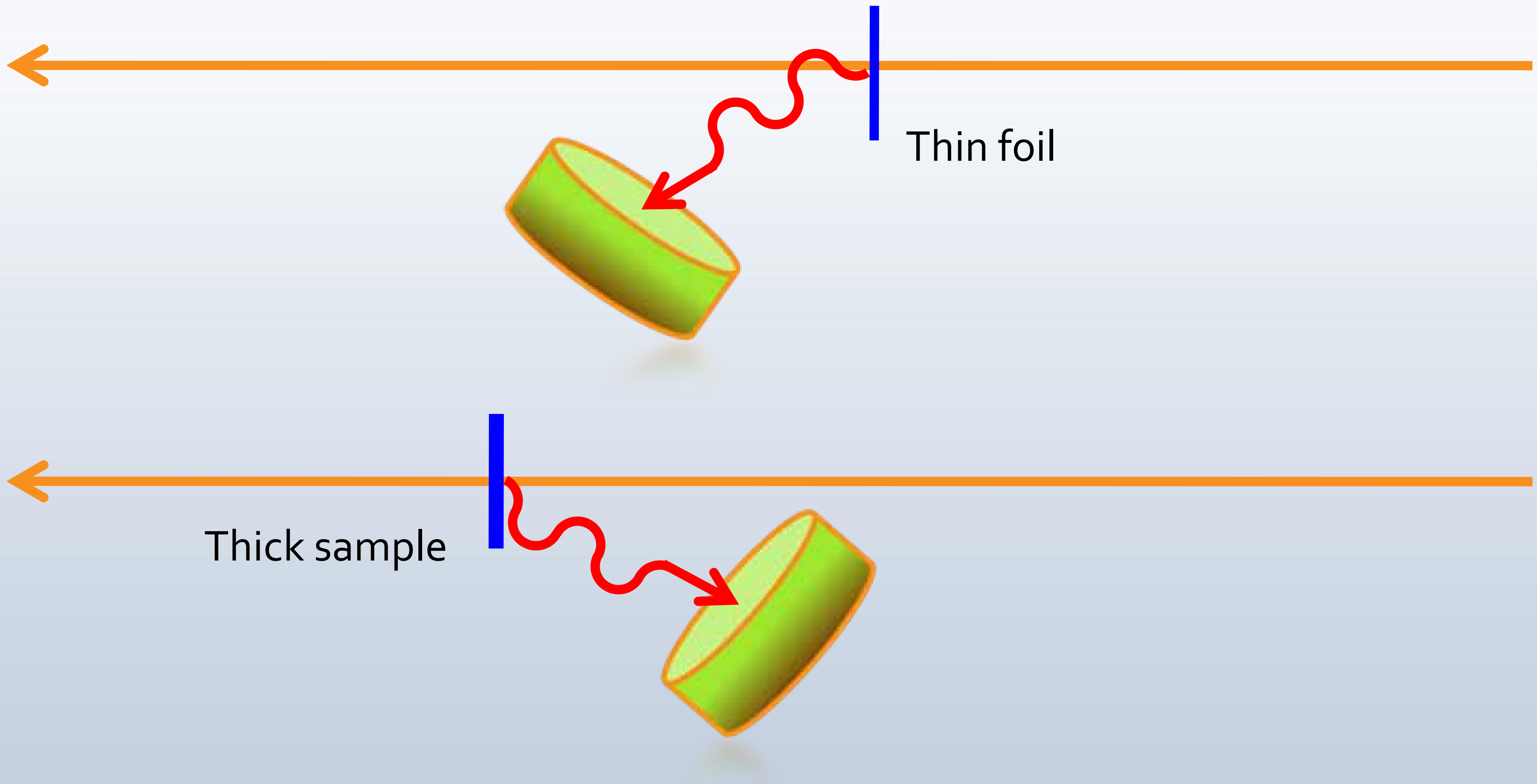
Calibration



- Inter-calibration target = Ag (22 keV)
- Select hits with $0.95 < S_1/S_4 < 1$ $600 < S_1 < 1000$
- Calibrate *outputs*
- Spread = 1.6% (!)

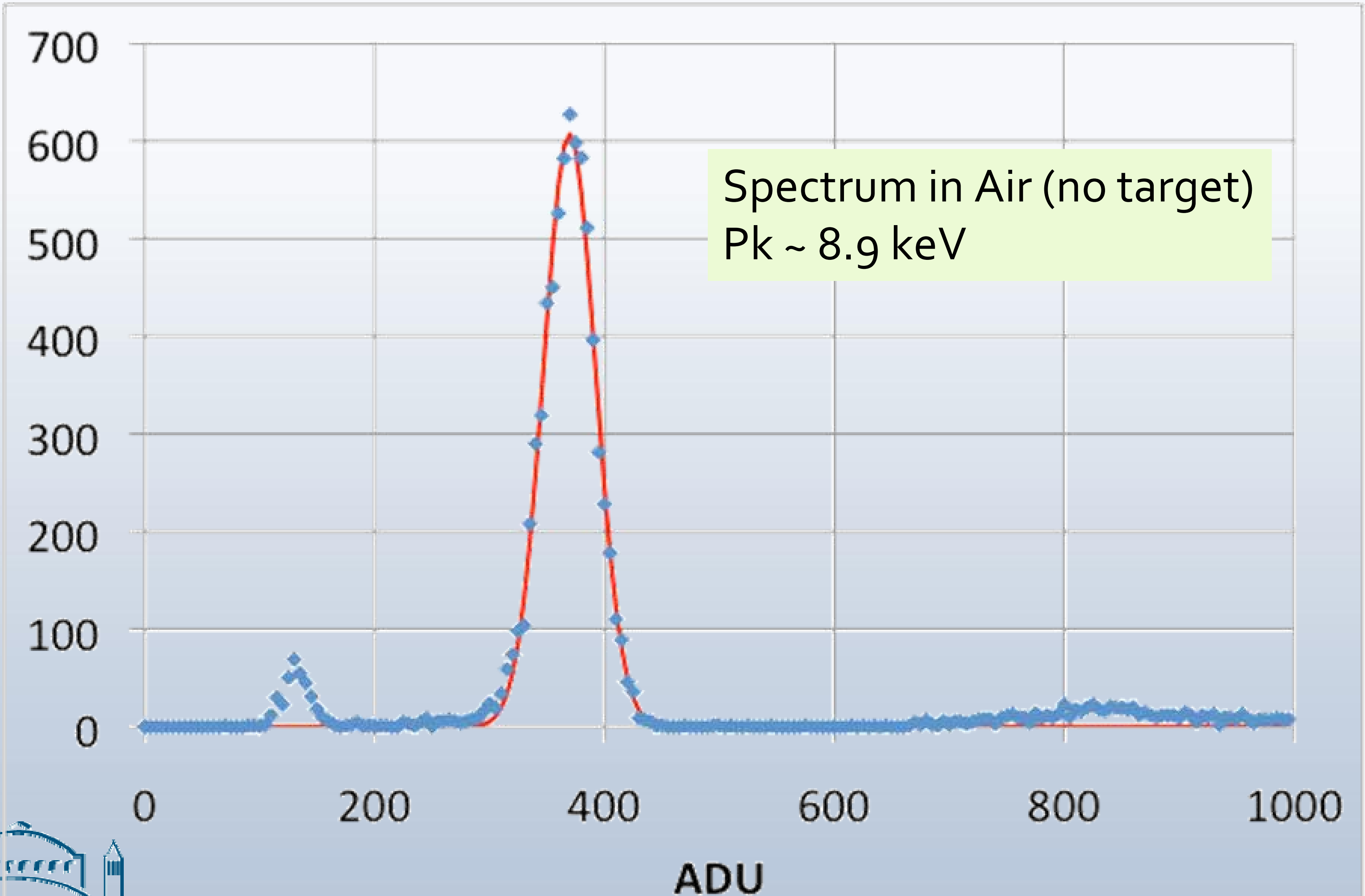
New substrate, Forced x8

Two arrangements in 5.3.1



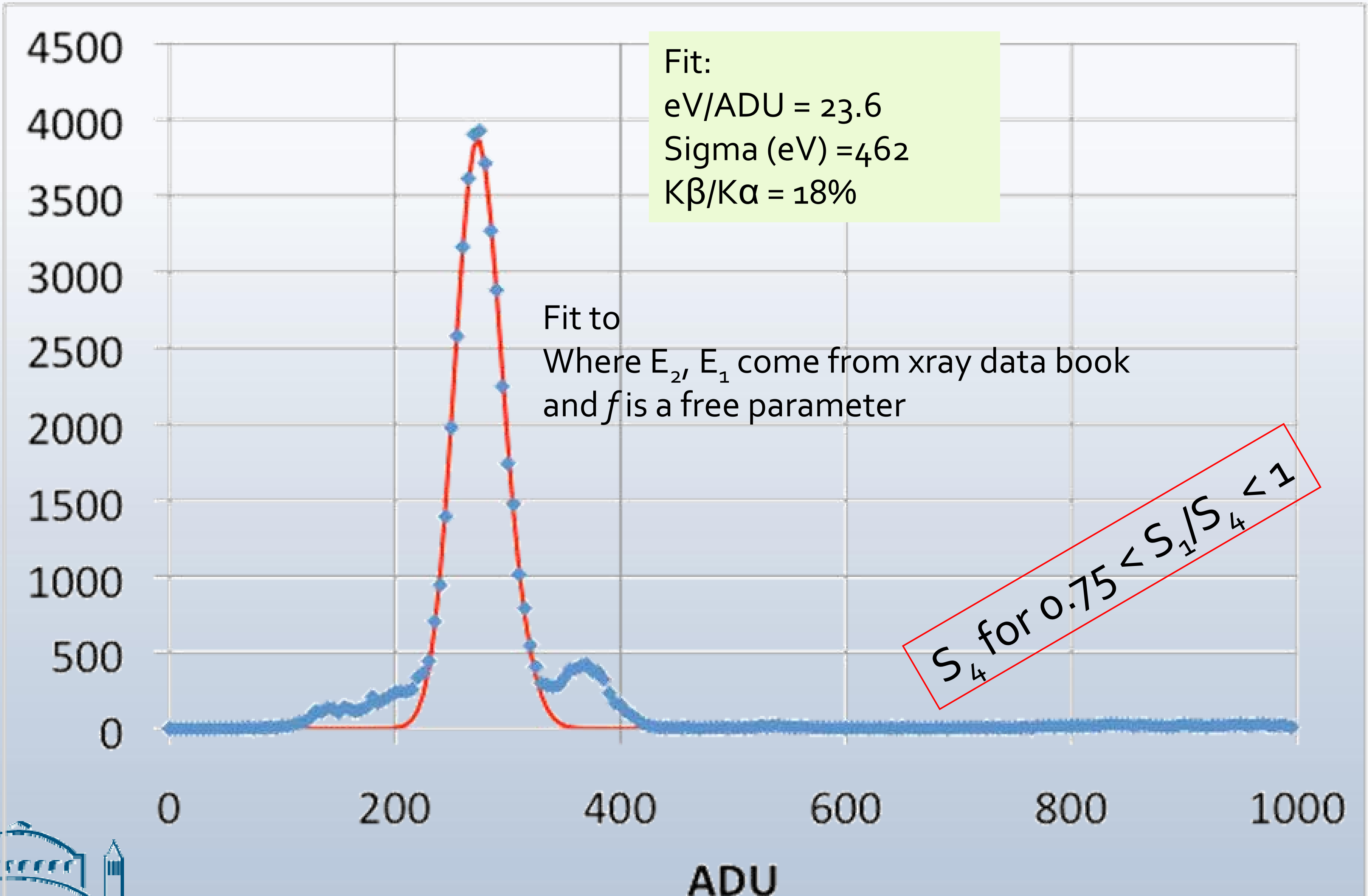
Background

We have a background (we had this before in 5.3.1)



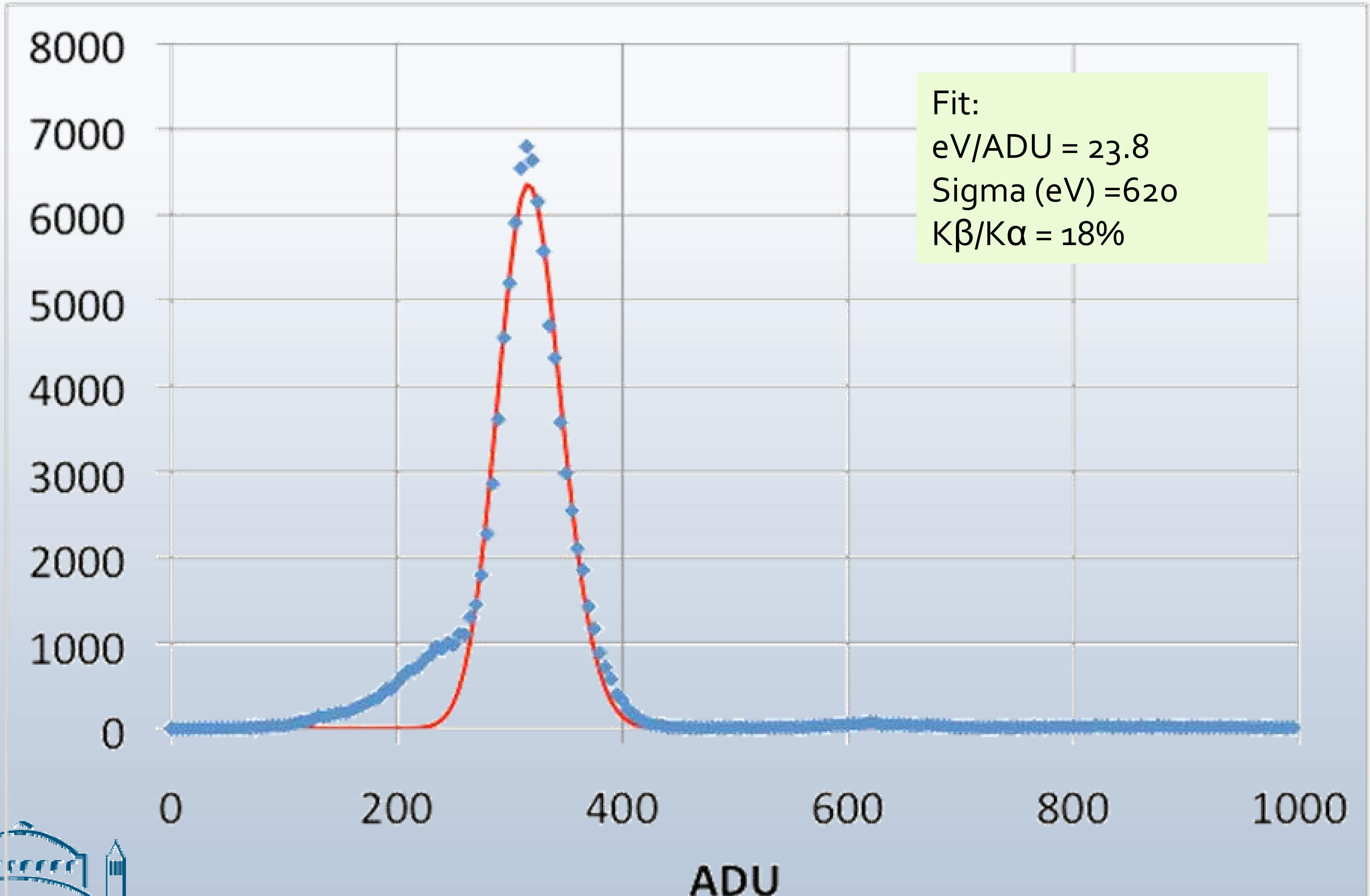
New substrate, Forced x8

Fe - Transmission



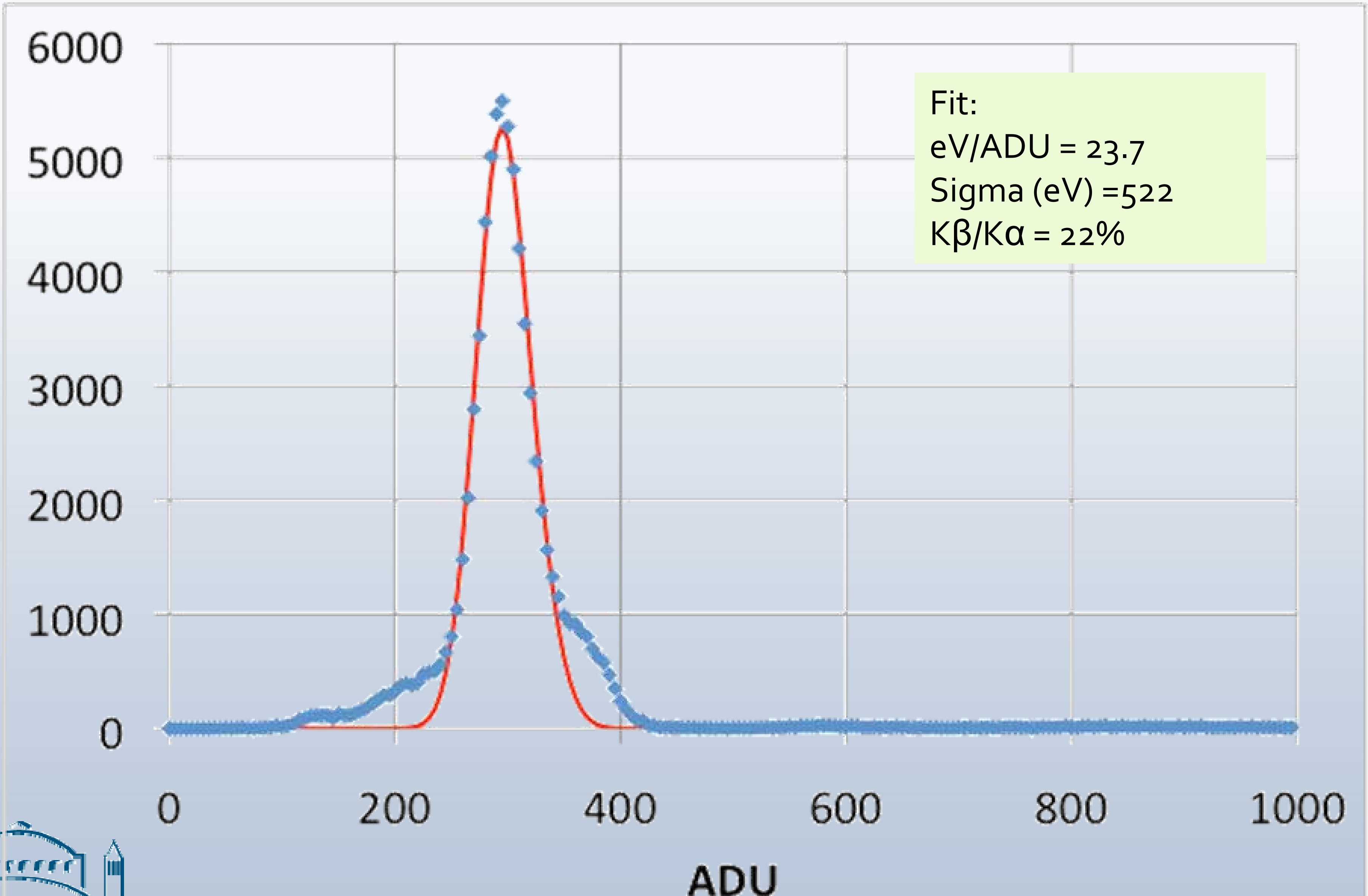
New substrate, Forced x8

Ni - transmission



New substrate, Forced x8

Co - Transmission



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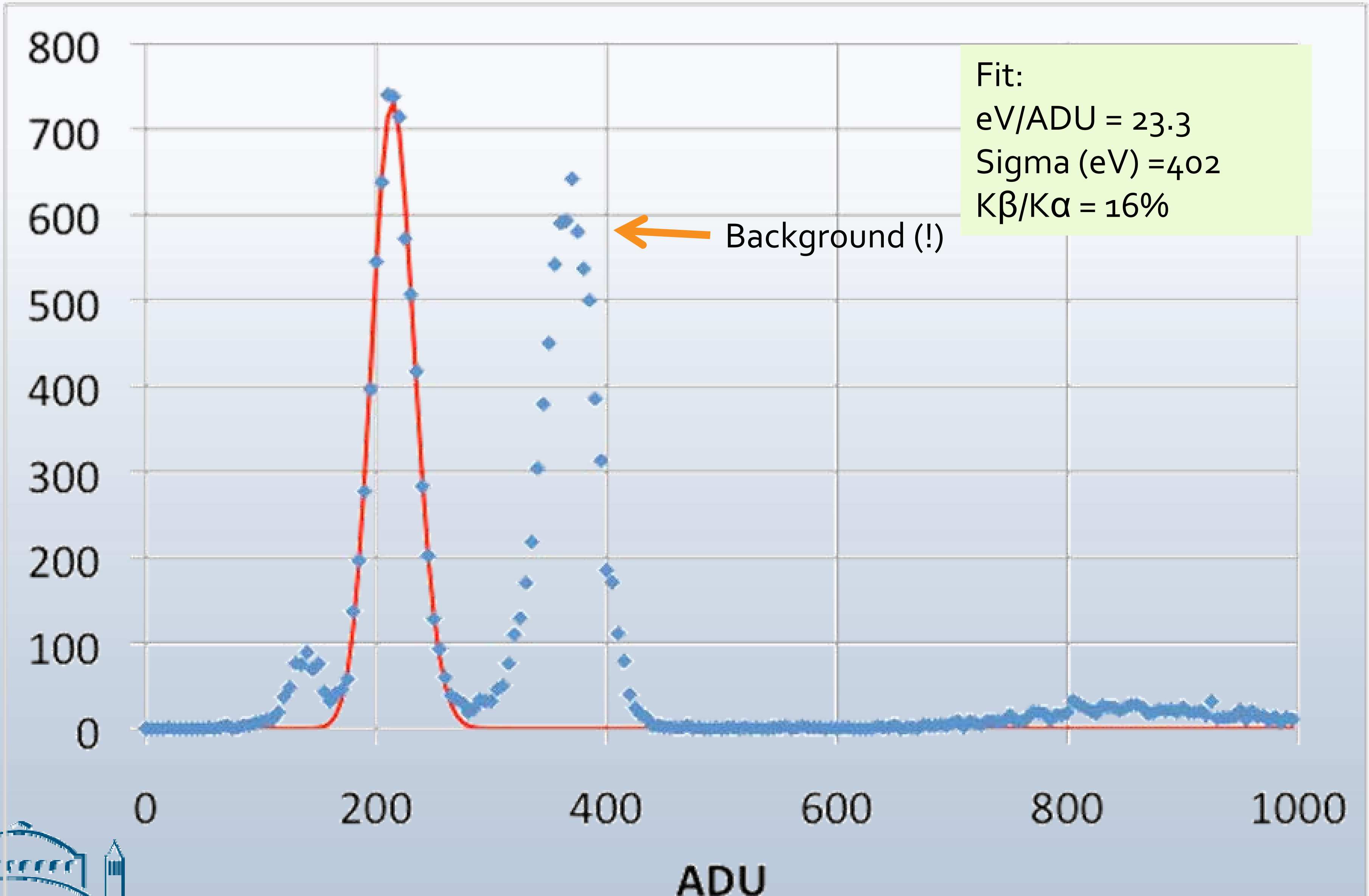
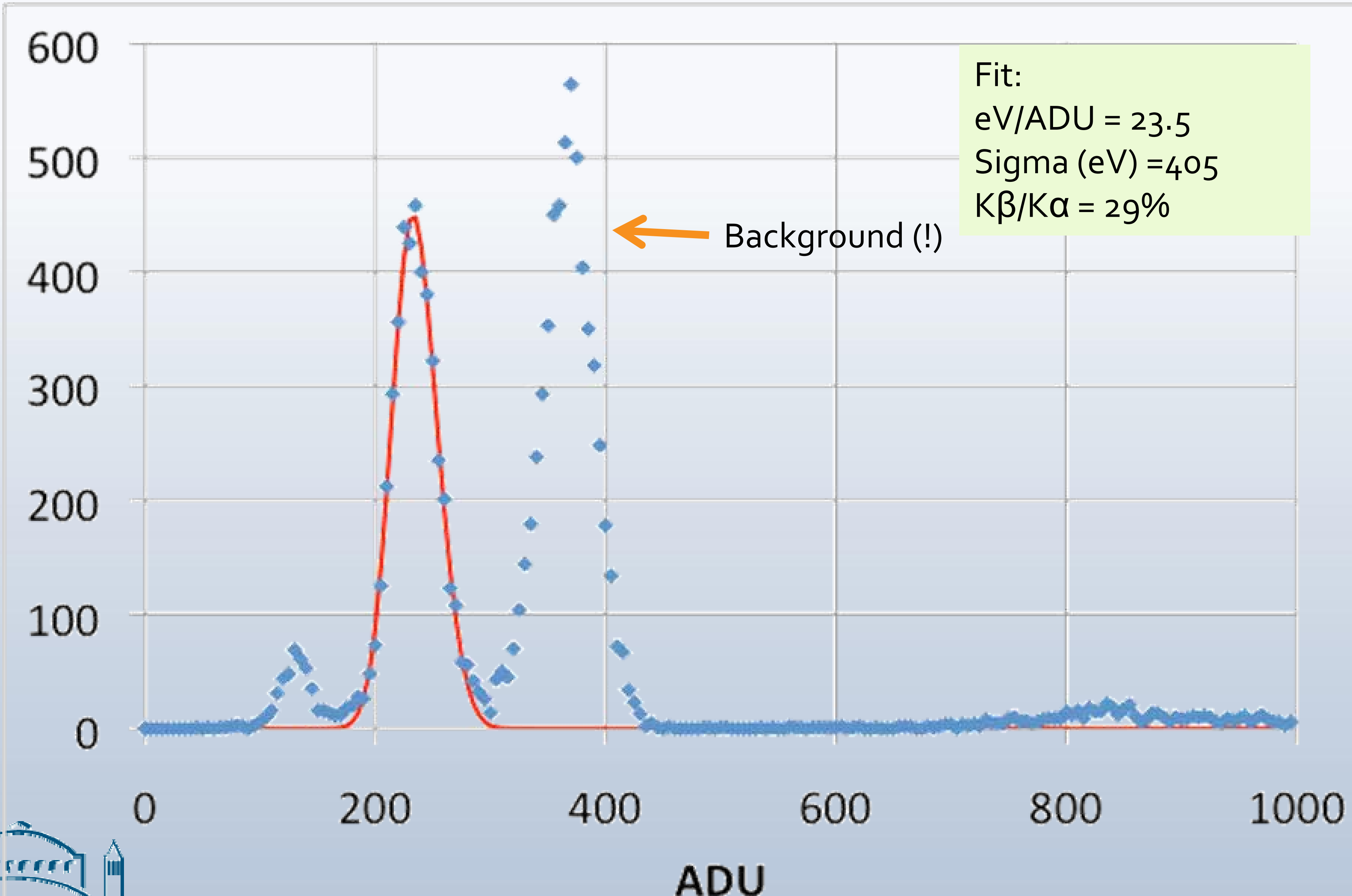
New substrate, Forced x8

V - transmission



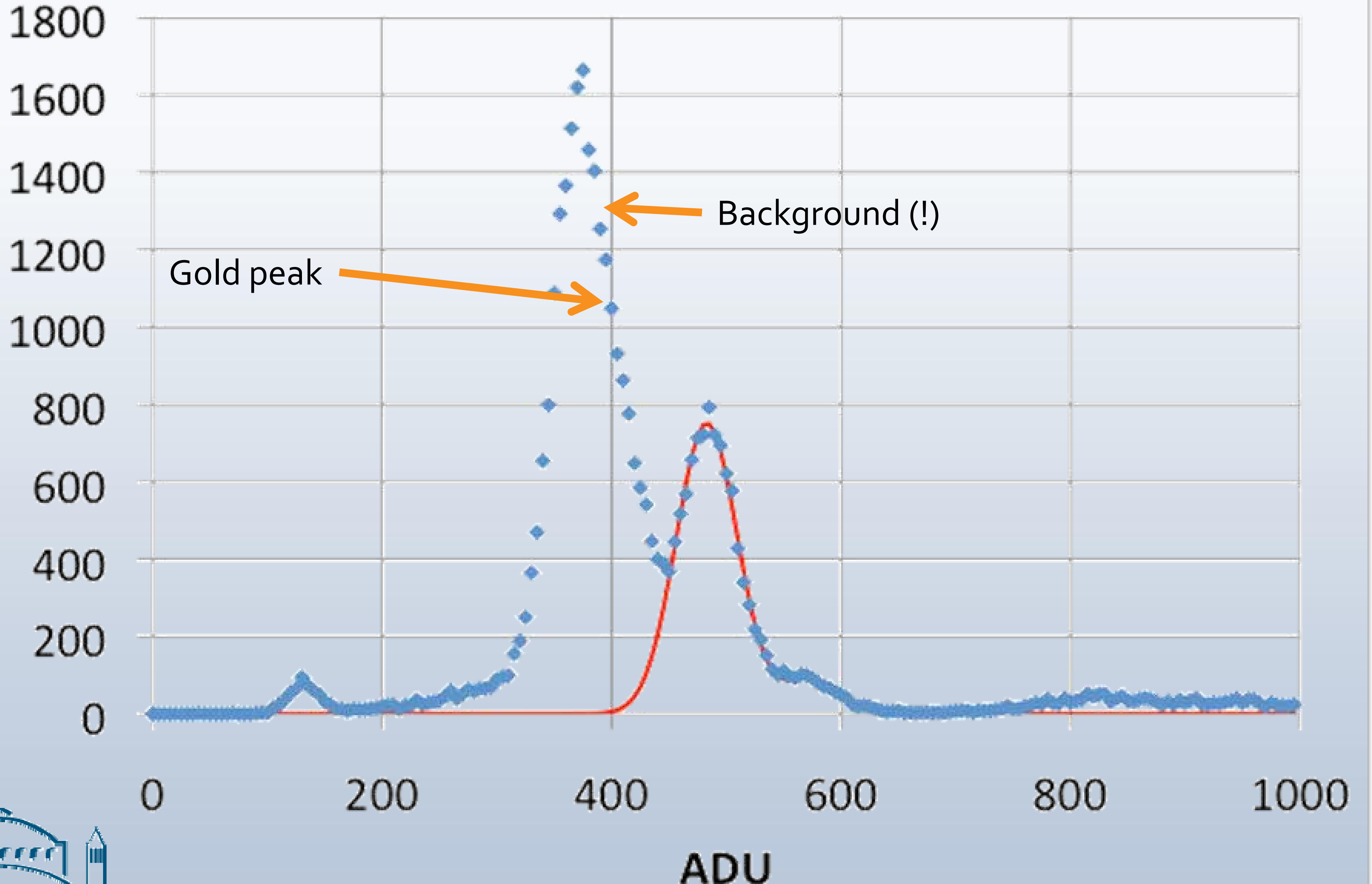
New substrate, Forced x8

Cr - transmission



New substrate, Forced x8

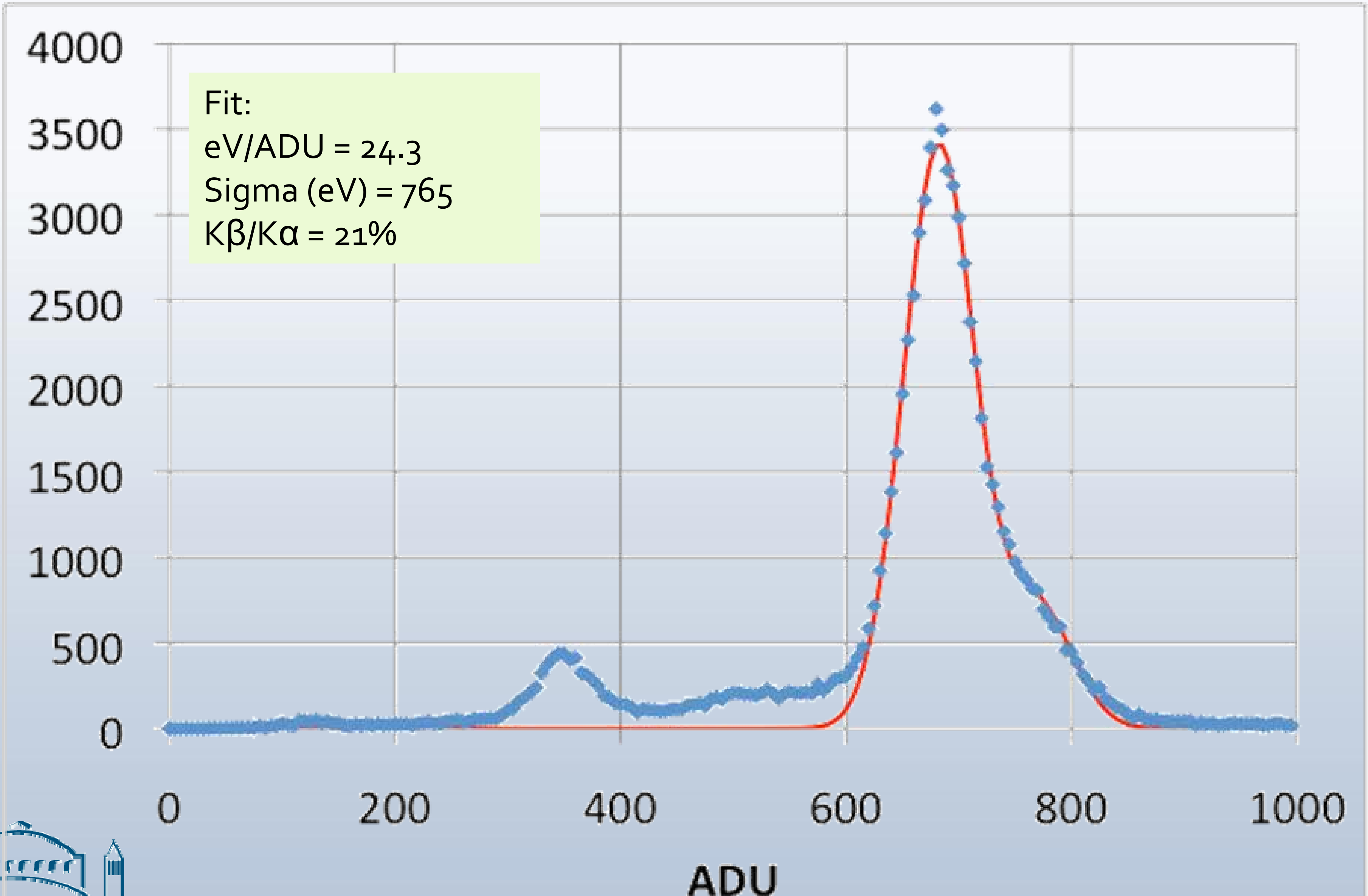
Au - transmission



P. Denes 01/09

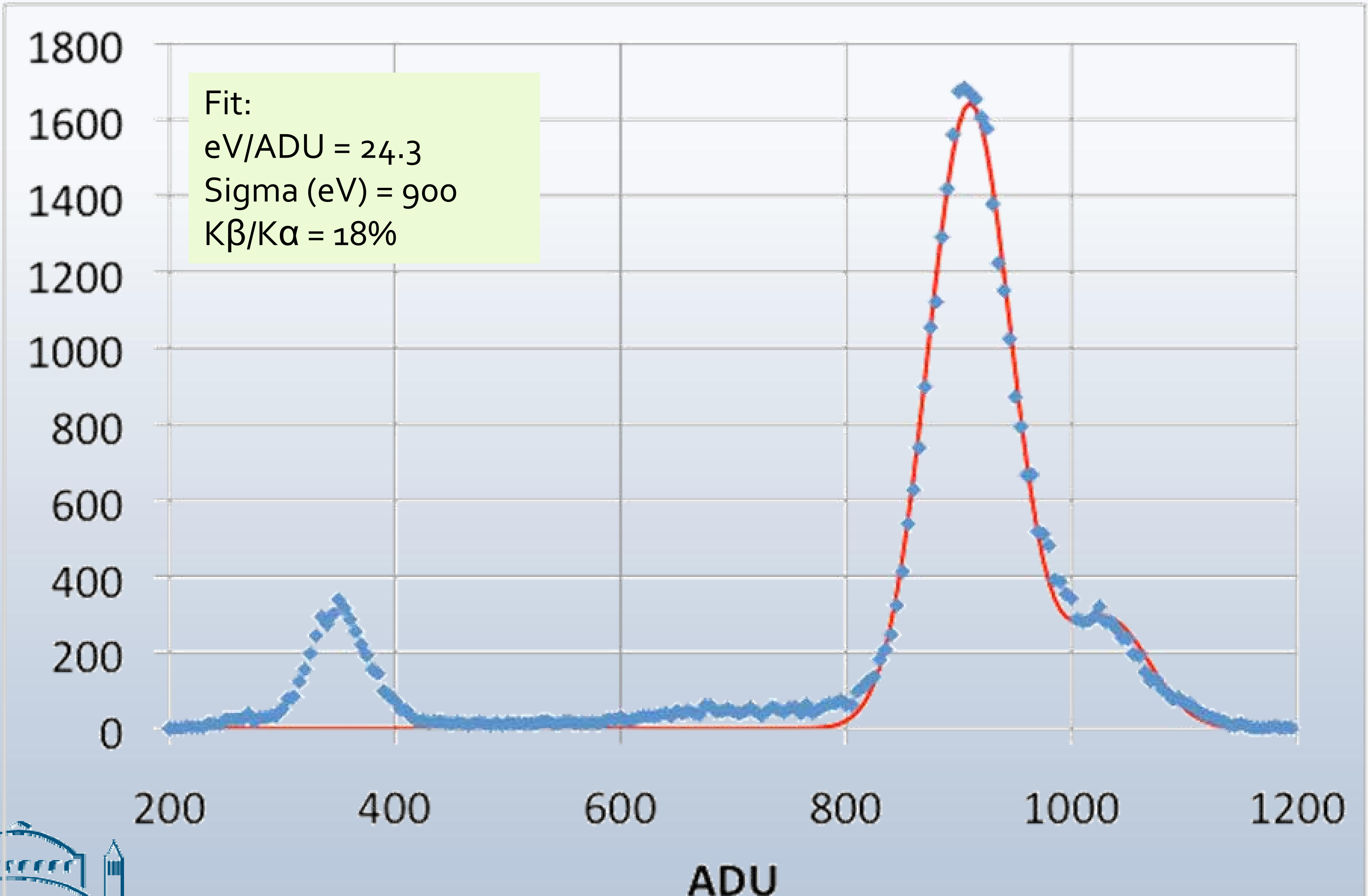
New substrate, Forced x8

Nb- backscatter



New substrate, Forced x8

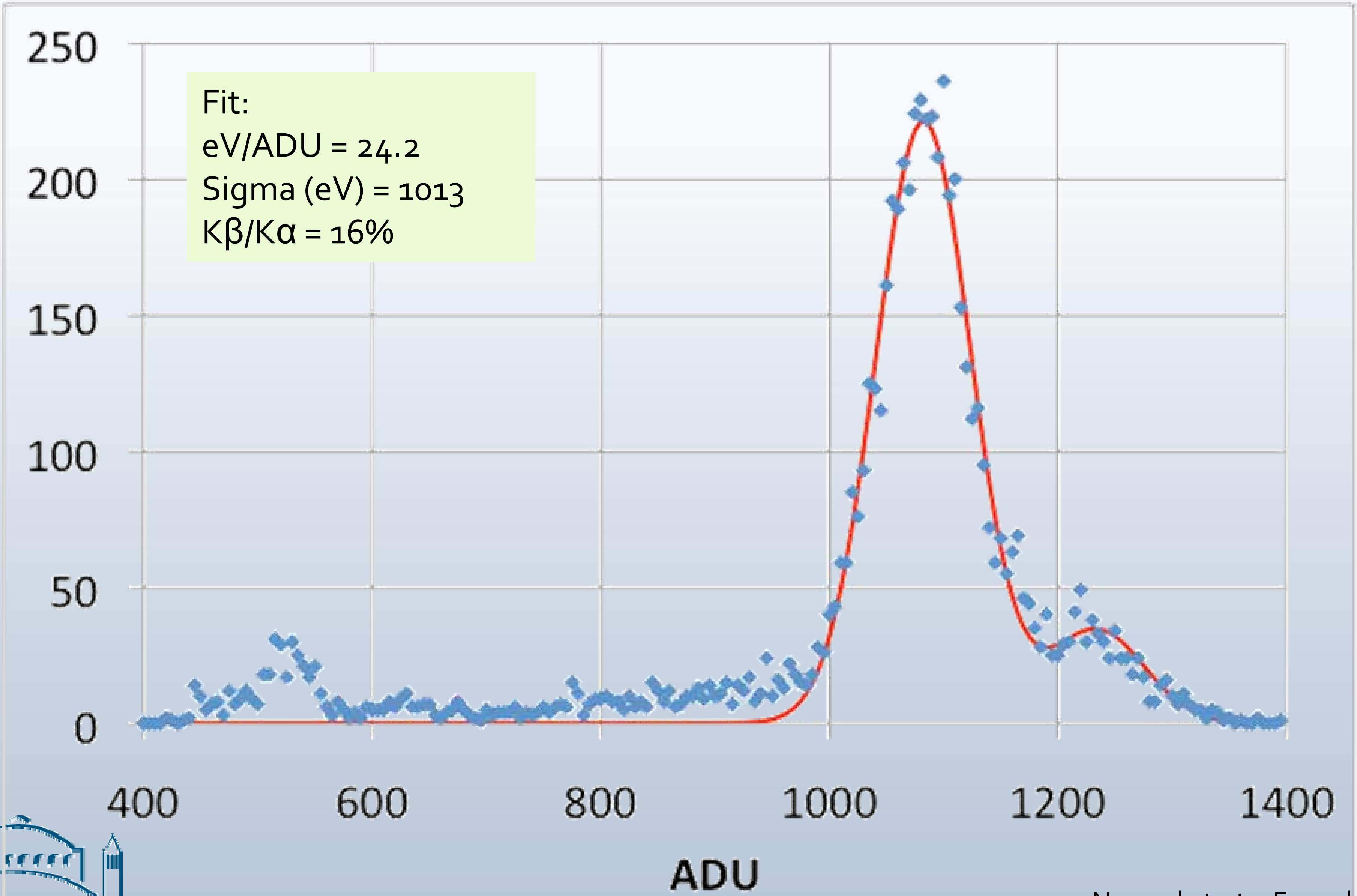
Ag - backscatter



P. Denes 01/09

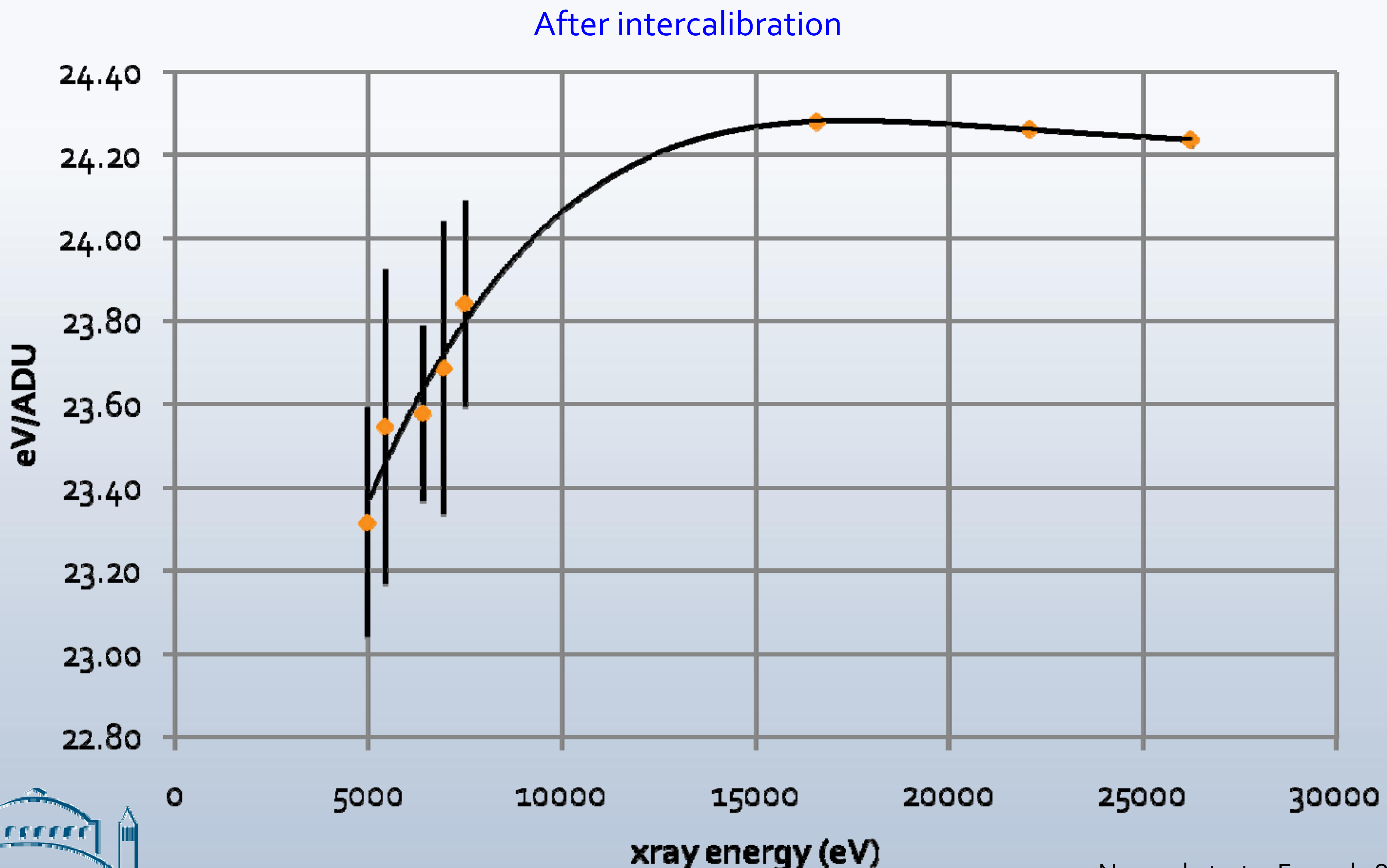
New substrate, Forced x8

Sb - backscatter



New substrate, Forced x8

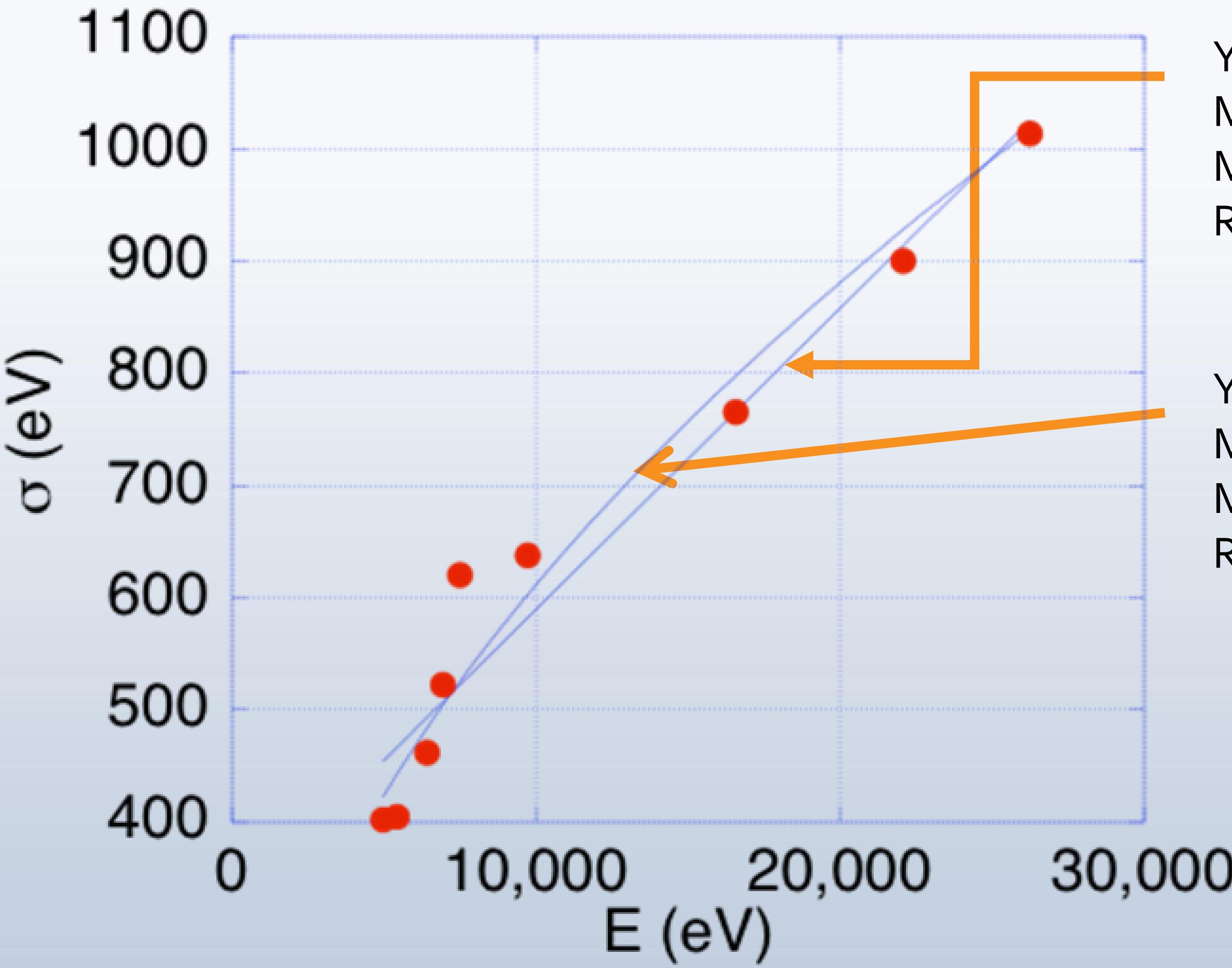
Calibration



P. Denes 01/09

New substrate, Forced x8

Resolution (S_4)



Y = M0 + M1*X
M0 321.38
M1 0.026824
R 0.9723

Y = M0*XM1
M0 4.8072
M1 0.52617
R 0.98099

Linear? Square Root?

New substrate, Forced x8

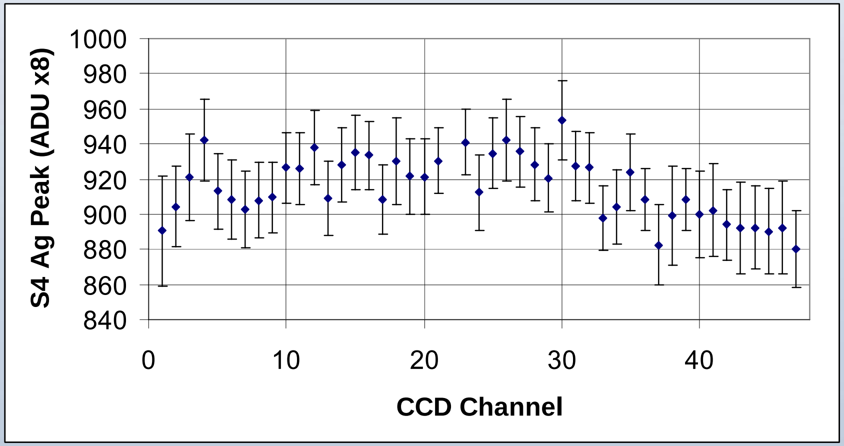
Pause

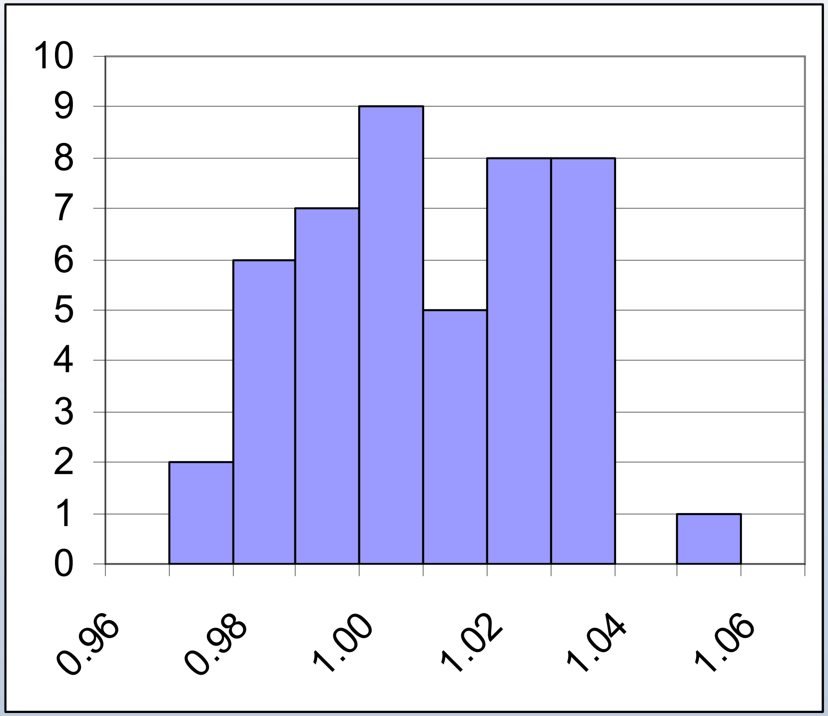
- Old and New substrates have same gain
  - Old: 90 eV/ADU (x2)
  - New: 24 eV/ADU (x8)
- Both have small spread (~2%) in output uniformity
- Noise is not great
- "Simple resolution" is not great (*far* from "Fano-limited")
- Focus a bit on resolution

Simple calibration

Some more data taken just before the shutdown. Several thousand exposures (all in "backscatter" geometry). Forced x8, T = -90C, T_{INT} = 50 ms
(so several thousand exposures = a few minutes!)
Goal – try to understand resolution

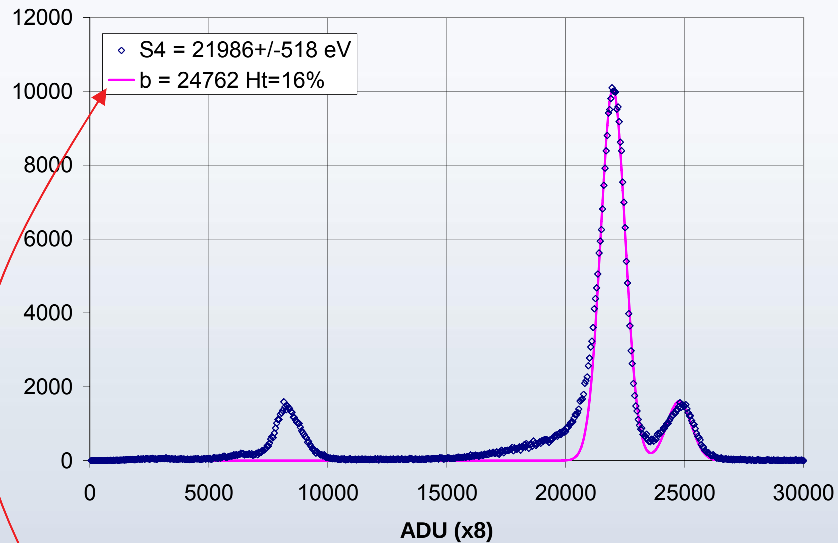
Line up all of the S4 peaks from each CCD output for Ag target (22 keV)



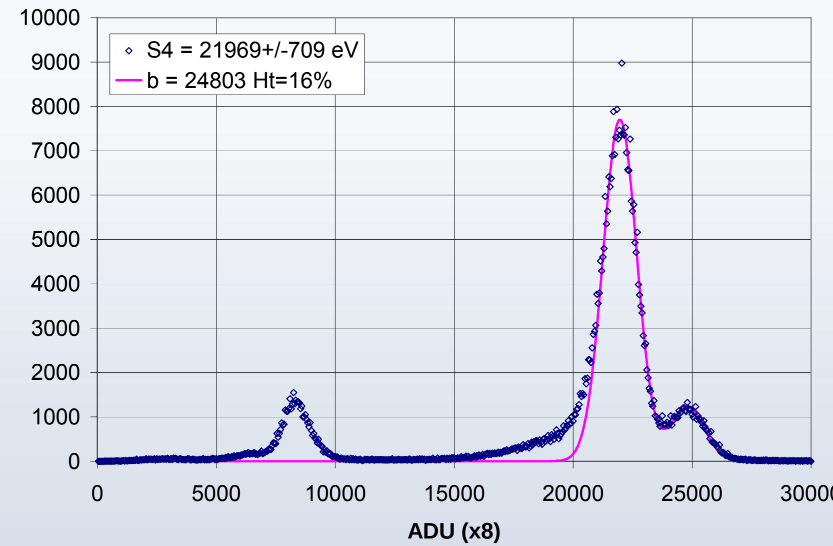


Ag – "calibration is better than no calibration"

(Ag) Calibration Constants



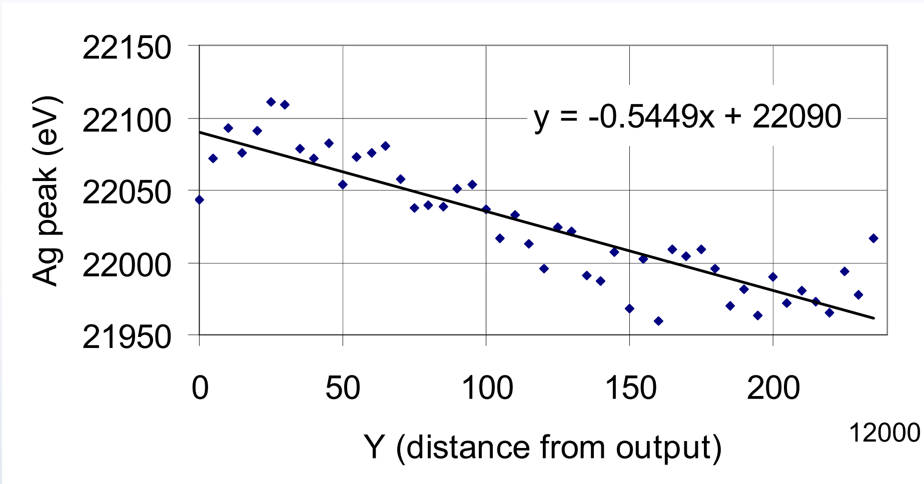
No Calibration



Fit to 2 Gaussians with independent amplitude and mean, but same σ
Legend = main peak at 21,986 eV with σ = 518 eV; secondary peak at 24,762 eV and amplitude 16% of main peak

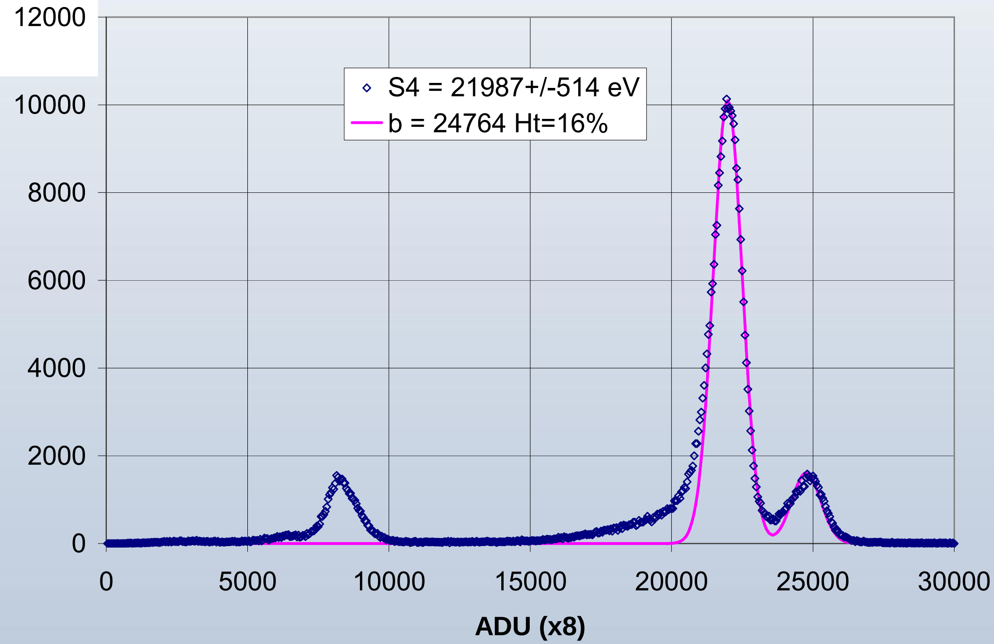
New substrate, Forced x8

Ag with linear y-correction



There is a small (0.6%) effect in y (presumably CTE)

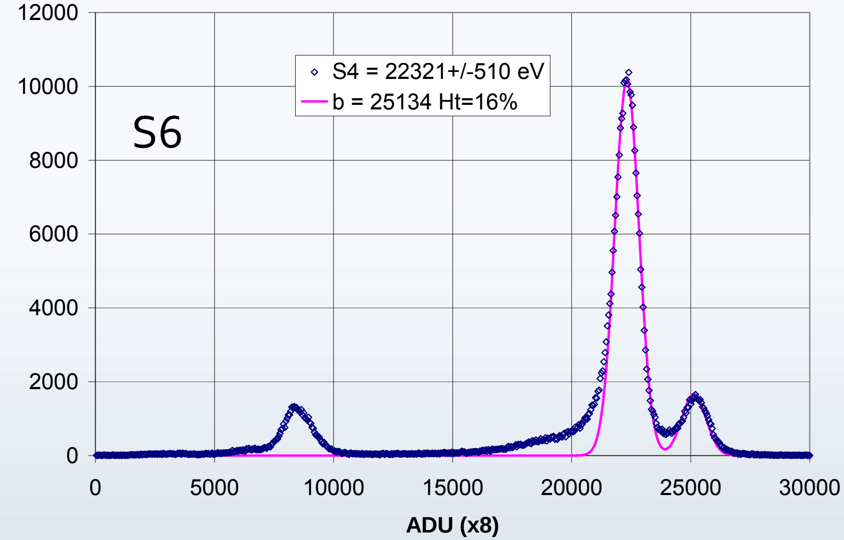
Correcting the 0.6% effect does not change overall resolution

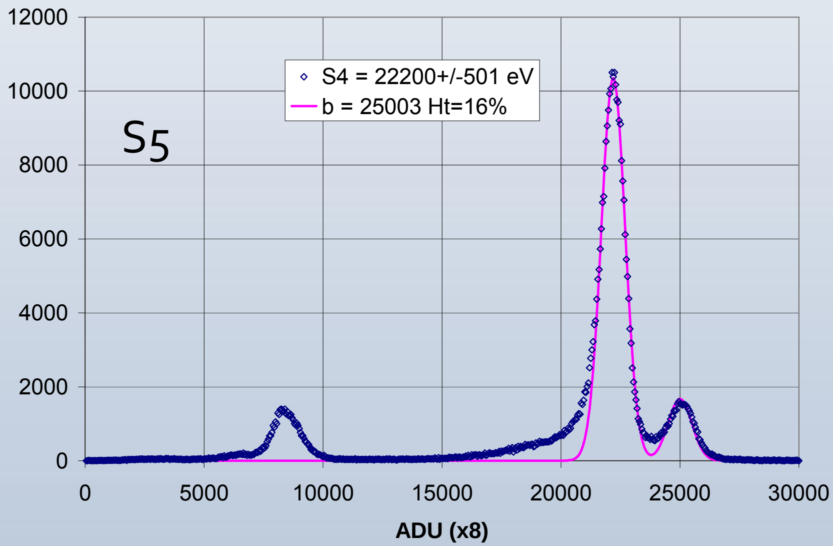


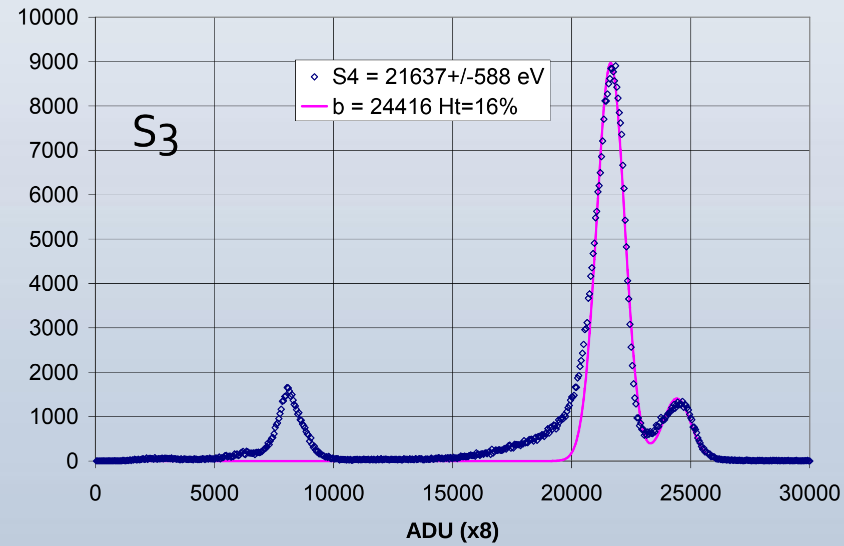
New substrate, Forced x8

Ag – S3,S5, S6

S4, S5, S6 roughly the same
S3 clearly worse

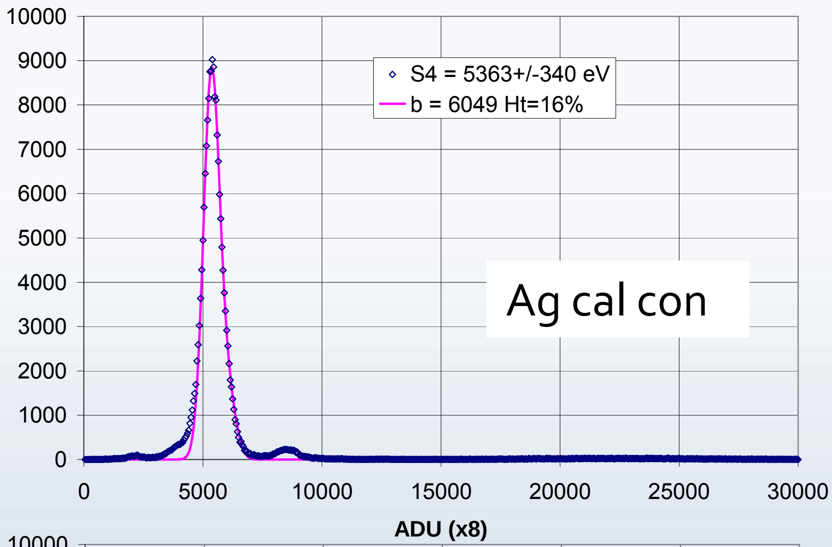


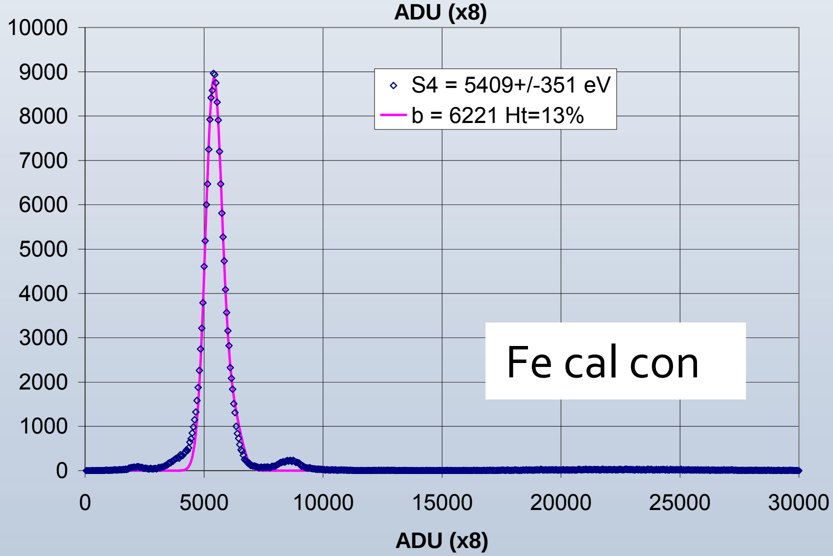


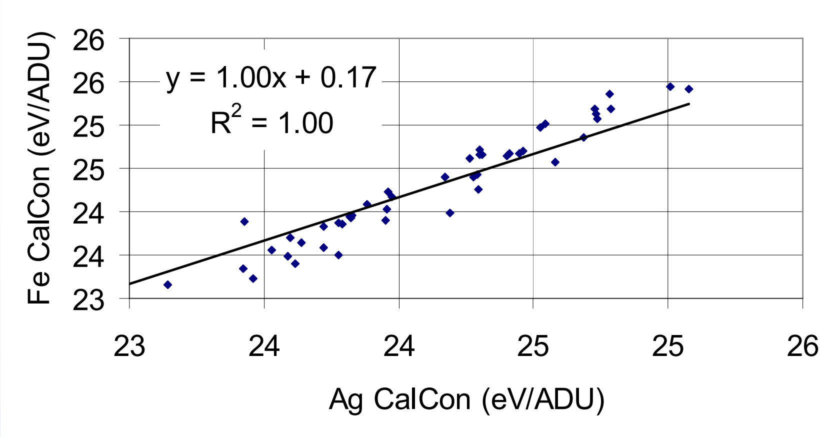


New substrate, Forced x8

Low/High energy calibration? -- Cr



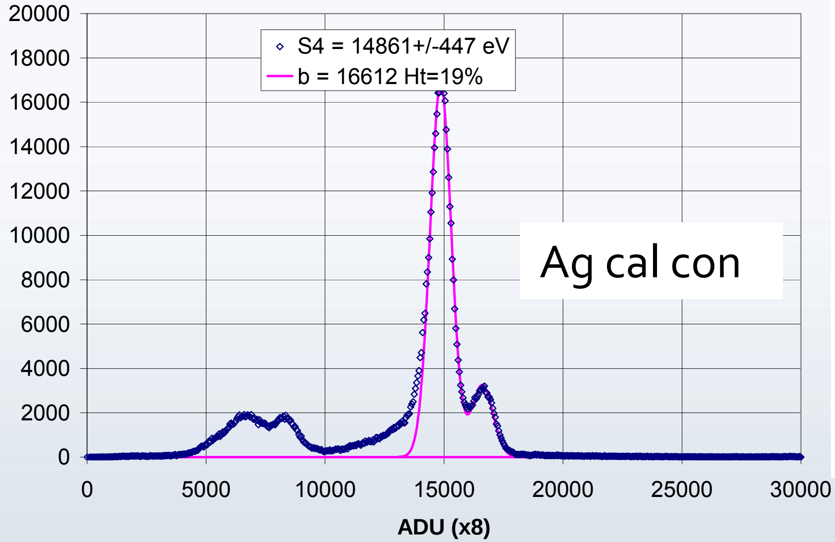


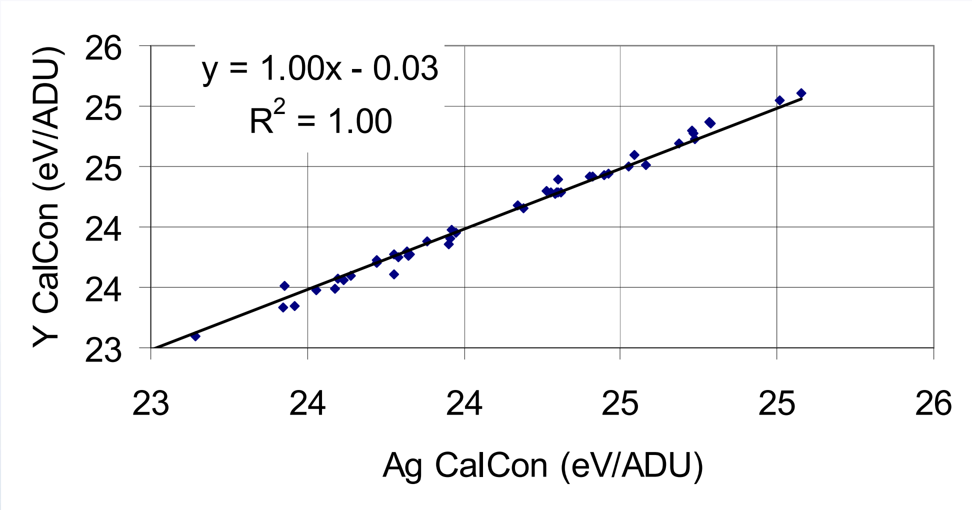


Compare Ag and Fe calibration constants

New substrate, Forced x8

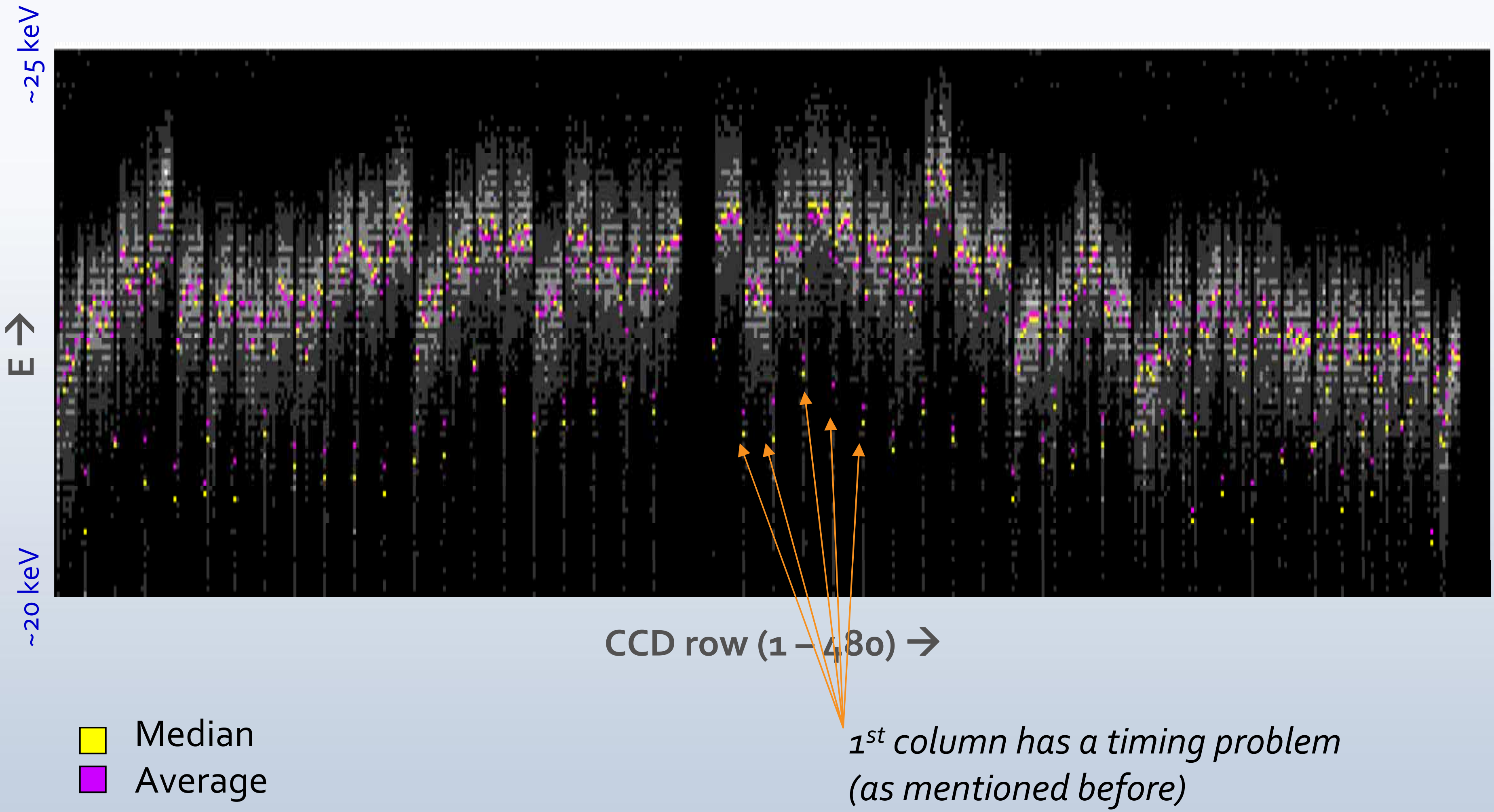
Y





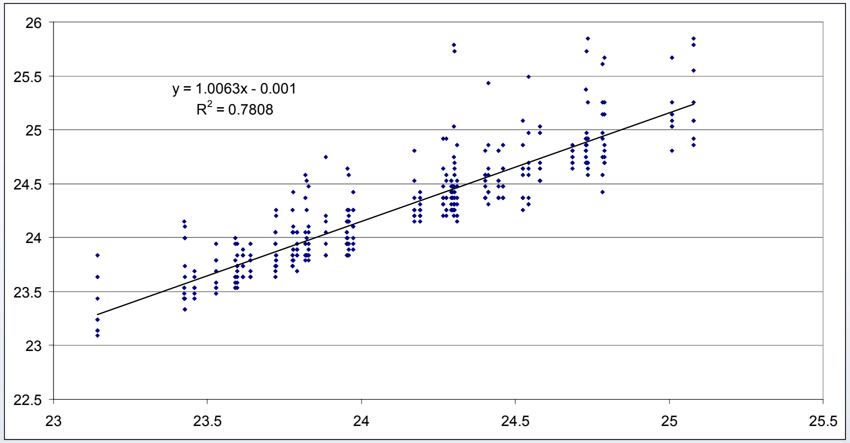
Compare Ag and Y calibration constants

Sub-structure? Scatterplot for Ag (raw)

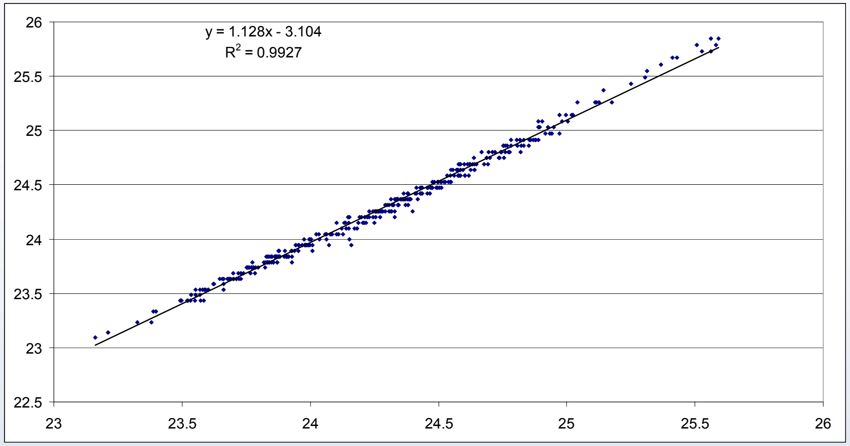


New substrate, Forced x8

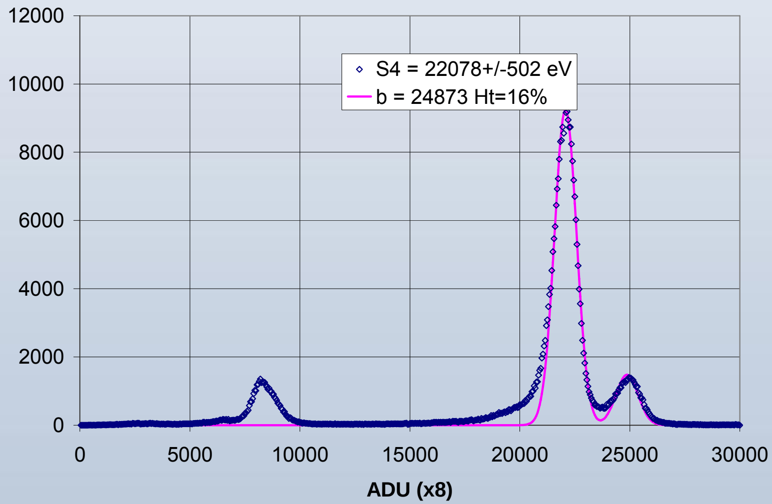
Ag: Calibrate more finely – row-by-row



Median of each row vs CalCon



Median of each row vs Average

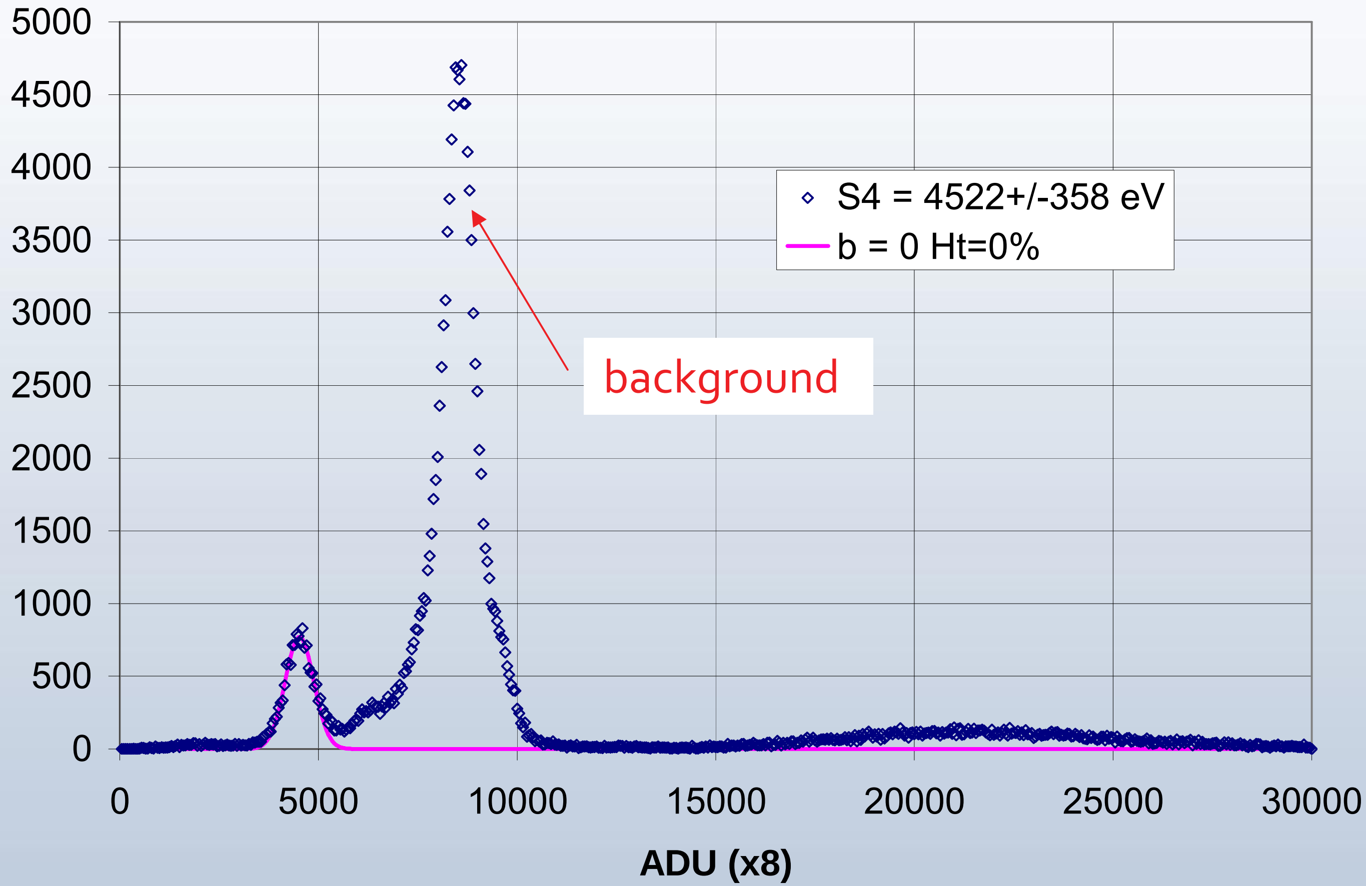


Use median of each row as calibration

These are all sub-percent tweaks to 2% resolution

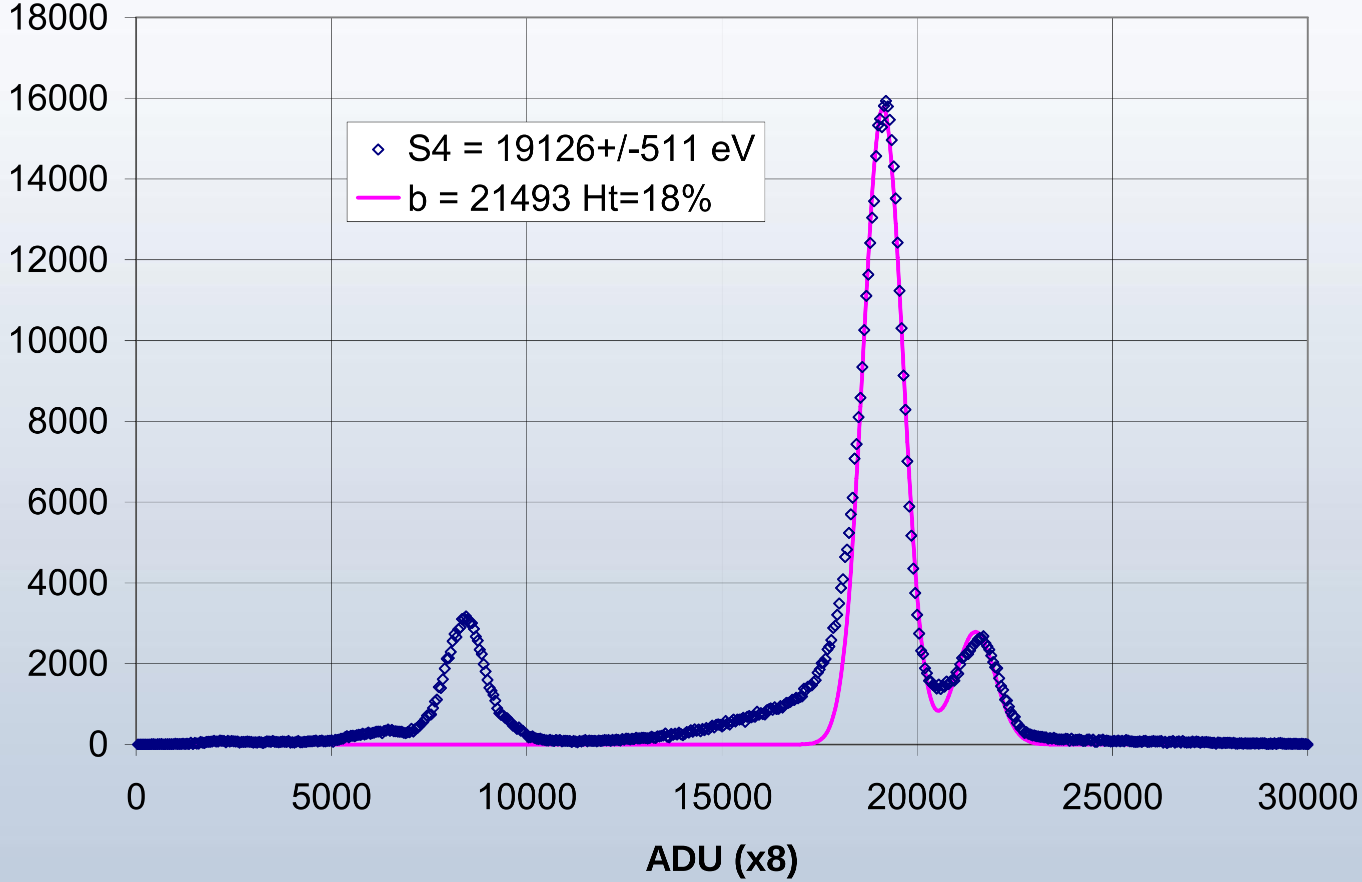
New substrate, Forced x8

Ti



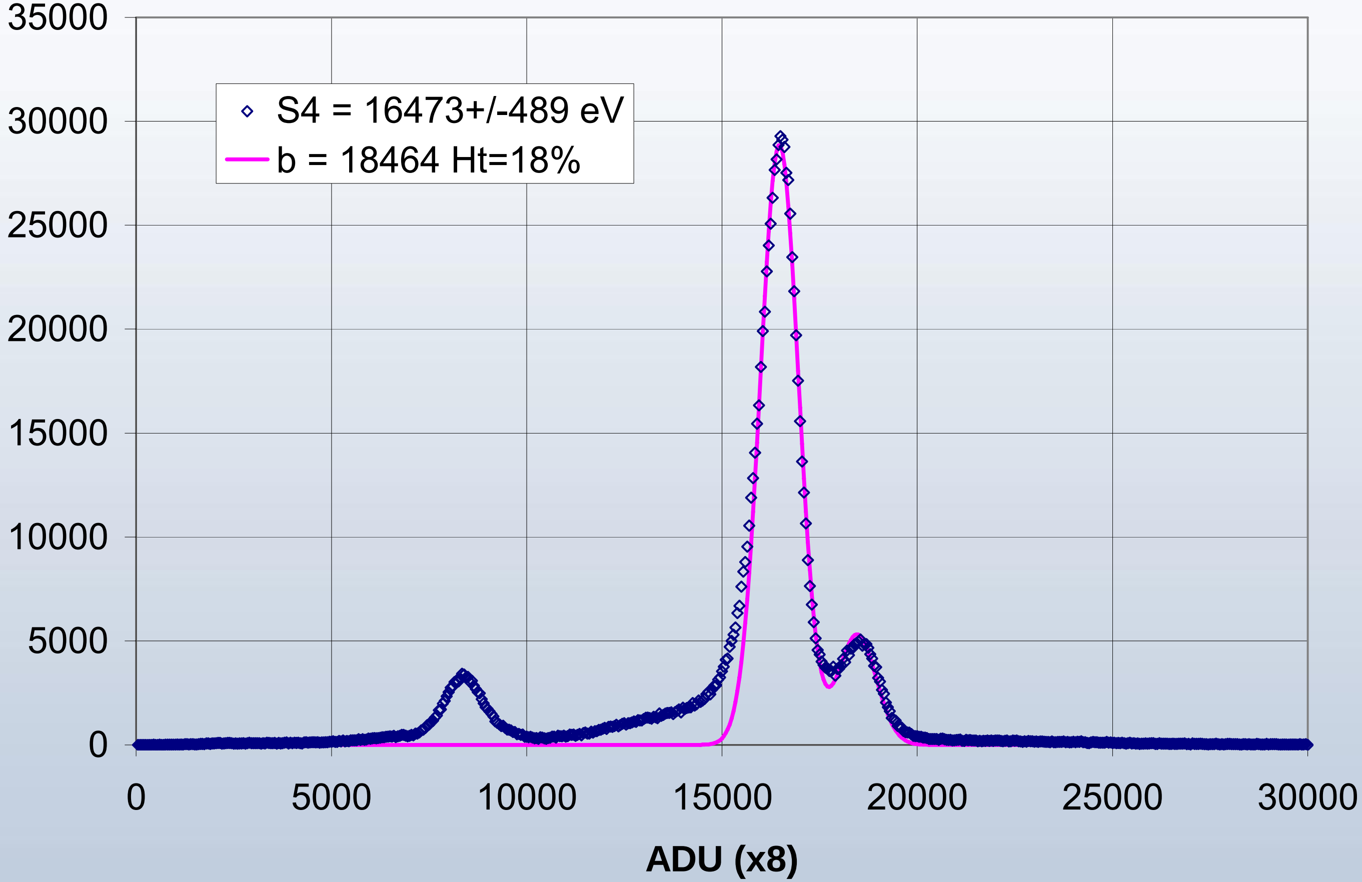
New substrate, Forced x8

Ru

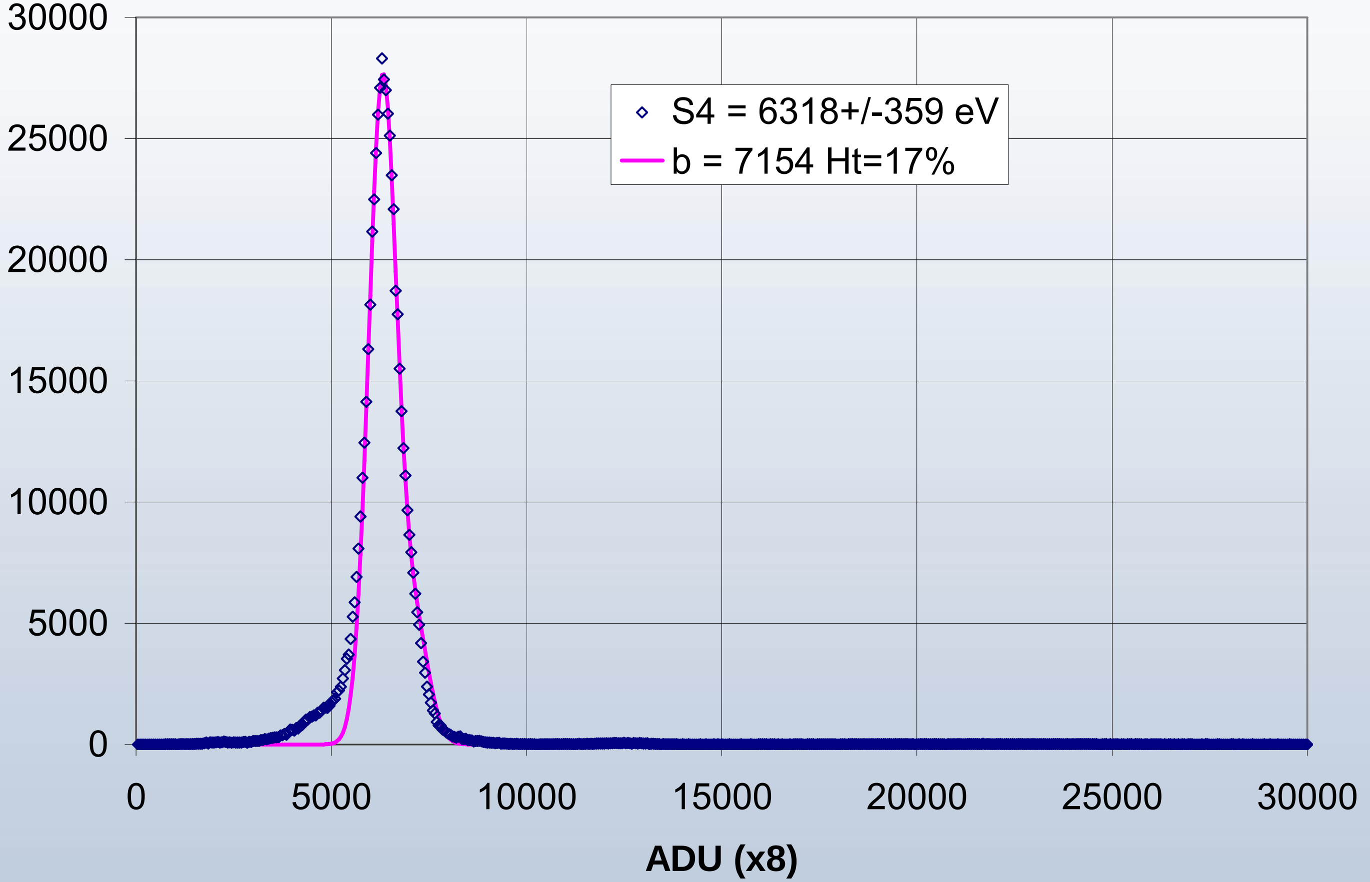


New substrate, Forced x8

Nb

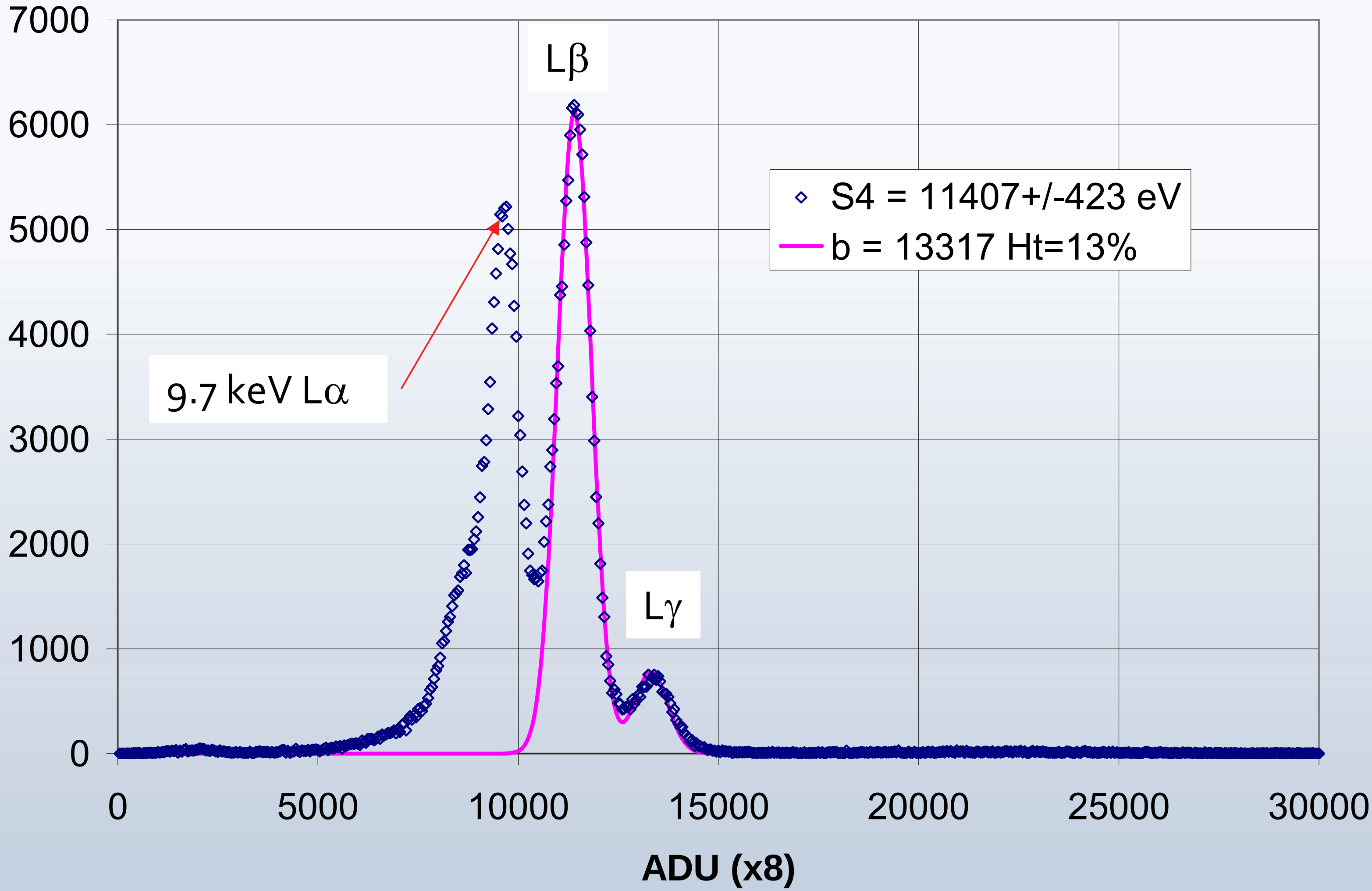

35000
30000
25000
20000
15000
10000
5000
0
0
5000
10000
15000
20000
25000
30000
ADU (x8)
S4 = 16473+/-489 eV
b = 18464 Ht=18%

Fe



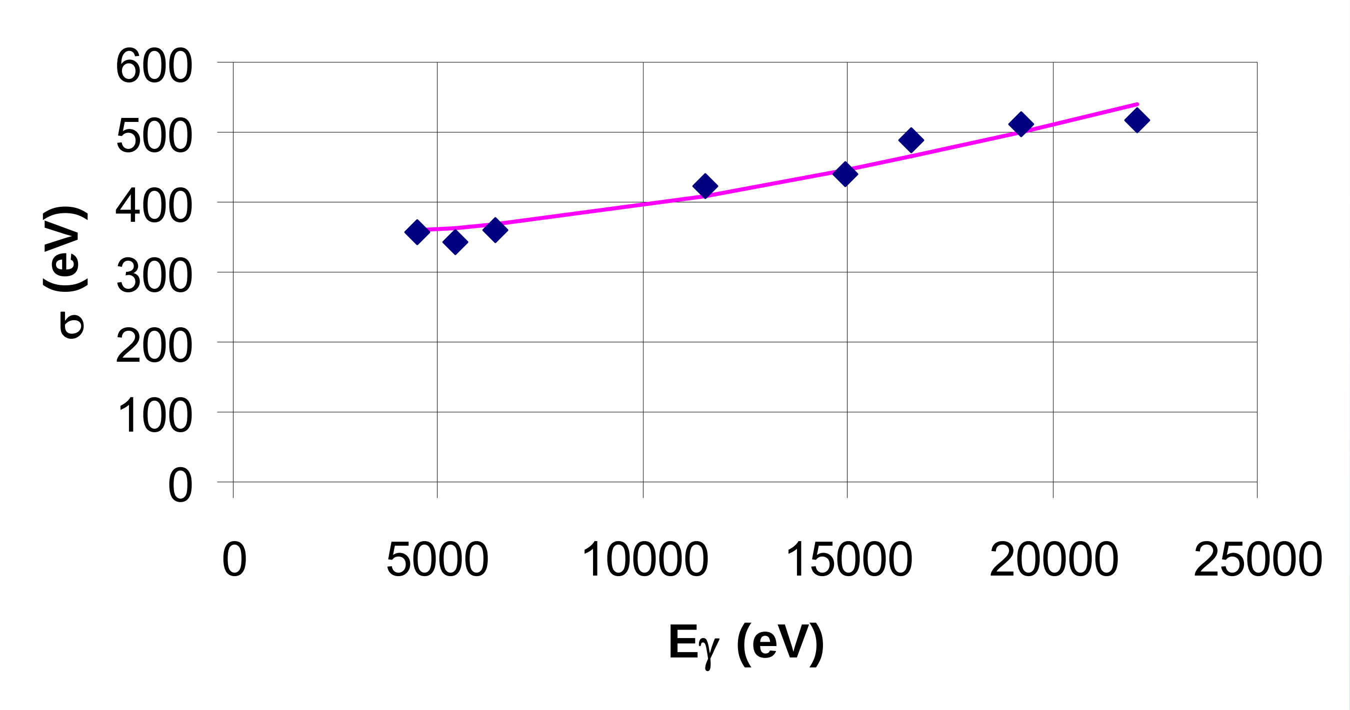
New substrate, Forced x8

Au



Mono set to 9.8 keV – perhaps calibration is a bit off …

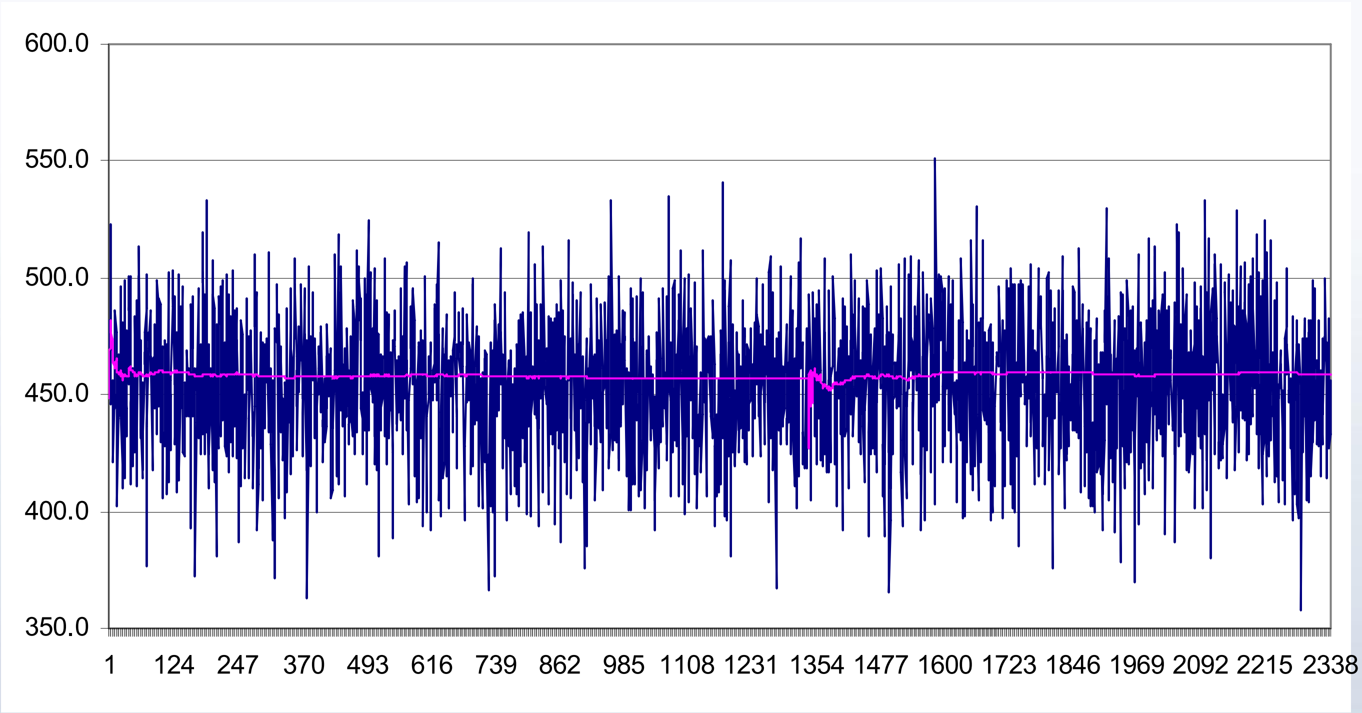
Resolution vs. E



Fit to $a \oplus bE$
a = 350 eV
b = 0.019

⇒Noise ~ 175 eV/pixel (factor 3 too high)
b should be zero. Could power supply noise cause gain fluctuations? (e.g. if V_{RESET} moves up and down, current through output transistor changes, so g_m changes, …)

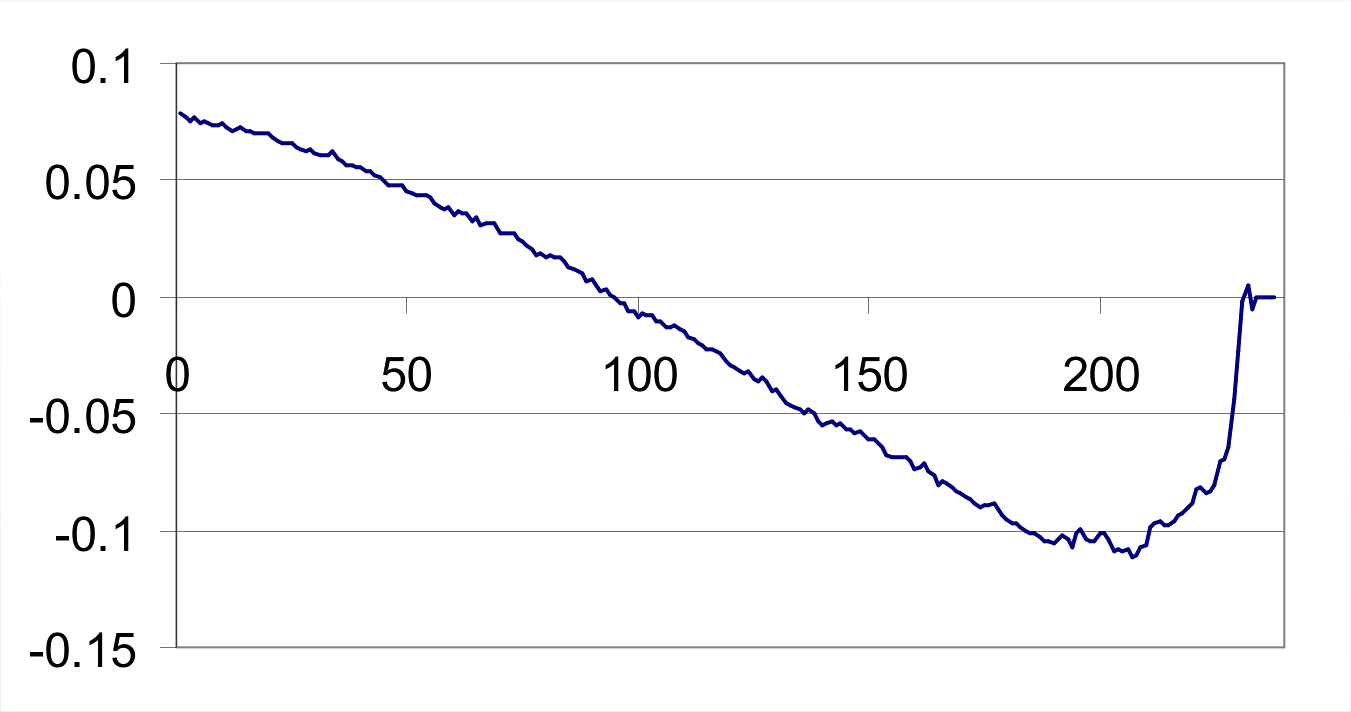
Long-term variation?



Each “exposure” for Ag has about 90 photons within 2σ of the peak
The plot above shows the RMS value per exposure (for hits within 2σ)
and the running RMS
FFT and autocorrelation don’t show anything…

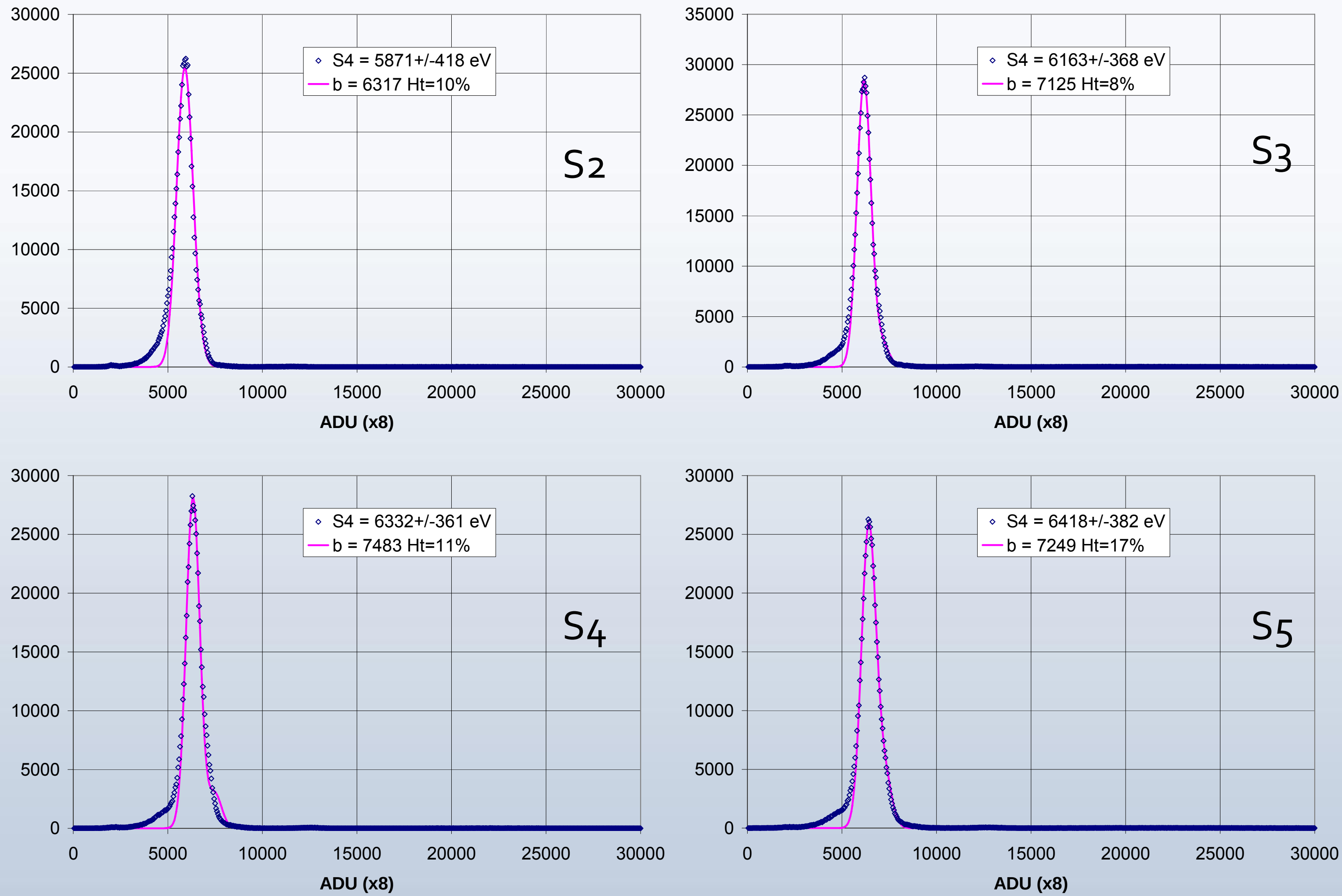
New substrate, Forced x8

Autocorrelation



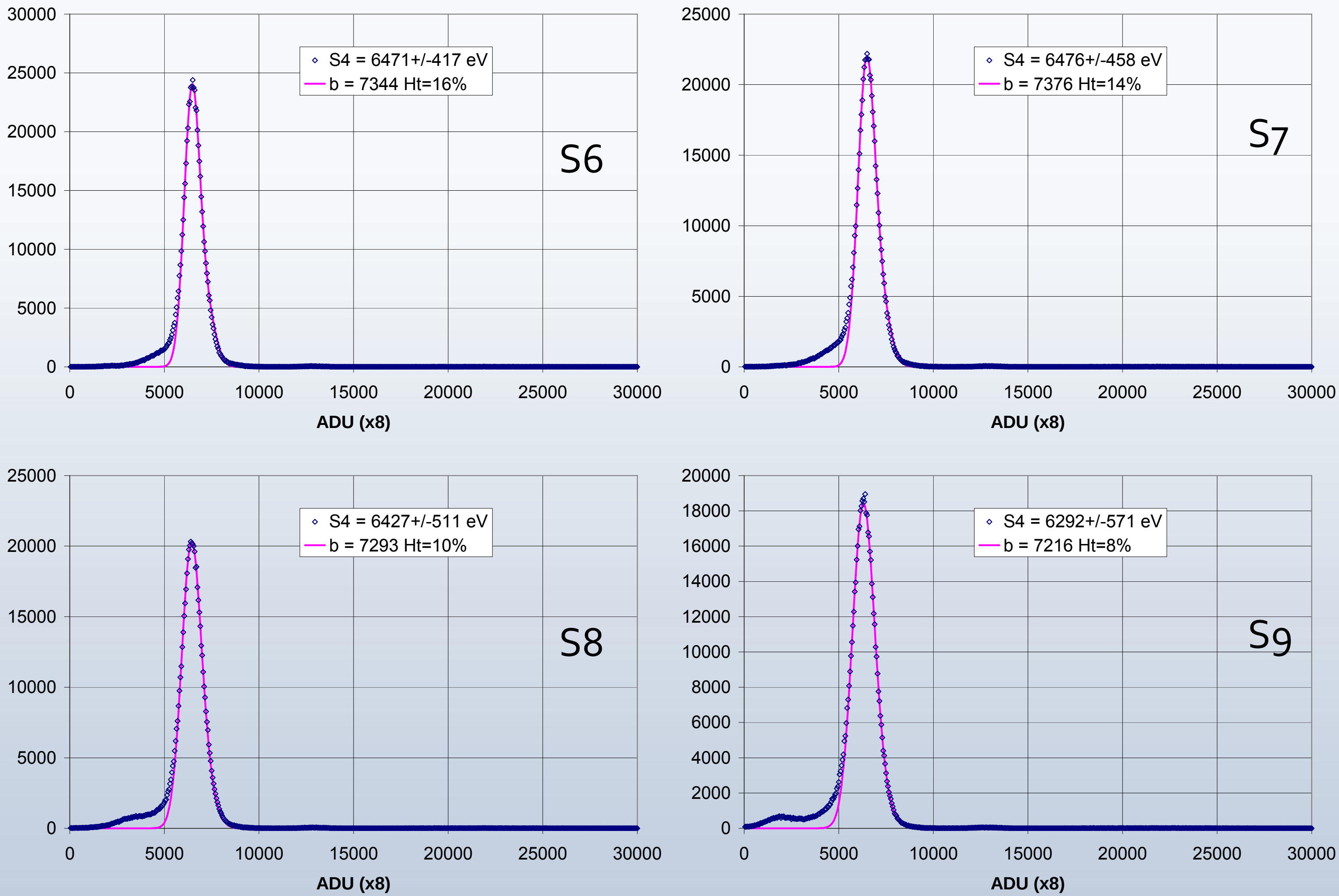
Autocorrelation (for all Ag data) looks like y-correction plot
(so there is no obvious variation on the time scale of the vertical shift clock)

Fe – S2, S3, S4, S5



New substrate, Forced x8

Fe – S6, S7, S8, S9

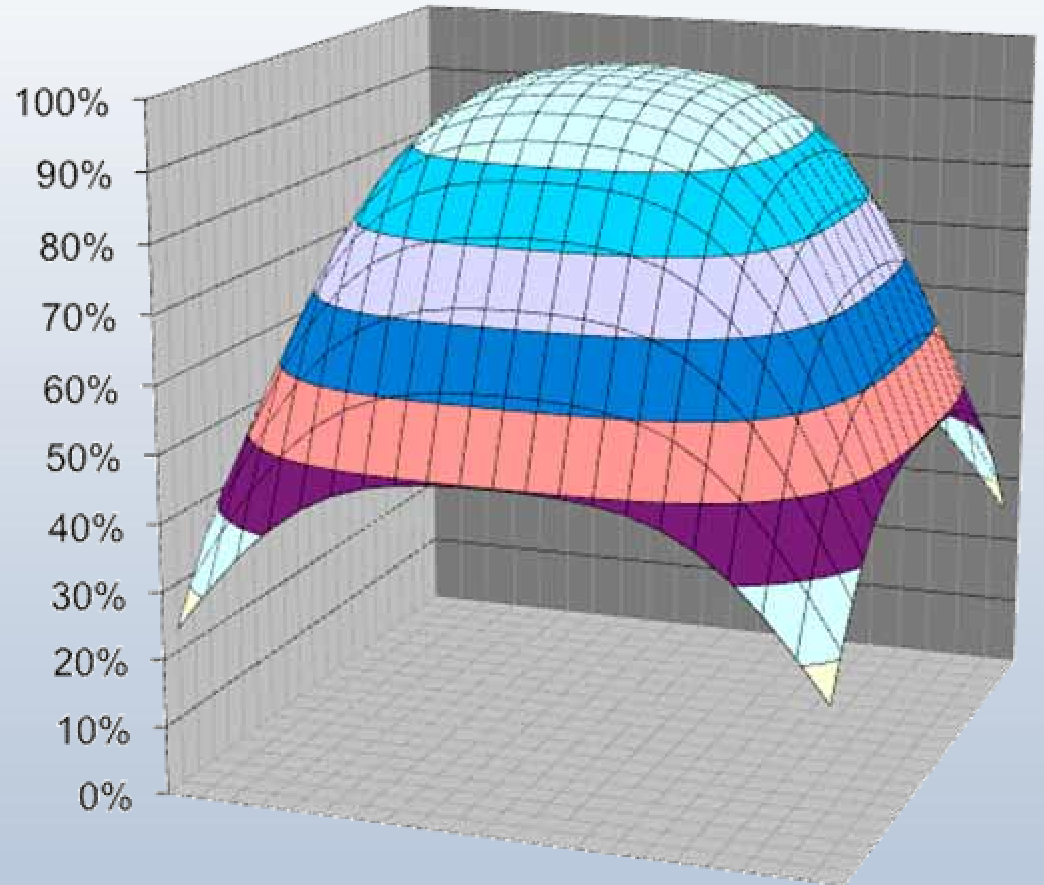


New substrate, Forced x8

Charge sharing – what *should* it be?

Much help from Chris Bebek in understanding "features" of these CCDs. A key difference between our CCD and the SNAP CCD is that for us, pixels are 30 μm and for SNAP they are 10 μm. PSF from diffusion is assumed to be σ = 5 μm → so summing over many pixels is obligatory for SNAP, but not (?) for us (?).
Some comments:

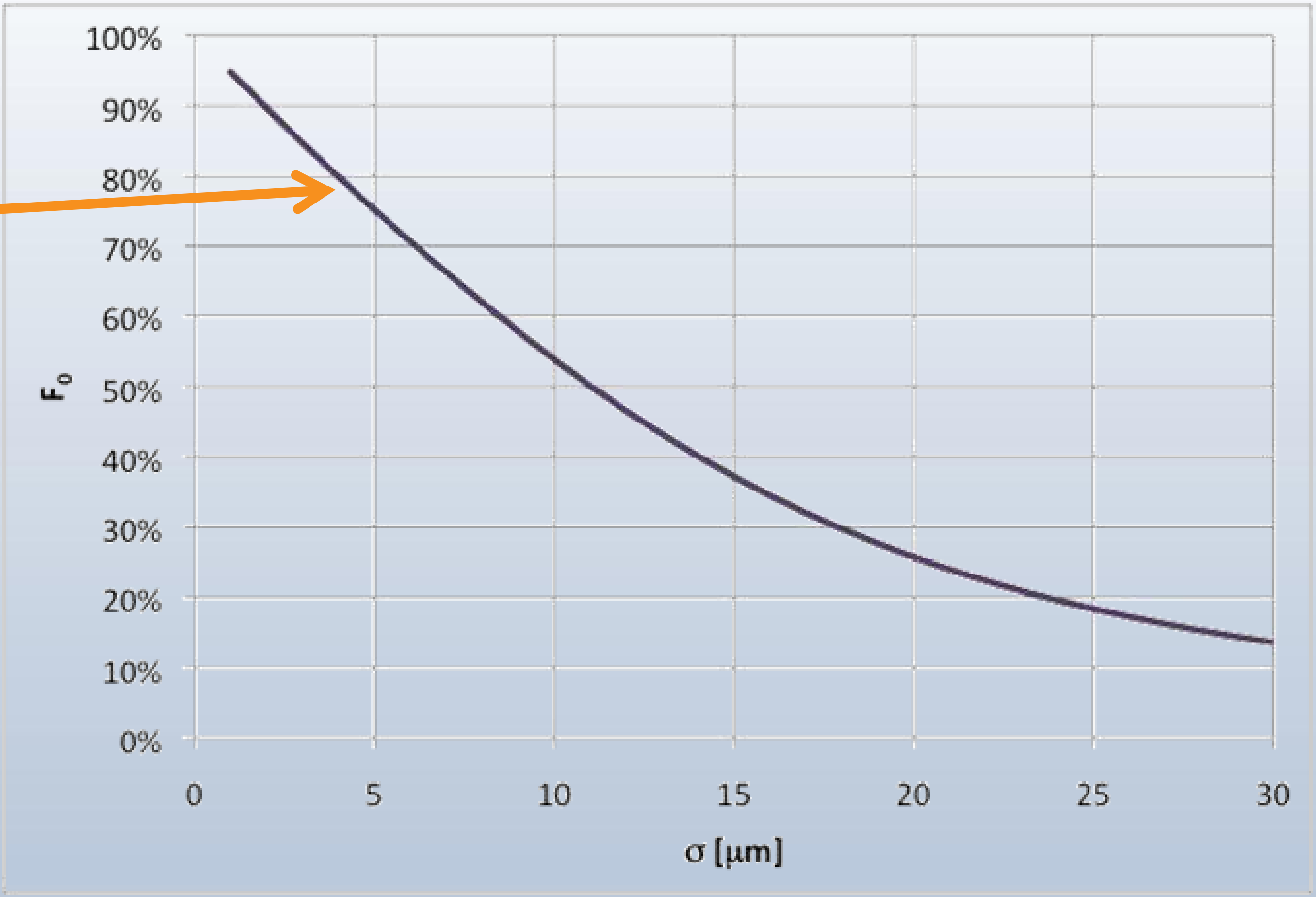
Assume that the "charge cloud" from a single incident photon has a Gaussian distribution. For a 30 μm pixel, σ = 5 μm would imply charge collection in the central pixel as shown on the right (i.e. the fraction of charge, f_o, collected in the central pixel when the photon is incident at (x_o,y_o) in the pixel



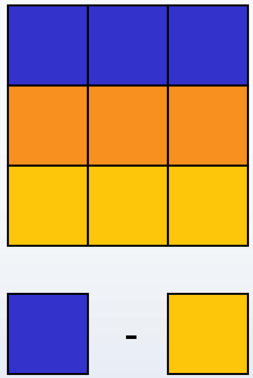
Charge sharing – what should it be?

If my arithmetic is correct, then for a pixel of pitch P, the fraction of signal in the central pixel (as a function of PSF σ) is:

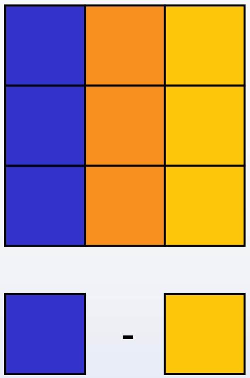
4 – 5 μm σ → 75 – 80% in the central pixel.
Not more – even though the pixel is 30 μm

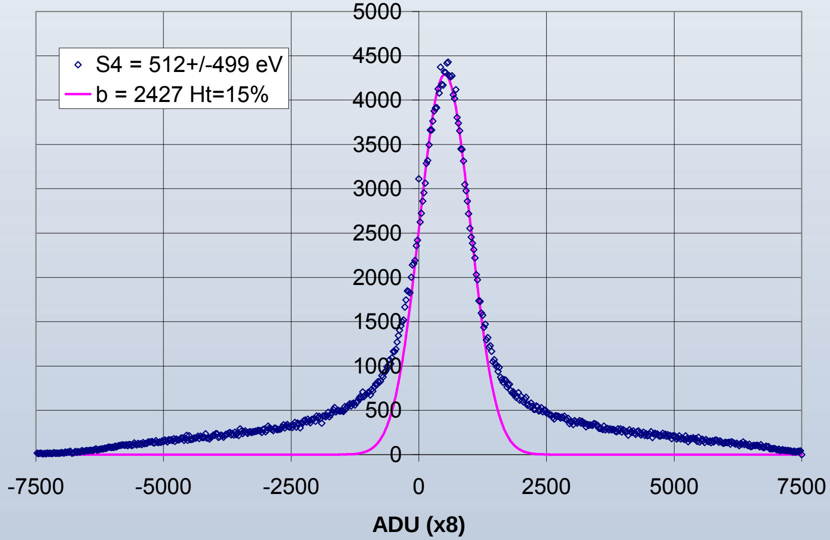


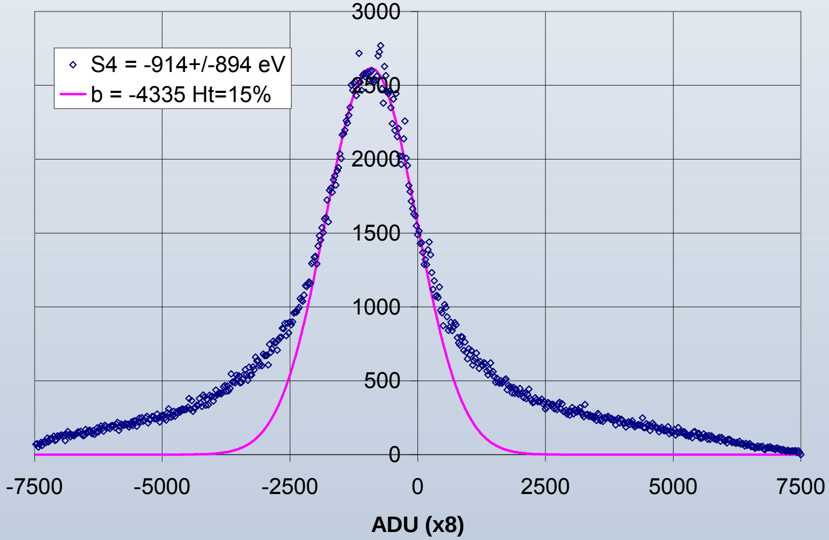
Ag – Center of Gravity (un-normalized) coordinates



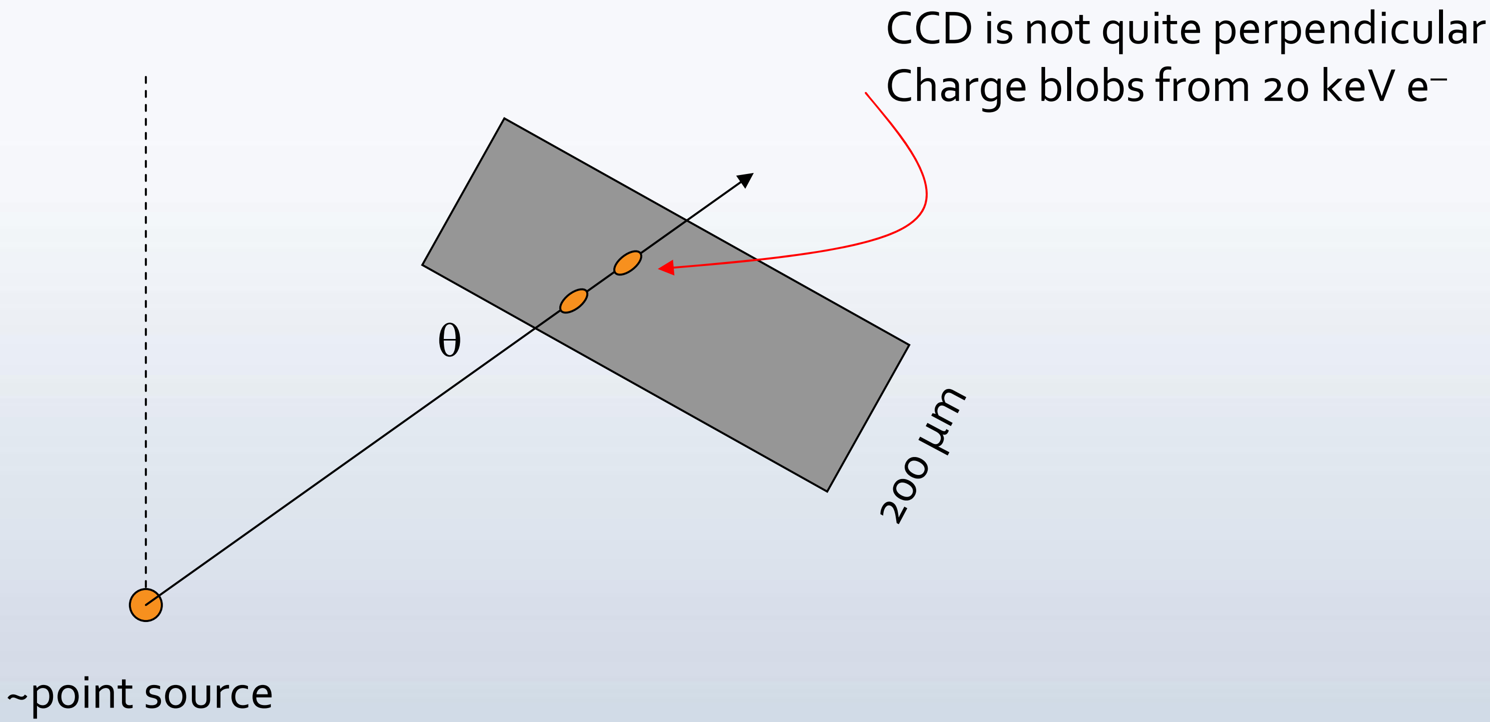
CCD y
(physical x,
CCD is at 90°)





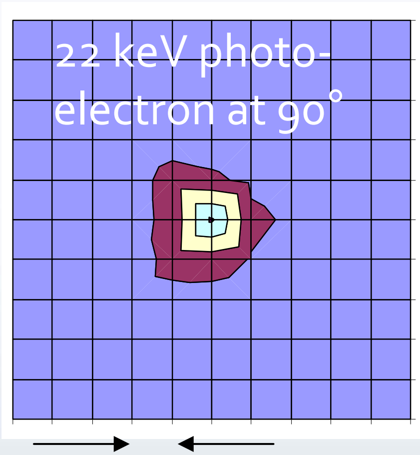


Maybe 30 μm is not so big

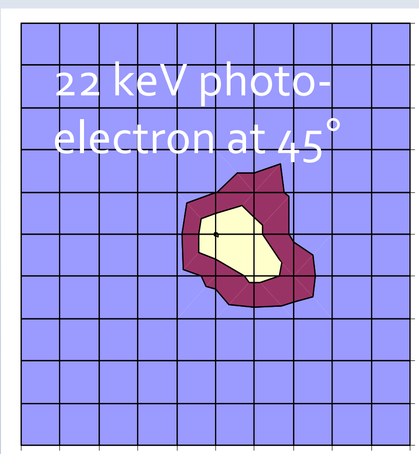


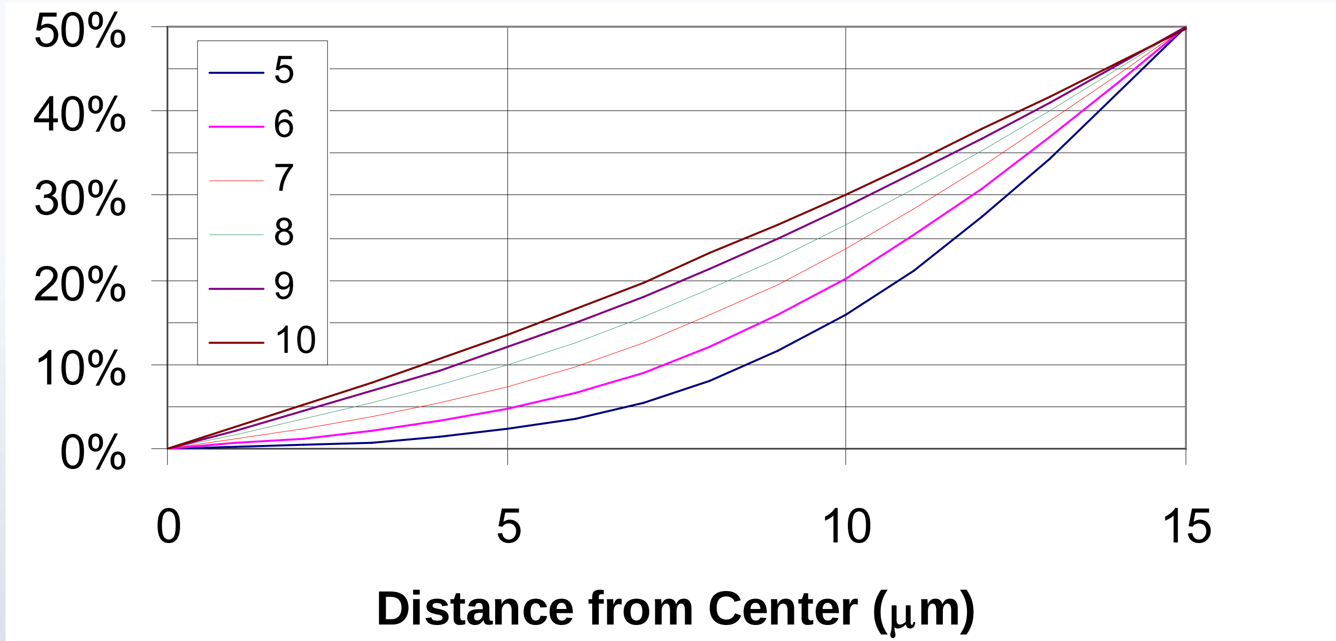
Leading to offset and asymmetry in C.O.G. coordinates (previous page)

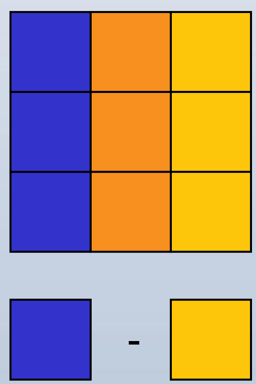
Oh yeah?



1 µm

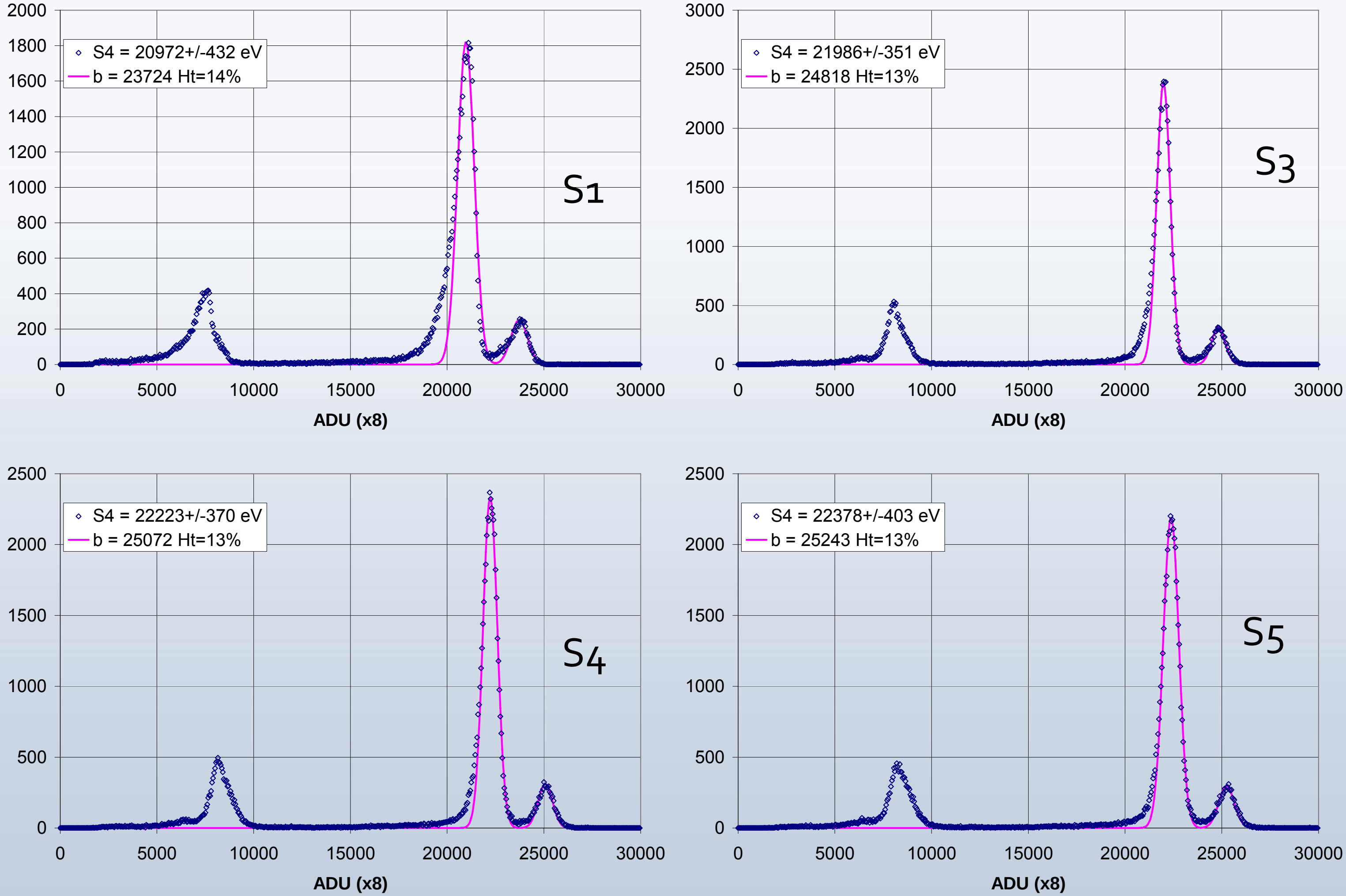




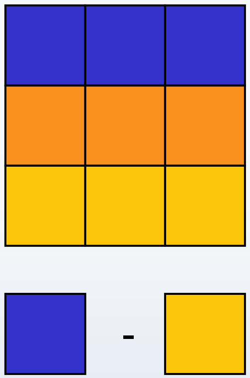


vs distance from center of 30 µm pixel for 5 .. 10 µm blob+diffusion

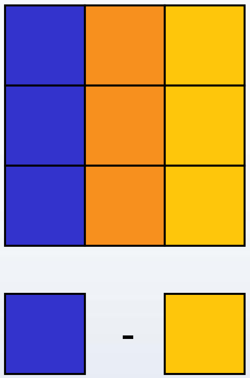
Ag – restrict to COG peak ±1 σ

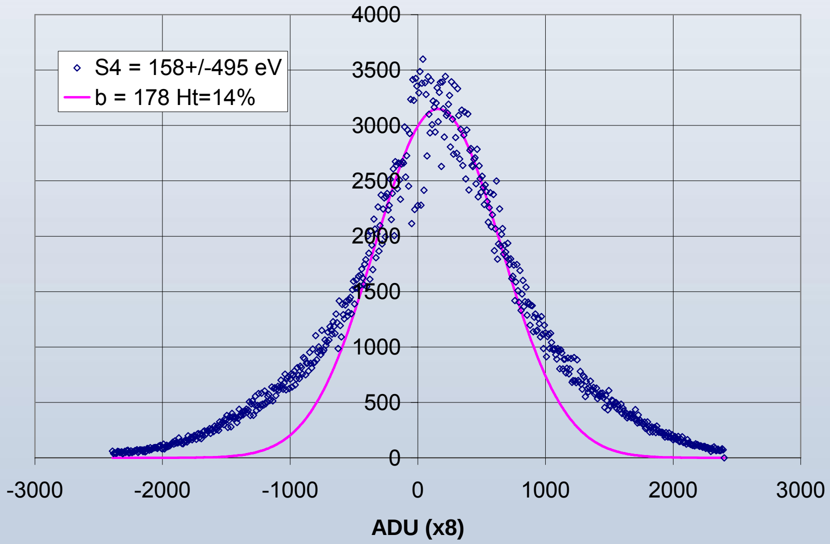


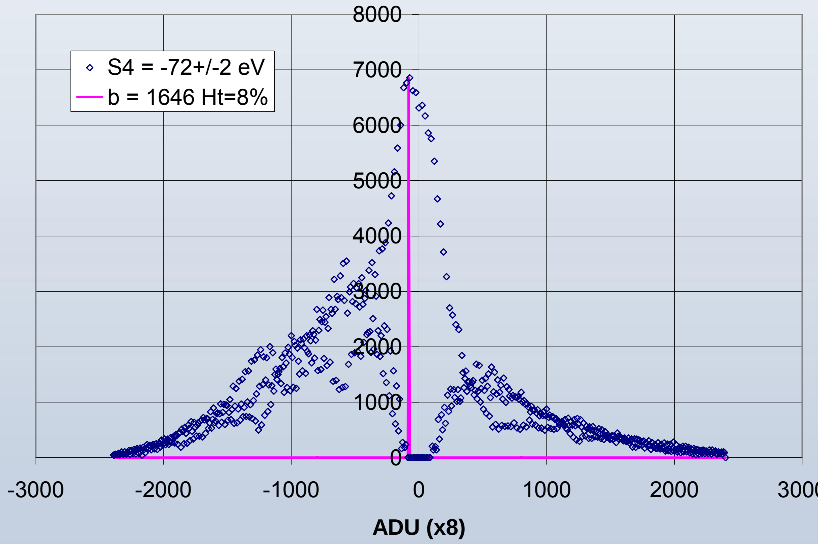
Fe



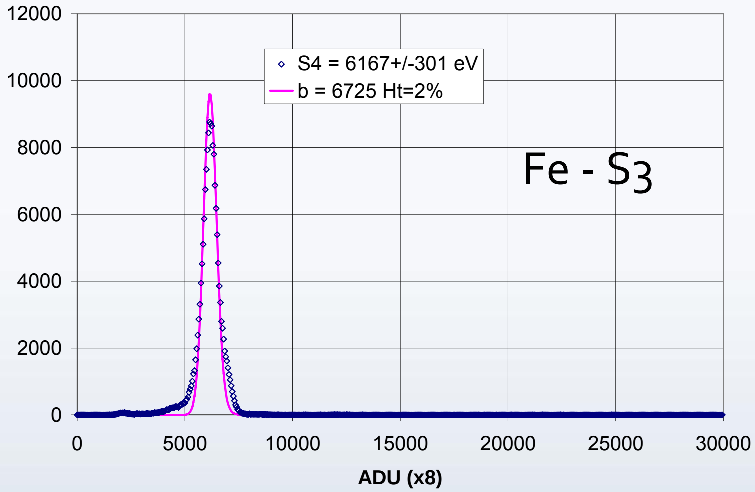
CCD y
(physical x,
CCD is at 90°)

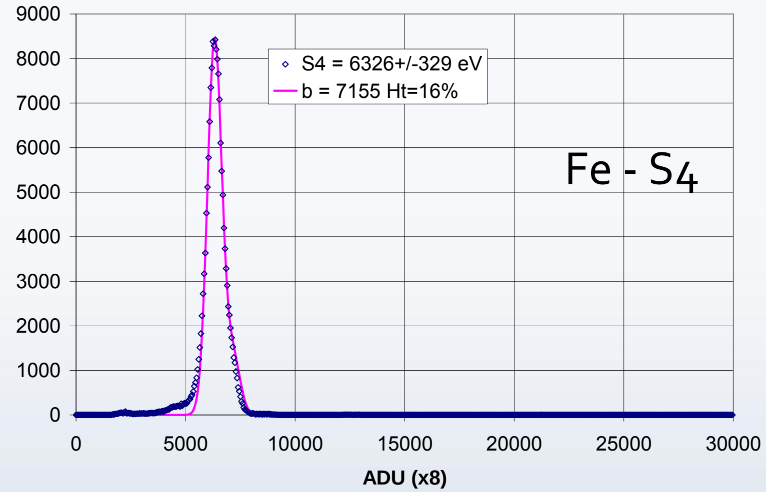


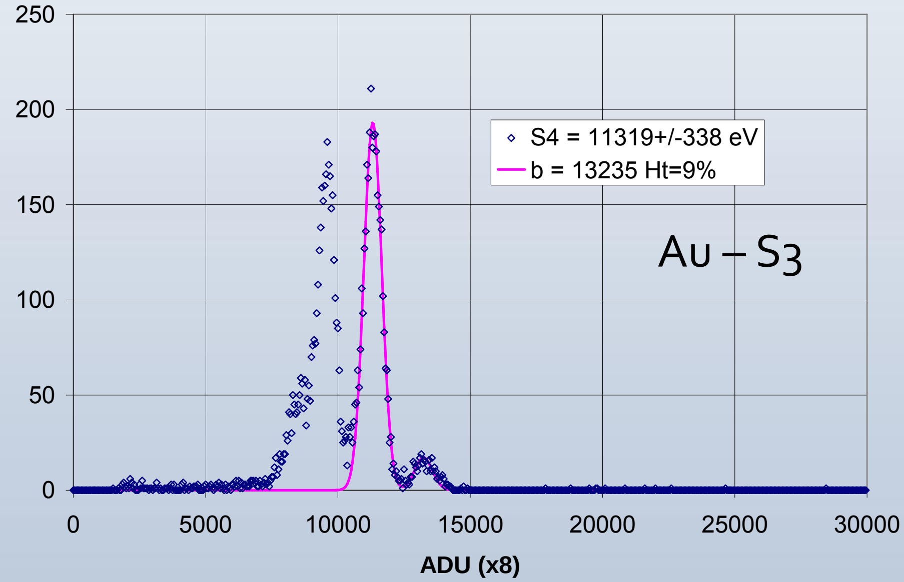




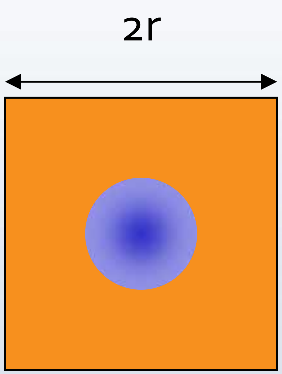
Restrict to COG peak ±1 σ

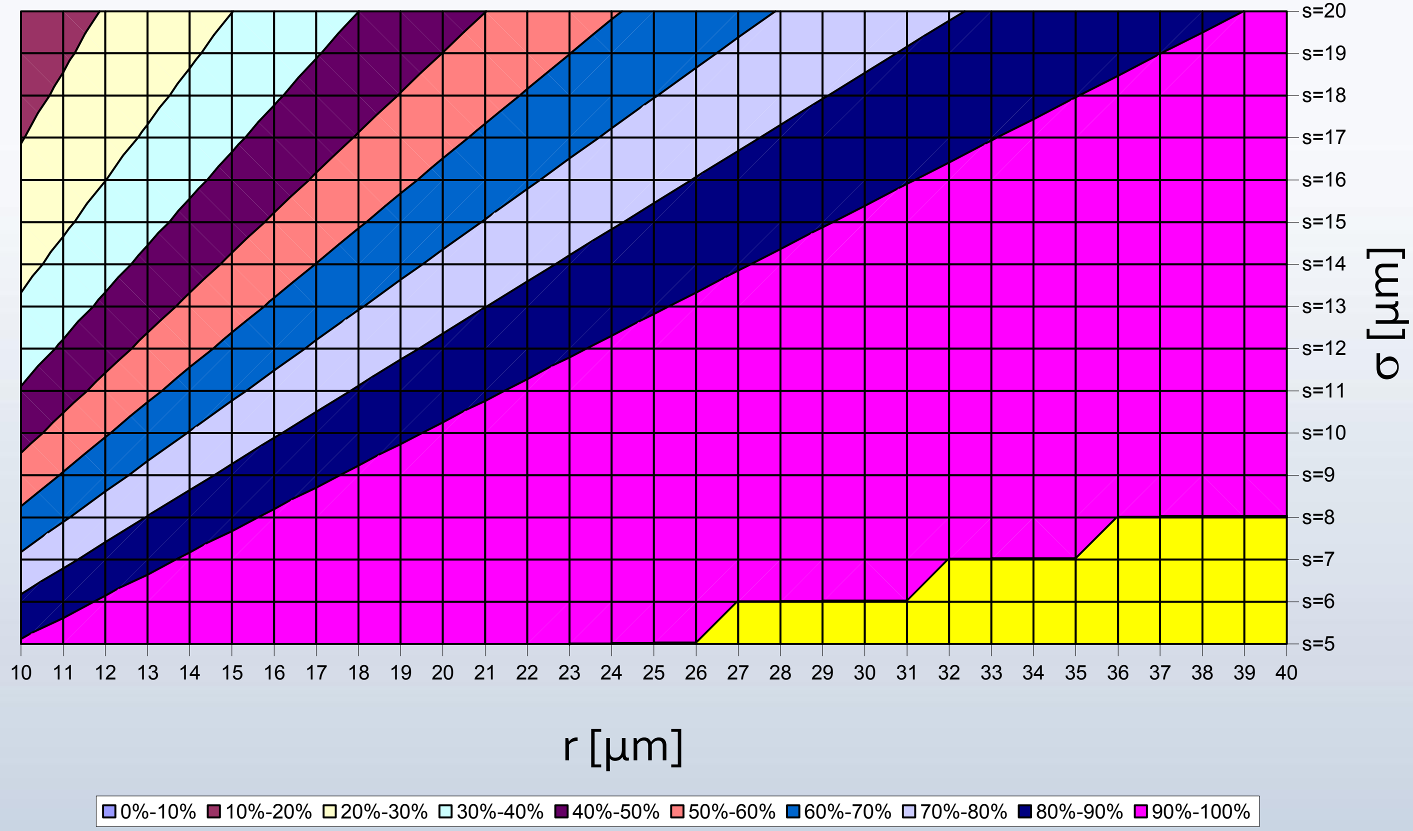






Reminder - containment



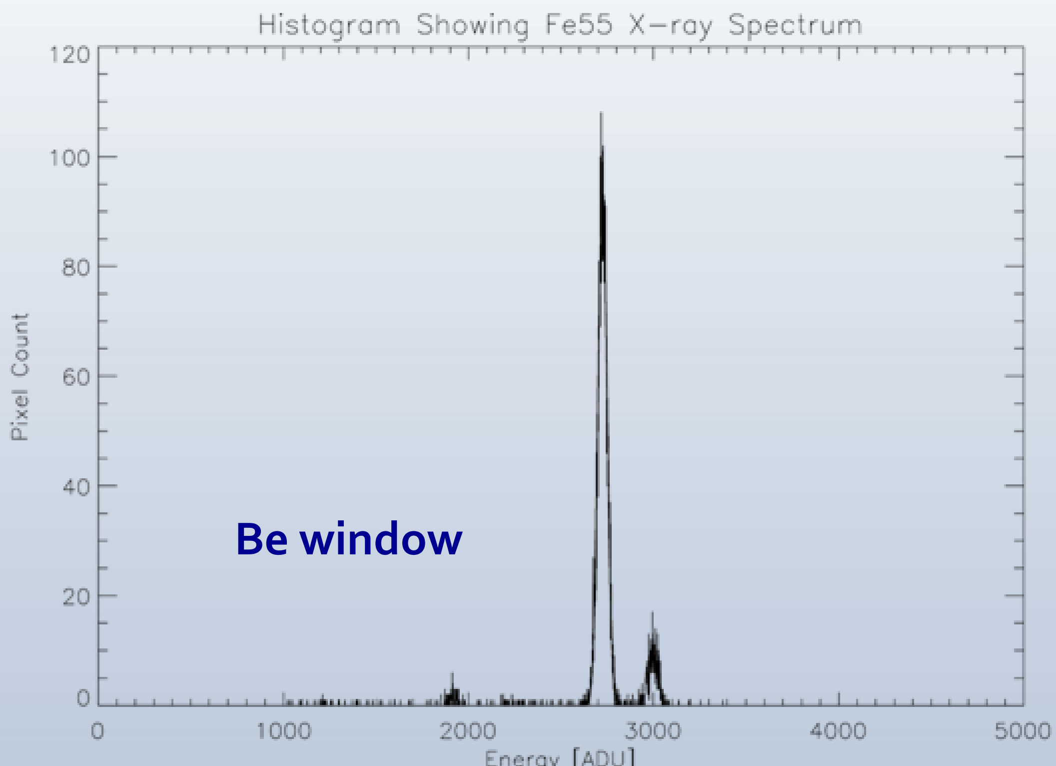


% of charge contained in a $(2r)^2$ square from a Gaussian blob of size σ

Measure (confirm) PSF!

650 μm thick CCD

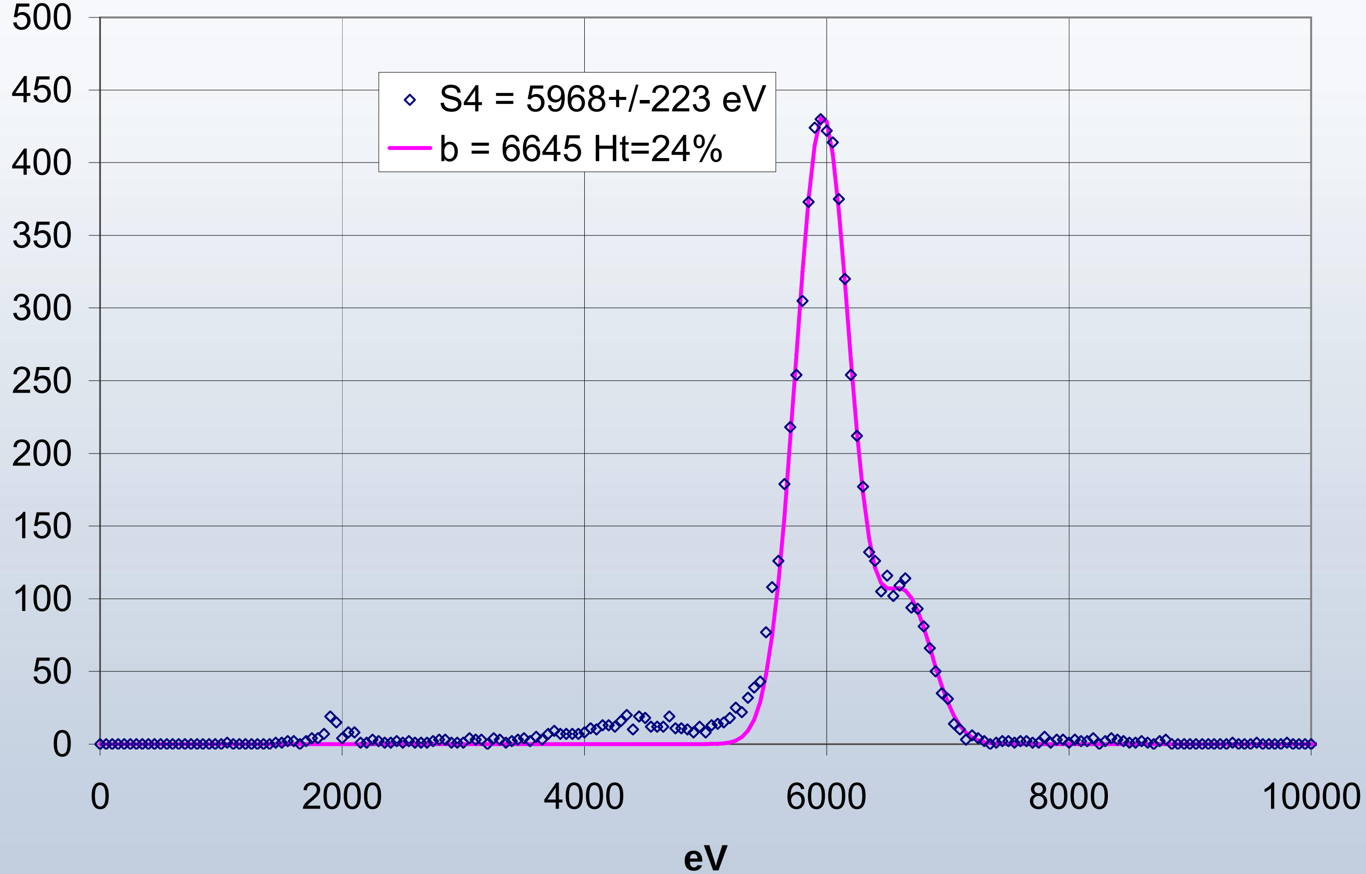
^{55}Fe K_α and K_β. Resolution ~ 126 eV at 5.6 keV



- SNAP
- 10 μm pixels
- Slow readout
- T = -140 C
- single-pixel hits

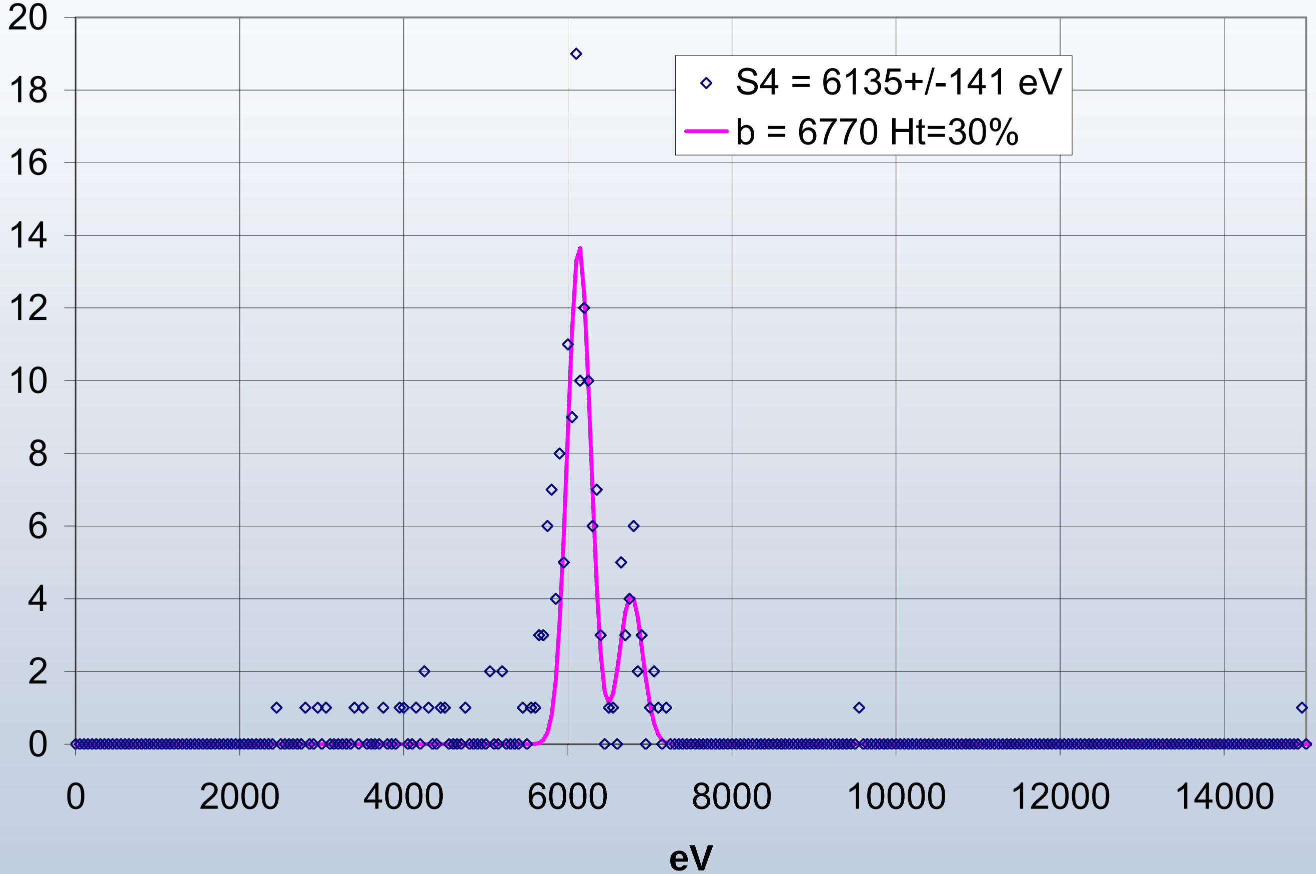
What if we do the same?

S_1 Fe COG +/- 500 eV S_1/S_4 >95%

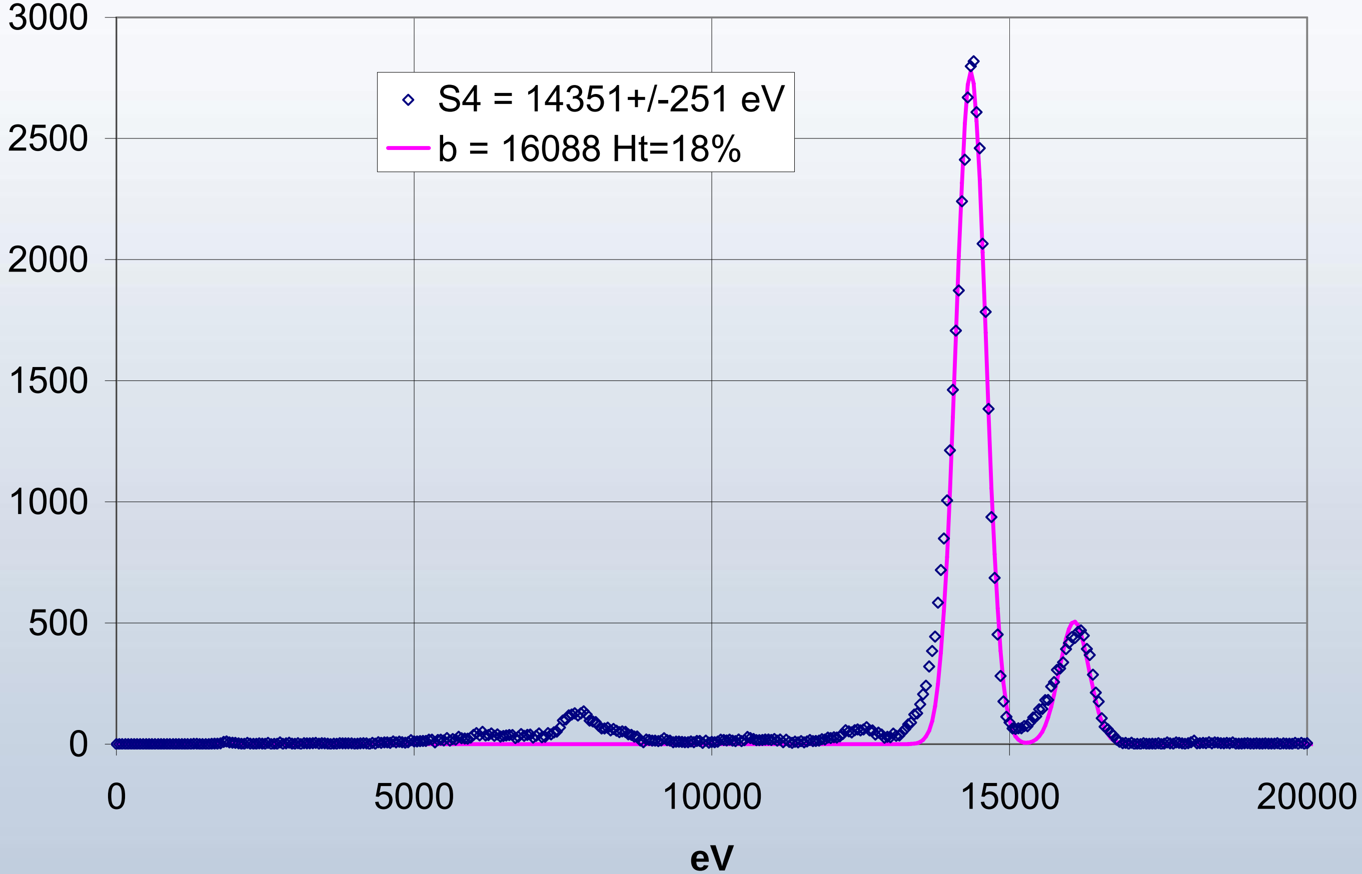


S_1 Fe COG +/- 500 eV S_1/S_4 >95%

One output (1st one)

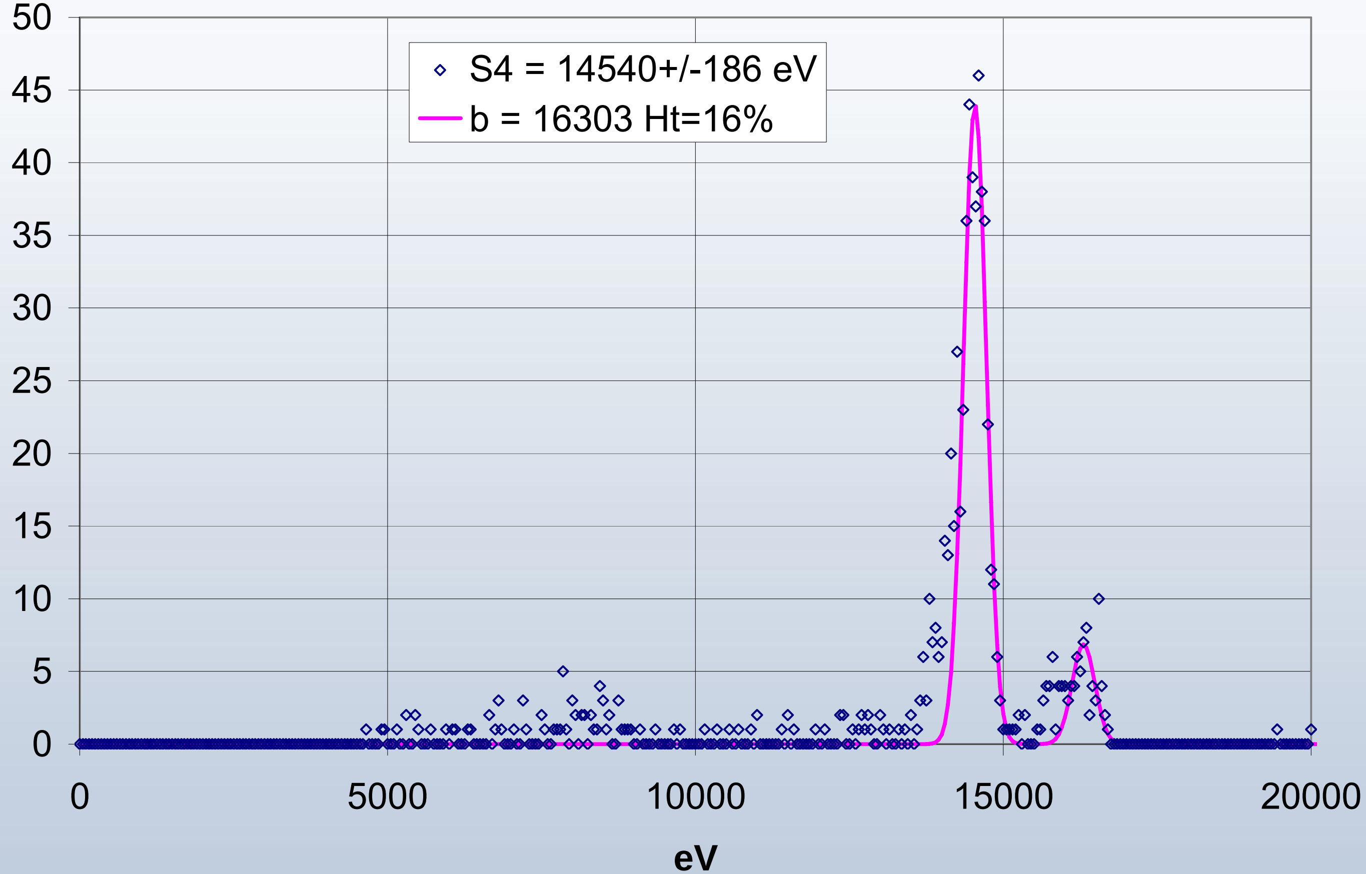


S_1 Y COG +/- 500 eV S_1/S_4 >95%

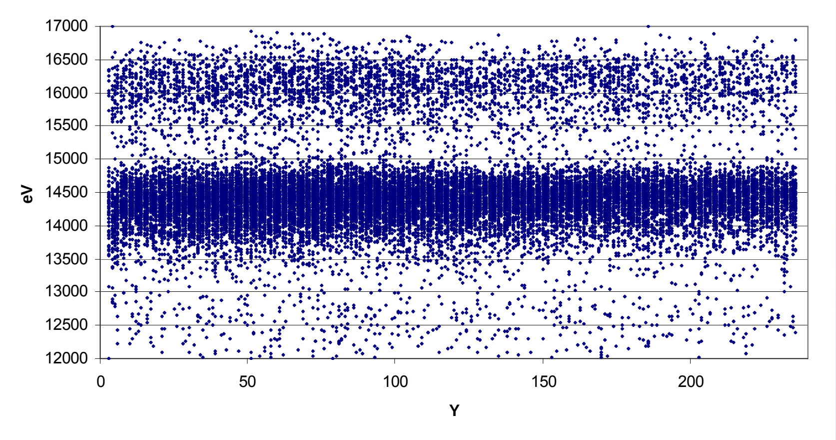


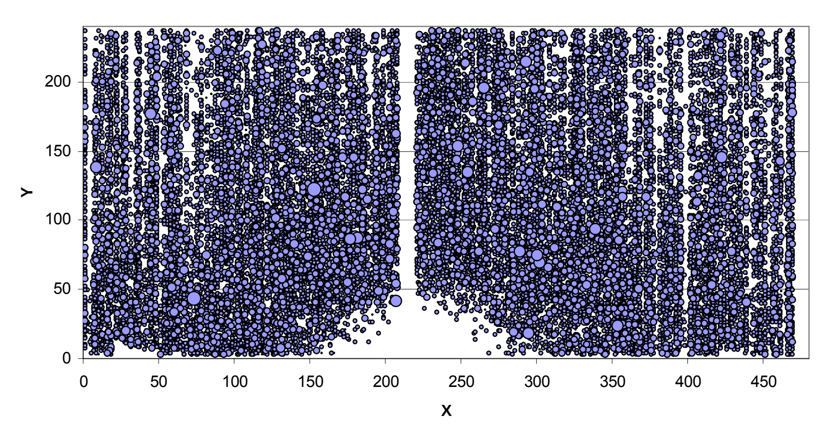
S_1 Y COG +/- 500 eV S_1/S_4 >95%

One output



Y

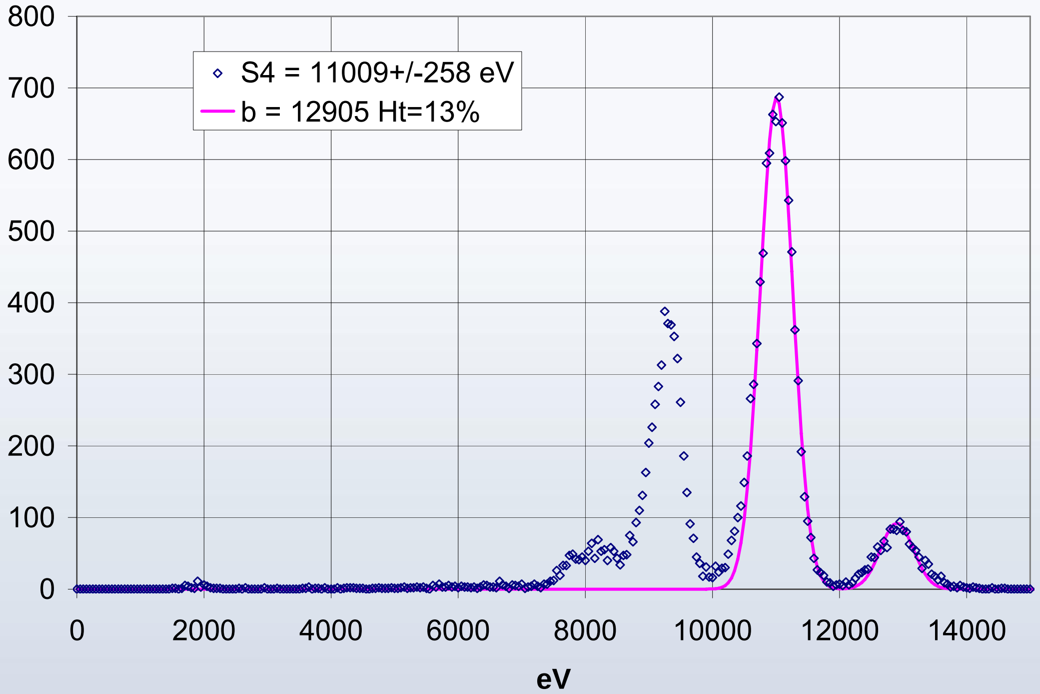


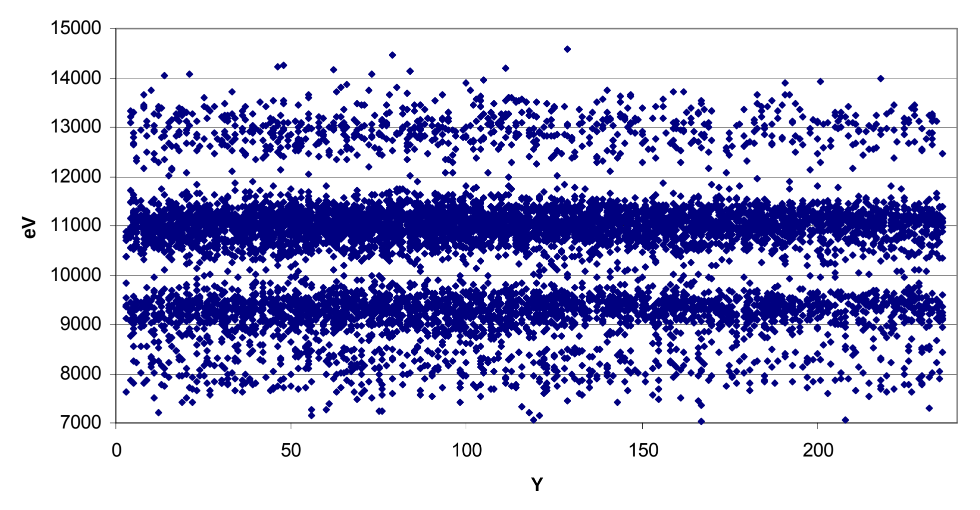


Pulse height vs. y
No y-dependence
(after corrections)

(x,y) distribution of hits

Au

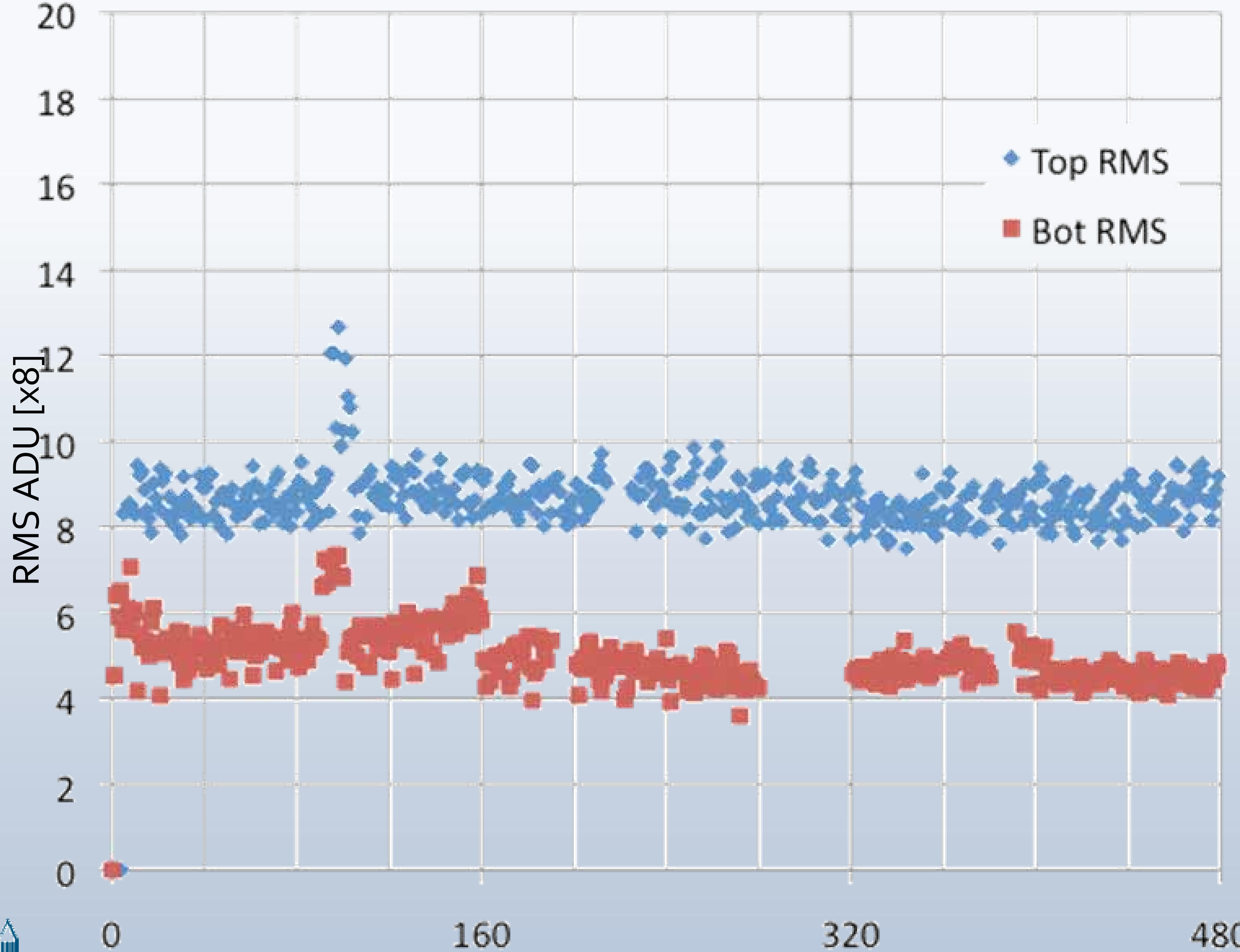




Single pixel spectra consistent
With noise + Fano-limited
resolution

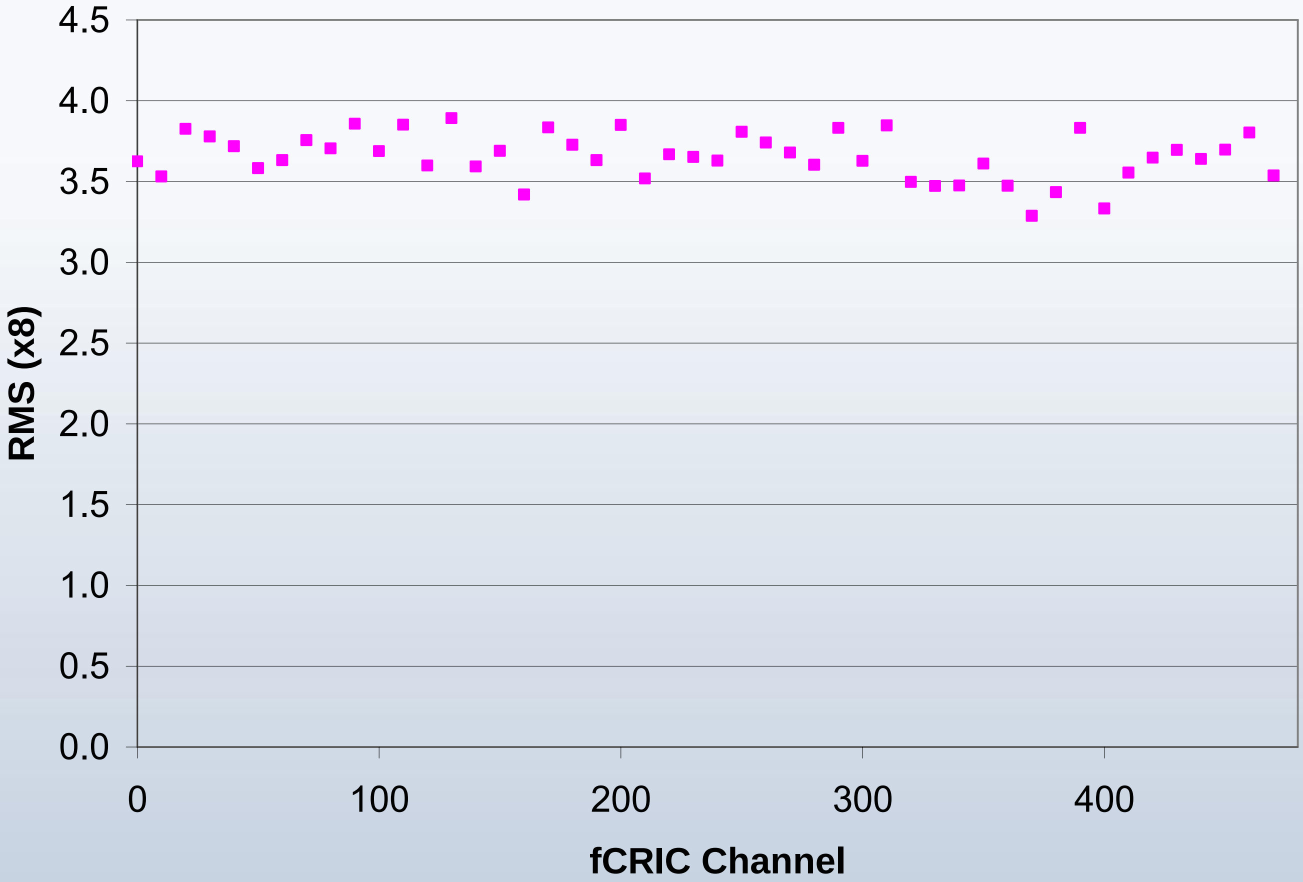
480 x 480 → APS Jan. '09

Noise with Readout v. 2



New substrate, New firmware, Forced x8

fCRIC clamped, x8

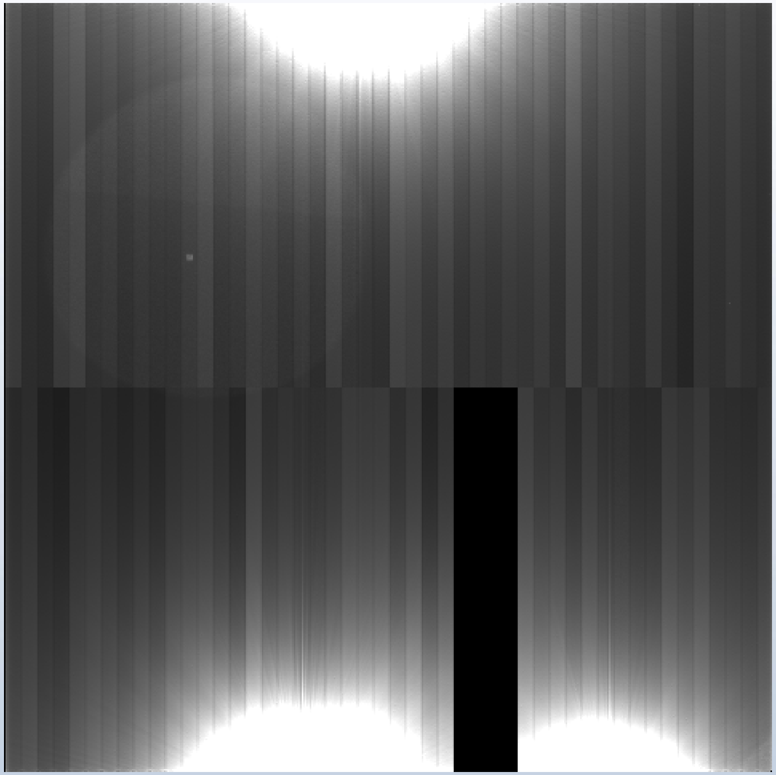


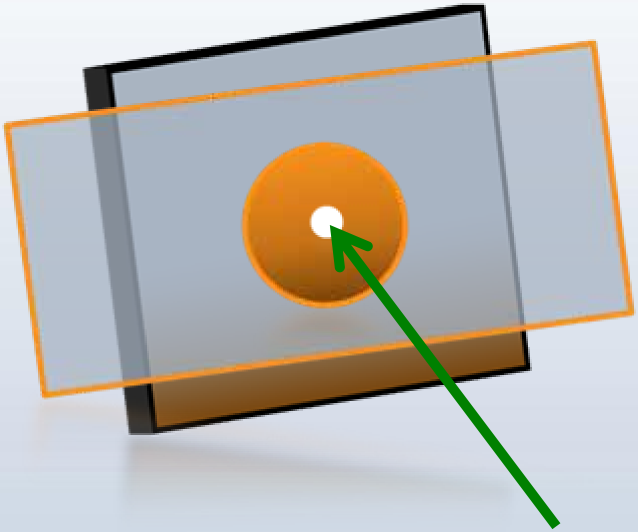
Measured before coming to ANL – noise contribution from fCRIC itself 3.5 – 4 ADU

Test with xray tube and pinhole

Yesterday

Goal – PSF vs. V_{SUB}





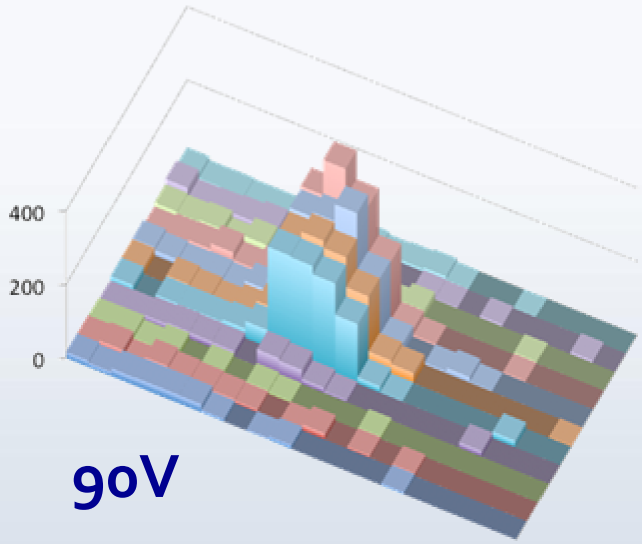
Pinhole in tungsten on a carrier

Warts and all

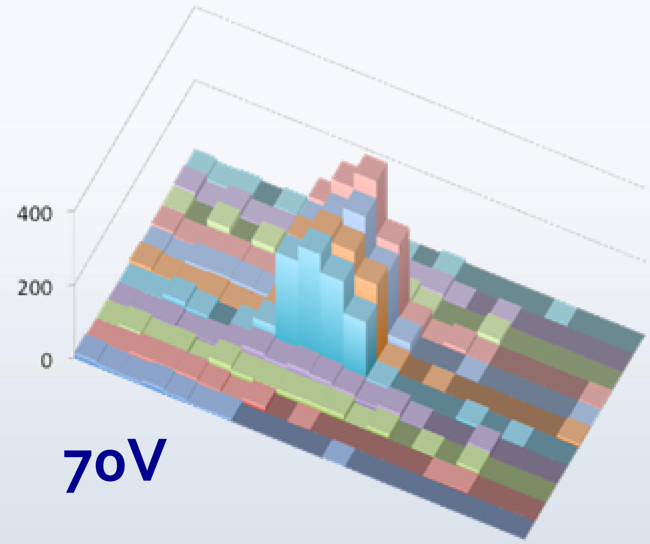
T_{INT} = 900 ms

Signal vs V_{SUB}

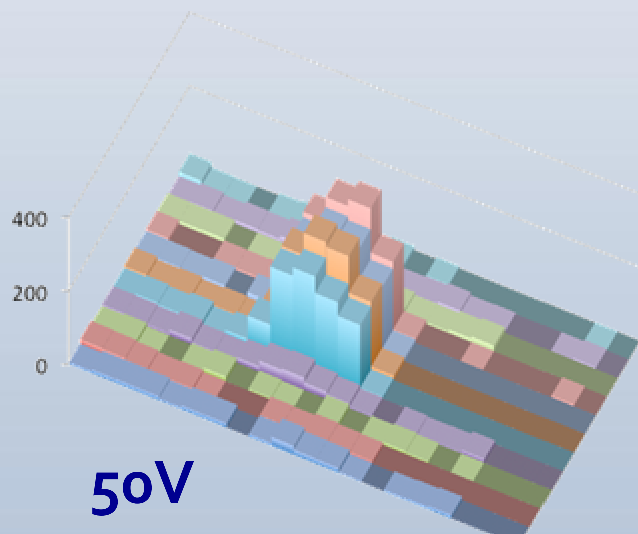
Yesterday
Preliminary!



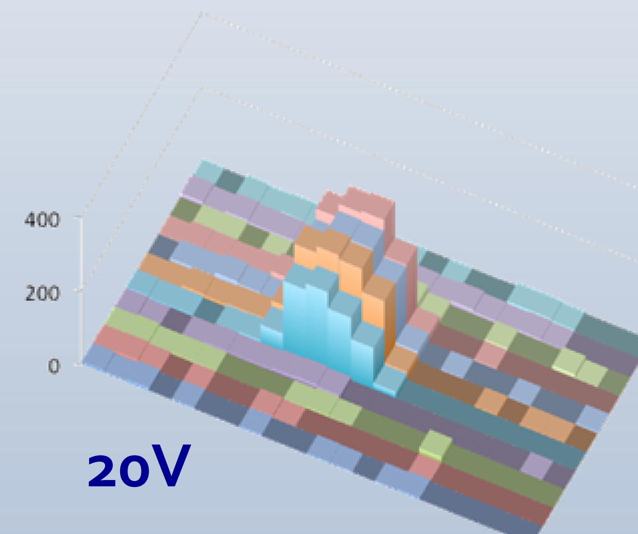
90V



70V



50V

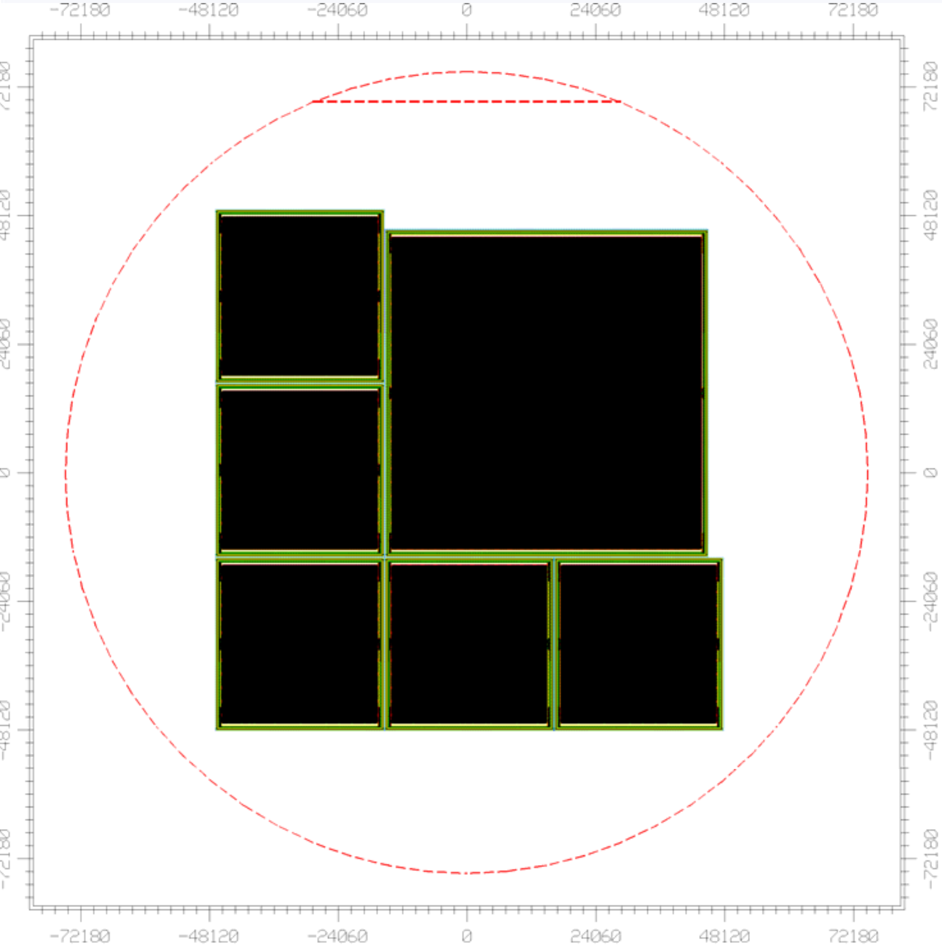


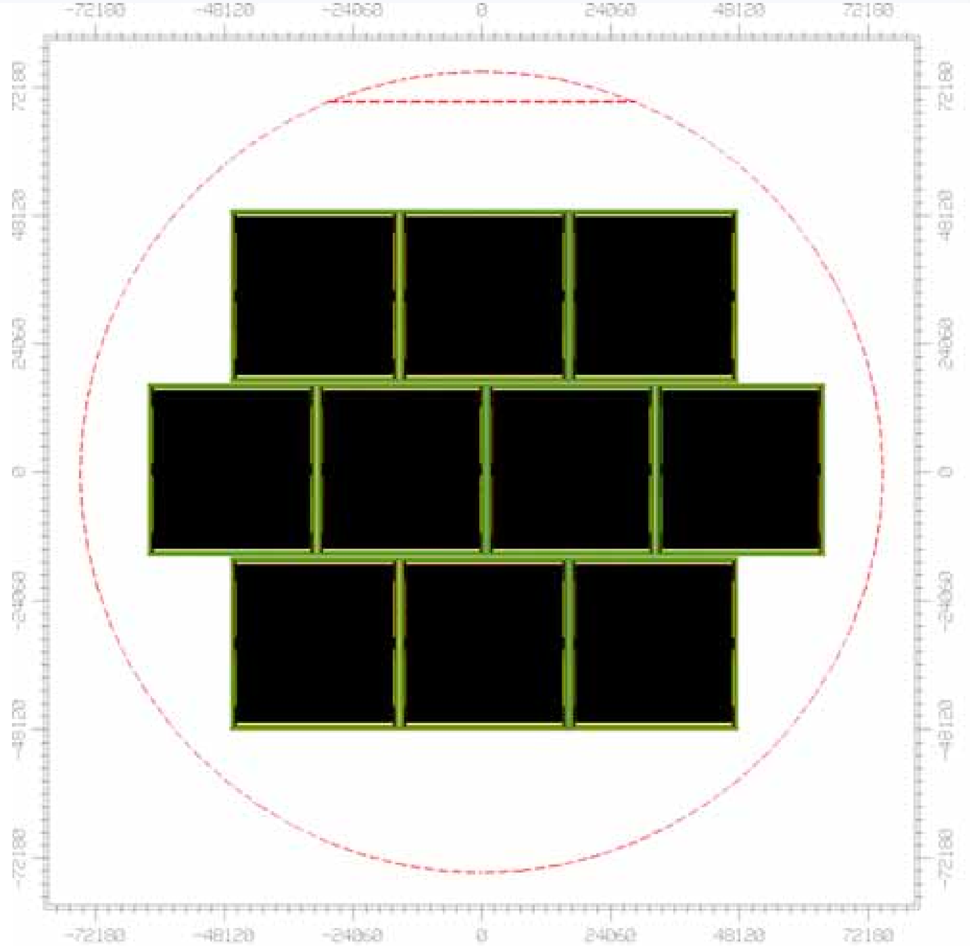
20V

Conclusions

- Pretty much there
  - A few minor fixes
  - Noise now OK on one half, fix on other half
- Plan to make some 1k devices on an LDRD run this FY (but …)
  - Easy to add small "specialized" CCDs
- Starting to think of compact packaging

In an ideal world ...





- Run a CCD lot (~20 wafers)
- Run an fCRIC lot (several thousand chips)
- Probe chips