SSD Ladder Card Traveler

Date: June 12th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
62						X	☑	☑	☐	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.75
2 V +	0.021
2 V -	0.036

	Plugged to "TestBoard"	Plugged to Ladder (start from 15) July 1st-13			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	~~5th Alice Broken~~ 3, 4, 5, 6 Noisy
1	☑	☑	X ☒	☑	~~Noisy 1st Alice Broken~~
2	☑	☑	X ☒	☑	1st Alice Broken
3	☑	X ☒	⊟ —	☑	6th Alice Broken
4	☑	X ☒	⊟ —	☑	2, 3, 4, 5, 6 Alice Broken
5	☑	☑	☑	☑	6th Alice Broken
6	☑	X ☒	⊟ —	☑	Very high spike end of 3rd Alice
7	☑	X ☒	⊟ —	☑	high spike end of 3rd Alice
8	☑	☑	☑	☑	high spike end of 3rd Alice
9	☑	☑	☑	☑	5, 6 Alice Broken
10	☑	☑	☑	☑	
11	☑	X ☒	⊟ —	☑	
12	☑	X ☒	⊟ —	X ☒	No ANALOG DATA
13	☑	☑	☑	☑	High Noisy when Biased
14	☑	☑	☑	☑	Noisy 1, 2, 6 Alice Broken
15	☑	☑	☑	☑	5th Alice Broken

⑪ Inspection		Initials
Passed ☐	Failed ☐	

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
1 (zero)	☑	☐

Comments:

SSD Ladder Card Traveler

Date: June 12th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
61					X		☑	☑	☐	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn] — ⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

	⑧ LC Current [A]
5 V	0.75
2 V +	0.021
2 V -	0.036

	Plugged to "TestBoard"	Plugged to Ladder (start from 15) July 1st			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	X ☒	⊟ —	☑	A 3, 4, 5 smaller peaks.
1	☑	☑	☑	☑	
2	☑	☑	☑	☑	
3	☑	☑	☑	☑	
4	☑	☑	X ☒	☑	
5	☑	☑	☑	☑	
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	stdev 1,1 Background 4 Alice Bad Noisy 1, 5, 6, 3
8	☑	☑	☑	☑	2 Alice Bad high spike end of 3rd 4th noisy
9	☑	X ☒	⊟ —	☑	high peak end of 3rd Alice
10	☑	☑	☑	☑	
11	☑	☑	X ☒	☑	
12	☑	X ☒	⊟ —	☑	6th Alice Bad
13	☑	☑	☑	☑	
14	☑	☑	X ☒	☑	
15	☑	☑	☑	☑	stdev 3 Background 2nd Alice Bad

⑪ Inspection		Initials
Passed ☐	Failed ☐	

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
1 (Zero)	☐	☑

Comments:

SSD Ladder Card Traveler

Date: July 8th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
40		X		X	X	X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn] — ⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.75
2 V +	0.019
2 V -	0.030

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	2, 3, 5, 6 Bad
1	☑	☑	☑	☑	~~1 Broken~~ 1, 3, 4 Bad
2	☑	☑	☑	☑	1 smaller
3	☑	☑	☑	☑	2, 3, 4 Bad
4	☑	☑	☑	☑	2, 4, 5 Bad
5	☑	☑	☑	☑	5 Bad 1, 2, 3, 6 smaller
6	☑	☑	☑	☑	1, 2 smaller
7	☑	☑	☑	☑	Analog Background 1, 2 smaller 2 Bad
8	☑	☑	☑	☑	5, 6 Smaller 5 Noisy
9	☑	☑	☑	☑	1 Broken 2, 6 Noisy
10	☑	☑	☑	☑	2 Bad 3 Smaller
11	☑	☑	X ☒	☑	5 Noisy
12	☑	☑	X ☒	☑	2, 3 smaller
13	☑	☑	X ☒	☑	3 bad & smaller
14	☑	☑	X ☒	☑	2 Noisy 1 smaller
15	☑	☑	☑	☑	5 Noisy

⑪ Inspection		Initials
Passed ☐	Failed ☐	

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
2	☑	☐

Comments:

55 V 30 μA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
58				X		X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	2, 3, 4, 5, 6 Bad
1	☑	☑	☑	☑	3, 6 Bad 2, 4, 5 smaller
2	☑	☑	☑	☑	3, 4, 5, 6 Bad
3	☑	☑	☑	☑	stdev 1 Background 6 Bad
4	☑	☑	☑	☑	6 Noisy
5	☑	☑	☑	☑	2 flat 4 smaller
6	☑	☑	☒	☑	1 noisy 4, 5, 6 Bad
7	☑	☑	☒	☑	stdev 1 Background 6 very small
8	☑	☑	☒	☑	2, 3, 6 smaller
9	☑	☑	☑	☑	1, 4 flat
10	☑	☑	☑	☑	1, 2, 3, 6 smaller
11	☑	☑	☒	☑	1 Broken 4, 6 smaller
12	☑	☑	☑	☑	1 Noisy 2, 3, 5 smaller
13	☑	☑	☑	☑	2, 6 smaller
14	☑	☑	☑	☑	1, 2 smaller
15	☑	☑	☑	☑	3, 6 smaller

⑪ Inspection		Initials
Passed ☐	Failed ☐	

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
2	☐	☑

Comments:

35 ✓ 39 μA

SSD Ladder Card Traveler

Date: July 8th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
41		X		X	X		☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.75
2 V +	0.019
2 V -	0.030

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	5 Bad 1, 4, 6 Noisy
1	☑	☑	☑	☑	1, 3 No spikes
2	☑	☑	☑	☑	1, 3 No spikes
3	☑	☑	☑	☑	3 Small 6 Noisy 5 Noisy 6 Bad
4	☑	☑	☑	☑	2, 3, 4 No spikes
5	☑	☑	☑	☑	3, 5 Flat 6 No spikes 8 Noisy
6	☑	☑	☑	☑	2 Smaller
7	☑	X ☒	⊟	☑	1, 4 Bad Flat
8	☑	☑	X ☒	☑	
9	☑	☑	X ☒	☑	9 No spikes
10	☑	☑	X ☑	☑	
11	☑	☑	X ☒	☑	1, 3, 6 Bad Noisy
12	☑	☑	X ☒	☑	
13	☑	☑	X ☒	☑	
14	☑	☑	X ☒	☑	3 Bad 4 Noisy
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.06
+2	0.869
-2	2.1

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
03	☑	☐

Comments:

50 ✓ 28 μA

SSD Ladder Card Traveler

Date: July 9th 2003

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
25	X			X	X		☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn] — ⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)				
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid		Comments
0	☑	☑	☑	☑		1, 2, 4, 6 No spikes
1	☑	☑	☑	☑		3, 5 Small spike
2	☑	☑	☑	☑		5 small
3	☑	☑	☑	☑		3, 5, 6 No spikes 4 Flat
4	☑	☑	☑	☑		4 small spikes
5	☑	☑	☑	☑		
6	☑	☑	☑	☑		
7	☑	☑	☑	☑		1, 2, 3, 6 Small
8	☑	☑	☒	☑		2 No spikes 6 No spikes.
9	☑	☑	☒	☑		
10	☑	☑	☒	☑		1, 3, 5, 6 Noisy 4 Bad
11	☑	☑	☒	☑		
12	☑	☑	☒	☑		4 Noisy
13	☑	☑	☒	☑		
14	☑	☑	☒	☑		3, 4, 5, 6 flat
15	☑	☑	☒	☑		5 No spikes

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.03
+2	0.875
-2	2.138

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
03	☐	☑

Comments:

50 V 44 μA

Short to carbon fiber screws removed and capton tape put power connector

SSD Ladder Card Traveler

Date: July 15th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
17	X		X	X	X		☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.835
2 V +	0.019
2 V -	0.035

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)				
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present		Analog Data from Hybrid	Comments
0	☑	☑	X	☒	☑	4, 5 No Peaks.
1	☑	☑	X	☒	☑	2 No Peaks 4 Noisy
2	☑	☑	X	☒	☑	
3	☑	☑	X	☒	☑	4 No Peaks
4	☑	☑	X	☒	☑	
5	☑	☑	X	☒	☑	
6	☑	☑	X	☒	☑	
7	☑	☑	X	☒	☑	4 No Peaks
8	☑	☑	☑		☑	
9	☑	☑	☑		☑	
10	☑	☑	☑		☑	
11	☑	☑	☑		☑	
12	☑	☑	☑		☑	3 Broken Noisy 1, 2, 5, 6 Noisy
13	☑	☑	☑		☑	
14	☑	☑	☑		☑	
15	☑	☑	☑		☑	5 Flat

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.035
+2	0.877
-2	2.148

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
04	☑	☐

Comments:

BIAS Leakage current 32 μA

SSD Ladder Card Traveler

Date: July 15th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
20	X		X		X	X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.84
2 V +	0.019
2 V -	0.039

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)				
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☒	☑	1, 6 No Peaks
1	☑	☑	☒	☑	1, 6 No Peaks
2	☑	☑	☑	☑	1, 3, 6 No Peaks
3	☑	☑	☒	☑	
4	☑	☑	☒	☑	
5	☑	☑	☒	☑	2 No Peaks
6	☑	☑	☒	☑	3 Very small
7	☑	☑	☒	☑	
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	3 Noisy
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	4 Noisy
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	6 No Peaks

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.052
+2	0.888
-2	2.157

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
24	☐	☑

Comments:

BIAS current 4 μA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
28	X				X	X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.079

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)				
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid		Comments
0	☑	☑	☑	☑		3, 6 No Peaks
1	☑	☑	☑	☑		2, 3, 5 No Peaks
2	☑	☑	☑	☑		4, 5 small
3	☑	☑	☑	☑		1 small
4	☑	☑	☑	☑		
5	☑	☑	☑	X	☑	All Noisy Broken 3 Flat
6	☑	☑	☑	X	☑	All Noisy Broken
7	☑	☑	☑		☑	6 Noisy
8	☑	☑	☑		☑	1 No Peaks
9	☑	☑	☑		☑	6 Noisy
10	☑	☑	☑		☑	3 Noisy
11	☑	☑	☑		☑	8 Noisy
12	☑	☑	☑		☑	
13	☑	☑	☑		☑	
14	☑	☑	☑	X	☑	6 Noisy 10th BIAS Broken, Crazy
15	☑	☑	☑		☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.036
+2	0.891
-2	2.178

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
05	☑	☐

Comments:

BIAS current 42 μA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
46		X				X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.5
2 V +	0.014
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	
1	☑	☑	☑	☑	3, 4, 6 No Peaks
2	☑	☑	☑	☑	5, 6 No Peaks
3	☑	☑	☑	☑	4 No Peaks
4	☑	☑	☑	☑	2 No Peaks
5	☑	☑	☑	☑	
6	☑	☑	☑	☑	3 No Peaks
7	☑	☑	☑	☑	5 Small
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

3	1.055
+2	0.9
-2	2.117

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
05	☐	☑

Comments:

Bias current 50 μA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
54			X			X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1 Noisy 2, 3 small
1	☑	☑	☑	☑	2, 4 small
2	☑	☑	☑	☑	1, 3, 5, 6 Small No Peaks
3	☑	☑	☑	☑	
4	☑	☑	☑	☑	1, 4, 6 Small
5	☑	☑	☑	☑	
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	1 Noisy
8	☑	☑	☑	☑	1 small
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	1 Noisy
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	1 Small
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	2 Flat 1,3,4,5,6 Noisy
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.047
+2	0.909
-2	2.189

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
Ø6	☑	☐

Comments:

46 V 92 MA

SSD Ladder Card Traveler

Date: July 15th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
19	X		X	X			☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.83
2 V +	0.019
2 V -	0.035

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1, 2, 3, 4, 5 No Peaks
1	☑	☑	☑	☑	1 No Peaks
2	☑	☑	☑	☑	1, 5 No Peaks
3	☑	☑	☑	☑	2 Small 6 No Peaks
4	☑	☑	☑	☑	5 No Peaks 6 Small
5	☑	☑	☑	☑	2 Small 3 No Peaks
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	
9	☑	☑	☑	X ☑	All Broken Noisy
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	X ☒	☒	X ☒	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	2, 5 Noisy

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5V	1.038
+2V	0.955
-2V	2.04

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
06	☐	☑

Comments:

46V 53 μA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
37		X	X		X		☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1, 5, 6 No peaks
1	☑	☑	☑	☑	1, 2 smaller
2	☑	☑	☑	☑	1 No peaks
3	☑	☑	☑	☑	2 No peaks 5, 6 Flat
4	☑	☑	☑	☑	1 smaller
5	☑	☑	☑	☑	1, 2 smaller
6	☑	☑	☑	☑	3 smaller
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	2 smaller
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	1, 3 Noisy 2 Noisy
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.04
+2	0.923
-2	2.22

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
08	☑	☐

Comments: Jackie reported she change 52 in the board, the wire wrapping gun destroyed the original one. (3 pin conn)

52V 67 μA

SSD Ladder Card Traveler

Date: July 7th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
34		X	X	X		X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.029

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	
1	☑	☑	☑	☑	1 No peaks
2	☑	☑	☑	☑	2, 3, 5 No peaks
3	☑	☑	☑	☑	1, 4 No peaks
4	☑	☑	☑	☑	4 No peaks
5	☑	☑	☑	☑	1 Noisy
6	☑	☑	☑	☑	6 No peaks
7	☑	☑	☑	☑	All Hybrids bad
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	2 Small peaks
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	~~☒~~	–	~~☒~~	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	3 Noisy

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.05
+2	0.88
-2	2.036 A

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
08	☐	☑

Comments:

52 V 73 μA → 66 μA

SSD Ladder Card Traveler

Date: July 8th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
60					X	X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn] — ⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.75
2 V +	0.019
2 V -	0.035

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	5 No peaks
1	☑	☑	☑	☑	2, 3 No peaks
2	☑	☑	☑	☑	All No peaks
3	☑	☑	☑	X ☑	All Broken Noisy
4	☑	☑	☑	☑	4 small peaks
5	☑	☑	☑	☑	4 Broken 1, 4, 5 Noisy
6	☑	☑	☑	☑	5, 6 small
7	☑	☑	☑	☑	2 No peaks
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	4 small peaks
14	☑	☑	☑	☑	2 No peaks
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5V	1.03
+2V	0.89
-2V	2.18

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
09	☑	☐

Comments:

50V 74 μA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
39		X	X				☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	3 Noisy
1	☑	☑	☑	☑	3 No peaks
2	☑	☑	☑	☑	1 No peaks
3	☑	☑	☑	☑	
4	☑	☑	☑	☑	6 small
5	☑	☑	☑	☑	3 Noisy
6	☑	☑	☑	☑	2 small
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	2 broken Rest small
10	☑	☑	☑	☑	6 flat
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	6 Noisy
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.05
+2	0.91
-2	2.18

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
09	☐	☑

Comments: Sackie reported flex with punctures

50V 73mA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
23	X		X				☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn] ⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	3,4 Bad
1	☑	X ☒	⊟	☑	5,6 Flat 3 very small
2	☑	☑	☑	X ☑	2,3,4,5,6 Flat All Noisy
3	☑	☑	☑	X ☑	All Bad Noisy
4	☑	☑	☑	☑	
5	☑	☑	☑	☑	1,2,6 Bad Noisy 6 Noisy
6	☑	☑	☑	☑	1,3 small 2 Noisy
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	6 Noisy
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	4th Noisy
11	☑	☑	☑	☑	stdev 1 Background
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	X ☑	Just Peristalic maybe STAG registers BAD
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

-5	1.02
+2	0.93
-2	2.2

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
10	☑	☐

Comments:

45 V 49 μA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
27	X			X			☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn] ⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	3, 5, 6 Bad
1	☑	☑	☑	☑	1, 3, 4 Bad 5 Small
2	☑	☑	☑	☑	1 Bad 1
3	☑	☑	☑	☑	1 Small 3 Noisy
4	☑	☑	☑	☑	
5	☑	☑	☑	☑	6 Terrible Bad 1, 5 Bad
6	☑	X ☒	☐	☑	5, 6 Small/ Noisy 6 Bad Flat
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	5 small
9	☑	☑	☑	☑	5 Flat
10	☑	☑	☑	☑	1, 6 Bad
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	3, 4 small
15	☑	☑	☑	☑	6 Alice flat

⑪ Inspection		Initials		
Passed ☐	Failed ☐		S	1.03
			+2	0.9
			-2	2.16

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
10	☐	☑

Comments:

45 V 48 μA

SSD Ladder Card Traveler

Date: July 16th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
18	X		X	X		X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8 A
2 V +	0.019
2 V -	0.035

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1, 2, 3 No peaks
1	☑	☑	☑	☑	4 Noisy
2	☑	☑	☑	☑	3, 4, 5 Small
3	☑	☑	☑	☑	
4	☑	☑	☑	☑	
5	☑	☑	☑	☑	5, 6 Small
6	☑	☑	☑	☑	4 No peaks
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	1 No peaks 6 Flat All Flat Noisy

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.077
+2	0.93
-2	2.24

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
11	☑	☐

Comments:

53 V 38 μA

SSD Ladder Card Traveler

Date: July 15th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
16	X		X	X	X	X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.77
2 V +	0.019
2 V -	0.035

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	6 No peaks
1	☑	☑	☑	X ☑	All Bad Noisy
2	☑	☑	☑	☑	5 No peaks
3	☑	☑	☑	☑	1 No peaks
4	☑	☑	☑	☑	1.6 No peaks
5	☑	☑	☑	☑	2.5 No peaks
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	4 No peaks
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	1.1 Odd Background
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	2.3 Flat
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.04
+2	0.9
-2	2.155

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
11	☐	☑

Comments:

5.3 V +2 [illegible]

SSD Ladder Card Traveler

Date: July 15th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
13	X	X			X		☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.872
2 V +	0.019
2 V -	0.035

	Plugged to "TestBoard"	Plugged to ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	X ~~☑~~	☐	X ~~☑~~	
1	☑	☑	☑	☑	1, 5 No peaks 3 Flat
2	☑	☑	☑	☑	2 No Peaks
3	☑	☑	☑	☑	3, 6 No Peaks
4	☑	☑	☑	☑	2, 3 No Peaks
5	☑	☑	☑	☑	
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	6 No Peaks
12	☑	☑	☑	☑	1, 2, 3, 6 Flat
13	☑	☑	☑	☑	1, 2, 5, 6 Flat
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.04
+2	0.855
-2	2.03

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
12	☑	☐

Comments:

SSD Ladder Card Traveler

Date: July 8th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
42		X		X		X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	X ☑	All bad 3 Flat, 6 Noisy
1	☑	☑	☑	☑	4 No Peaks 6 Flat Noisy
2	☑	☑	☑	☑	2, 6 No Peaks
3	☑	☑	☑	☑	4 No Peaks.
4	☑	☑	☑	☑	1, 2 No Peaks
5	☑	☑	☑	☑	2, 5 No Peaks 3 Flat
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	
9	☑	☑	☑	X ☑	All Broken Noisy
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	3, 6 No Peaks
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.036
+2	0.366
-2	2.099

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
12	☐	☑

Comments:

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
36		X	X		X	X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn] — ⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.029

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	5, 6 small
1	☑	☑	☑	☑	
2	☑	X ☒	~~☑~~	X ☒	
3	☑	☑	☑	☑	6 No peaks
4	☑	☑	☑	☑	6 No Peaks
5	☑	☑	☑	☑	
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	4, 6 small
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.04
+2	0.89
-2	2.1

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
13	☑	☐

Comments:

30 V 40 μA

SSD Ladder Card Traveler

Date: July 15th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
14	X	X				X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.884
2 V +	0.019
2 V -	0.035

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1 Small
1	☑	☑	☑	☑	
2	☑	☑	☑	☑	1, 2 No peaks
3	☑	☑	☑	☑	1, 3, 5, 6 Small
4	☑	☑	☑	☑	
5	☑	X ☒	⊟	☑	3, 5, 6 Flat
6	☑	☑	☑	☑	3, Noisy, Small
7	☑	☑	☑	☑	
8	☑	☑	☑	☐	
9	☑	☑	☑	☑	1 Noisy
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	1, 2, 3, 6 Broken Noisy
12	☑	X ☒	⊟	☑	
13	☑	☑	☑	☑	2 No peaks
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5 V	1.04
+2 V	0.899
-2 V	2.142

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
13	☐	☑

Comments:

5.0 V 48 μA

SSD Ladder Card Traveler

Date: July 8th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
32		X	X	X	X	X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	6 No peaks
1	☑	☑	X ☒	☑	5 No peaks
2	☑	☑	X ☒	☑	
3	☑	☑	X ☒	☑	1, No peaks Noisy
4	☑	☑	X ☒	☑	1 No peaks
5	☑	☑	X ☒	☑	2, 3, 4 No peaks 4 Noisy
6	☑	☑	☑	☑	5 Small - No peaks
7	☑	☑	☑	☑	5, 6 Small
8	☑	☑	☑	☑	4 Small
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	
11	☑	☑	X ☒	☑	
12	☑	X ☒	☐	☑	6 Flat 4, 5 Flat
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5V	1.048
+2V	0.894
-2V	2.2

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
14	☑	☐

Comments:

90V 98 mA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
31	X						☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.029

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	X ☒	☑	6 No peaks
1	☑	☑	X ☒	☑	
2	☑	☑	☑	☑	6 No peaks
3	☑	☑	X ☒	☑	1, 3, 4, 6 Flat
4	☑	☑	☑	☑	2 No peaks
5	☑	☑	☑	☑	4 Noisy
6	☑	☑	☑	☑	3 No peaks
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	
9	☑	☑	X ☒	☑	
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	1, 6 Noisy
15	☑	☑	X ☒	☑	2, 3 No peaks 4 Noisy

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.025
+2	0.89
-2	2.15

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
14	☐	☑

Comments:

90 V 101 mA

SSD Ladder Card Traveler

Date: July 8th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
44		X			X	X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	2, 3, 4, 5 Smaller Noisy
1	☑	☑	☑	☑	1, 2, 6 Smaller
2	☑	☑	☑	☑	4, 6 Bad
3	☑	☑	☑	☑	4, 5, 6 Bad Flat
4	☑	☑	☑	☑	5 Bad 1, 2, 3 Smaller
5	☑	☑	☑	☑	5, 6 Smaller
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	4 Bad
8	☑	☑	☑	☑	2 Noisy
9	☑	☑	☑	☑	3 Bad 4, 5 Noisy
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.04
+2	0.91
-2	2.18

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
15	☑	☐

Comments:

~~45 V~~ 40 V

~~40 μA~~ 28 μA

SSD Ladder Card Traveler

Date: July 8th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
55			X				☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0,75
2 V +	0,019
2 V -	0,035

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1,2,3,4,5 smaller
1	☑	☑	☑	☑	1,2,6 smaller
2	☑	☑	☑	☑	1,5,6 smaller
3	☑	☑	☑	☑	6 flat smaller
4	☑	☑	☑	☑	4 smaller
5	☑	☑	☑	☑	5,6 Bad
6	☑	☑	☑	☑	2,4,5 smaller
7	☑	☑	☑	☑	5,6 Smaller 4 Noisy
8	☑	☒	—	☑	1 Bad 4 Noisy
9	☑	☑	☑	☑	5 Noisy
10	☑	☑	☑	☑	3 Noisy
11	☑	☑	☑	☑	6 Bad
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	3 4 Bad 5 Noisy
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	6 smaller

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5V	1.034
+2 +V	0,986
-2V	2,246

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
15	☐	☑

Comments:

40V 12 μA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
33		X	X	X	X		☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0,019
2 V -	0,03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	X ☒	⊟	☑	6 Flat
1	☑	☑	☑	☑	2 small
2	☑	☑	☑	☑	5, 6 small
3	☑	☑	☑	☑	
4	☑	☑	☑	☑	4 No Peaks
5	☑	☑	☑	☑	2, 3, 4, 5, 6 Flat
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	4 Small
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	1 No peaks
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	stdev 1 Background

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.043
+2	0.91
-2	2.19

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
16	☑	☐

Comments: First Peristaltic pattern was very noisy
Second looks good
45 V 36 μA 45 μA after 6 min

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
53			X		X		☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	
1	☑	☑	☑	☑	4, 6 small peaks
2	☑	☑	☑	☑	
3	☑	☑	☑	☑	
4	☑	☑	☑	☑	
5	☑	☑	☑	☑	4 small
6	☑	☑	X ☒	☑	
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	3, 6 No peaks
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	3 small
13	☑	☑	☑	☑	stays 1 Background
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.05
+2	0.91
-2	2.17

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
16	☐	☑

Comments:

45 V 57 μA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
24	X			X	X	X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	2, 3, 4, 6 No peaks
1	☑	☑	☑	☑	1, 2, 6 No Peaks
2	☑	☑	☑	☑	1 Small
3	☑	☑	☑	☑	5 Broken Noisy
4	☑	☑	☑	☑	5 Small
5	☑	☑	☑	☑	
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	1, 3 Small
8	☑	☑	☑	☑	
9	☑	☑	☒	☑	
10	☑	☑	☒	☑	
11	☑	☒	⊟	☑	
12	☑	☑	☒	☑	1, 2, 3, 6 Noisy Broken
13	☑	☑	☒	☑	3 Noisy
14	☑	☑	☒	☑	1, 2, 3, 4 Broken Noisy
15	☑	☑	☒	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.037
+2	0.882
-2	2.15

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
17	☑	☐

Comments:

HV turns back off Max current, we are unplugging hybrids to see if we get rid of the short

the short is in the N side the screws are conecting to the Fiber structure and the P side ground as well 2300 Ω

After removing the screws Bias current 45 μA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
57				X	X		☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.030

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1, 3, 5, 6 Small
1	☑	☑	☑	☑	4, 5, 6 No Peaks
2	☑	☑	☑	☑	1 No peaks
3	☑	☑	☑	☑	2 No Peaks 5 Flat
4	☑	☑	X ☒	X ☑	All Broken Noisy
5	☑	☑	☑	☑	1, No Peaks
6	☑	☑	☑	☑	1, 4 No peaks
7	☑	☑	☑	☑	4 No Peaks 5 Noisy
8	☑	☑	☑	☑	
9	☑	☑	X ☒	☑	
10	☑	☑	X ☒	☑	
11	☑	☑	X ☒	☑	
12	☑	☑	X ☒	☑	1, 3, 6 Flat
13	☑	☑	X ☒	☑	3 Flat, rest Noisy Broken
14	☑	☑	X ☒	☑	
15	☑	☑	X ☒	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.042
~~12~~	0.866
-2	2.11

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
17	☐	☑

Comments:

After removing the screws Bias current stuck

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
21	X		X		X		☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn] — ⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1, 4 No Peaks, 3 Noisy
1	☑	☑	☑	☑	2, 3 Noisy
2	☑	☑	☑	☑	3 No Peaks, 4 Noisy
3	☑	☑	☑	☑	
4	☑	☑	☑	☑	4 No Peaks
5	☑	☑	☑	☑	1, 3, 5 No Peaks
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	2 No Peaks, 6 Noisy
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	2 Small
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	6 No Peaks
15	☑	☑	☑	☑	

⑪ Inspection		Initials			⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
Passed ☐	Failed ☐		5	1.038	18	☑	☐
			+2	0.884			
			-2	2.109			

Comments:

Bias current 51 μA

SSD Ladder Card Traveler

Date: July 8th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
51			X	X			☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0,8
2 V +	0,019
2 V -	0,029

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1, 2, 3, 5, 6 No Peaks
1	☑	☑	☑	☑	1, 2, 5, 6 No Peaks
2	☑	☑	☑	☑	1, 6 No Peaks
3	☑	☑	☑	☑	
4	☑	☑	☑	☑	
5	☑	☑	☑	☑	3, 5, 6 No Peaks
6	☑	☑	☑	☑	2, 5 No peaks
7	☑	☑	☑	☑	1 No Peaks
8	☑	☑	☑	☑	2, 3 No Peaks
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	5 Flat
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	1 Flat
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.044
+2	0.877
-2	2.09

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
18	☐	☑

Comments:

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
56				X	X	X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1 Broken
1	☑	☑	☑	☑	1, 3 Broken
2	☑	☑	☑	☑	1, 3, 6 Broken
3	☑	☑	☑	☑	
4	☑	X ☒	~~☐~~	X ☒	
5	☑	☑	☑	☑	
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	4 Bad
9	☑	☑	☑	☑	4 Noisy
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	3, 4, 6 Noisy
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	4 Noisy
14	☑	☑	☑	☑	5 All are Broken
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.056
+2	0.846
-2	2.0

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
20	☑	☐

Comments:

65V 60mA → After removing 119N

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
47	P8	P3	P4	P5	P6	P7	☑	☑	☑	☑	☑
		X									

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1, 3, 5 Bad
1	☑	☑	☑	☑	2 Bad
2	☑	☑	☑	☑	1, 2, 4 Bad
3	☑	☑	☑	☑	
4	☑	☑	☑	☑	
5	☑	☑	☑	☑	
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	1, 3, 4 Bad
8	☑	☑	☑	☑	
9	☑	☑ ☒	☑ ⊟	☑ ☒	5 Noisy [Disconnected]
10	☑	☑	☑	☑	2nd Bad
11	☑	☑	X ☒	☑	Noisy
12	☑	☑	☑	X ☑	Broke After integrated test
13	☑	☑	☑	☐	3 Also Bad
14	☑	X ☒	⊟	X ☒	
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.05
+2	0.82
-2	1.97

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
20	☐	☑

Comments:

HIZ No data when debugging short to carbon fiber

Hybrid 9 Causing the short of N side to carbon fiber → Hybrid 9 disconected

65 V 46 μA

SSD Ladder Card Traveler

Date: July 8th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
50			X	X		X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0,8
2 V +	0,019
2 V -	0,03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1 No peaks
1	☑	☑	☑	☑	1, 6 No peaks
2	☑	☑	☑	☑	1, 5 No peaks
3	☑	☑	☒	☑	3 Broken 4 No peaks
4	☑	☑	☑	☑	5 Small
5	☑	☑	☑	☑	1, 6 No peaks
6	☑	☑	☑	☑	2 No peaks
7	☑	☑	☑	☑	6 Small
8	☑	☑	☑	☑	3, 6 Noisy
9	☑	☑	☒	☑	3, 4 Flat
10	☑	☑	☒	☑	1, 2, 3 Broken Noisy 5, 6 Flat
11	☑	☑	☒	☑	
12	☑	☑	☒	☑	6 Noisy
13	☑	☑	☒	☒	
14	☑	☑	☒	☑	All Broken Noisy
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.048
+2	0.856
-2	2.09

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
22	☑	☐

Comments:

53 V 34 μA

SSD Ladder Card Traveler

Date: July 8th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
43		X		X			☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.029

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☐	1,2 Noisy 3 No peaks 4,6 Flat
1	☑	☑	☑	☑	1, 4, 5 No peaks
2	☑	☑	☑	☑	2, 3, 6 Small 5 No peaks
3	☑	☑	☑	☑	6 No peaks 4 Small
4	☑	☑	☑	☑	4 Small
5	☑	☑	☑	☑	
6	☑	☑	☑	☑	1, 4 Small
7	☑	☑	☒	☑	3 No peaks
8	☑	☑	☒	☑	6 Noisy
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	5 Small
11	☑	☑	☑	☑	3 Noisy
12	☑	☑	☑	☑	
13	☑	☑	☒	☑	
14	☑	☒	—	☑	3, 4, 5, 6 Flat
15	☑	☑	☒	☑	1, 2, 3 Noisy

5	1.044
+2	0.87
-2	2.089

⑪ Inspection		Initials
Passed ☐	Failed ☐	

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
22	☐	☑

Comments:

53 V 41 μA

SSD Ladder Card Traveler

Date: July 8th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
30	X					X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	X ☑	All Bad Noisy
1	☑	☑	X ☒	☑	
2	☑	☑	☑	☑	4 small
3	☑	☑	☑	☑	5 Flat 2 small
4	☑	☑	☑	☑	4, 5 Flat
5	☑	☑	X ☒	☑	1, 2, 6 Bad Noisy 4 Flat
6	☑	☑	☑	☑	
7	☑	☑	X ☒	☑	1 flat
8	☑	☑	☑	☑	
9	☑	☑	X ☒	☑	5 Noisy
10	☑	☑	X ☒	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	X ☒	☑	3, 5, 6 Noisy
15	☑	☑	☑	☑	3 No peaks

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.03
+2	0.88
-2	2.15

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
23	☑	☐

Comments: The Pigtail was missing and stephane put a new one.
45 V 26 μA then 35 μA After 8 min

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
38		X	X			X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	3, 4, 5 Very small
1	☑	☑	☑	☑	3, 5 No peaks Rest very small
2	☑	☑	☑	☑	
3	☑	☑	☑	☑	1, 4, 5 No peaks
4	☑	☑	☑	☑	2, 5 No peaks
5	☑	☑	☑	☑	2, 3 No peaks
6	☑	☑	☑	☑	4 No peaks
7	☑	☑	☑	☑	1, 6 No peaks
8	☑	☑	☑	☑	4 small
9	☑	☑	X ☒	☑	
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	3 smaller
12	☑	☑	X ☒	☑	
13	☑	☑	X ☒	☑	
14	☑	☑	☑	☑	
15	☑	☑	X ☒	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5	1.05
+2	0.896
-2	2.164

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
23	☐	☑

Comments: Stoped taking readings after strip # 670 (Could be soplet?)
45 V 50 μA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
52			X		X	X	☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn] — ⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.029

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	1 No Peaks
1	☑	☑	☑	☑	1.5 No Peaks
2	☑	☑	☑	☑	1 No Peaks
3	☑	☑	☑	☑	1,2 No Peaks
4	☑	☑	☑	☑	3 No Peaks
5	☑	☑	☑	☑	1,2,5 small
6	☑	☑	☑	☑	1,4 small
7	☑	☑	☑	☑	std 1.2 Background
8	☑	☑	☑	☑	1,2 small
9	☑	☑	☑	☑	4 Flat 1,6 small
10	☑	☒	☐	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	2 Alice No Peak
13	☑	☒	☐	☑	
14	☑	☑	☑	☑	2,3,4,5,6 Flat
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5V	1.04
+2V	0.896
-2V	2.169

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
24	☑	☐

Comments:

SSD Ladder Card Traveler

Date: July 16th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
15	X	X					☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.828
2 V +	0.019
2 V -	0.035

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☒	☑	☑	0 No Peaks 5,6 Flat
1	☑	☑	☑	☑	5, 6 No Peaks
2	☑	☑	☑	☑	1, 2, 6 small
3	☑	☑	☑	☑	1, 6 small
4	☑	☑	☑	☑	1 No Peaks
5	☑	☑	☑	☑	
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	6 Flat
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	1, 2 sdev Background
15	☑	☑	☑	☑	

⑪ Inspection		Initials			⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
Passed ☐	Failed ☐		5	1.05	24	☐	☑
			+2	0.91			
			-2	2.192			

Comments:

BIAS current 95 μA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
45		X			X		☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.03

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	Noisy Alice 1,2,3,4,5 Broken 6
1	☑	☑	☑	☑	1st Alice Broken
2	☑	☑	☑	☑	1,2 Alice Broken Noisy
3	☑	☑	☑	☑	3, 6 Alice Broken
4	☑	☑	☑	☑	
5	☑	☑	☑	☑	2,3,4 Noisy
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	
9	☑	☑	☑	☑	
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	1 Noisy
13	☑	☑	☑	☑	3, 5 Noisy
14	☑	☑	☑	☑	3, 5 Alice Noisy
15	☑	☑	☑	☑	5 Alice Broken

⑪ Inspection		Initials
Passed ☐	Failed ☐	

5V	1.036
+2V	0.912
-2V	2.191

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
25	☑	☐

Comments:

45V 49 mA

SSD Ladder Card Traveler

Date: July 9th 2013

① LC#	② Put an X when solder joint present						③ Check if 1 and 2 match	④ Switch with **XTAL_disable** and **USB_debug** slided right	⑤ Wire wrap to power fiber over 3.3V	⑥ Sniped pins in **fiber cage** and **high voltage connector**	⑦ Grinded PCB to fit carbon fiber structure
	P8	P3	P4	P5	P6	P7					
59				X			☑	☑	☑	☑	☑

Run Script ./LCv5Test.sh 1 LC# [starting conn]

⑨ Are internal registers matching ☑

Run Script ./LCv5FullTest.sh LC# [#Readings] [ASK] [starting conn]

⑩ Connect "TestBoard" and fill up table once checked each column

⑧ LC Current [A]	
5 V	0.8
2 V +	0.019
2 V -	0.029

	Plugged to "TestBoard"	Plugged to Ladder (start from 15)			
Connector #	POWER +2, -2, RESET, TCK, TMS, TDI, TDO, TEST, HOLD, DCLK, TOKENIN, ANALOG	JTAG communication present	COSTAR chip present	Analog Data from Hybrid	Comments
0	☑	☑	☑	☑	3, 5 Alice Broken
1	☑	☑	☑	☑	6 Alice Broken
2	☑	☑	☑	☑	1, 2 Alice Broken
3	☑	☑	☑	☑	3 Alice Broken
4	☑	☑	☑	☑	
5	☑	☑	☑	☑	
6	☑	☑	☑	☑	
7	☑	☑	☑	☑	
8	☑	☑	☑	☑	6 Alice Broken
9	☑	☑	☑	☑	1 Alice Noisy
10	☑	☑	☑	☑	
11	☑	☑	☑	☑	
12	☑	☑	☑	☑	
13	☑	☑	☑	☑	
14	☑	☑	☑	☑	
15	☑	☑	☑	☑	

⑪ Inspection		Initials
Passed ☐	Failed ☐	

3V	1.044
+2V	0.915
-2V	2.197

⑫ Mounted on Ladder #	EAST (P-Pigtail-Pin)	WEST (N-Slot)
25	☐	☑

Comments:

49V 70 μA