

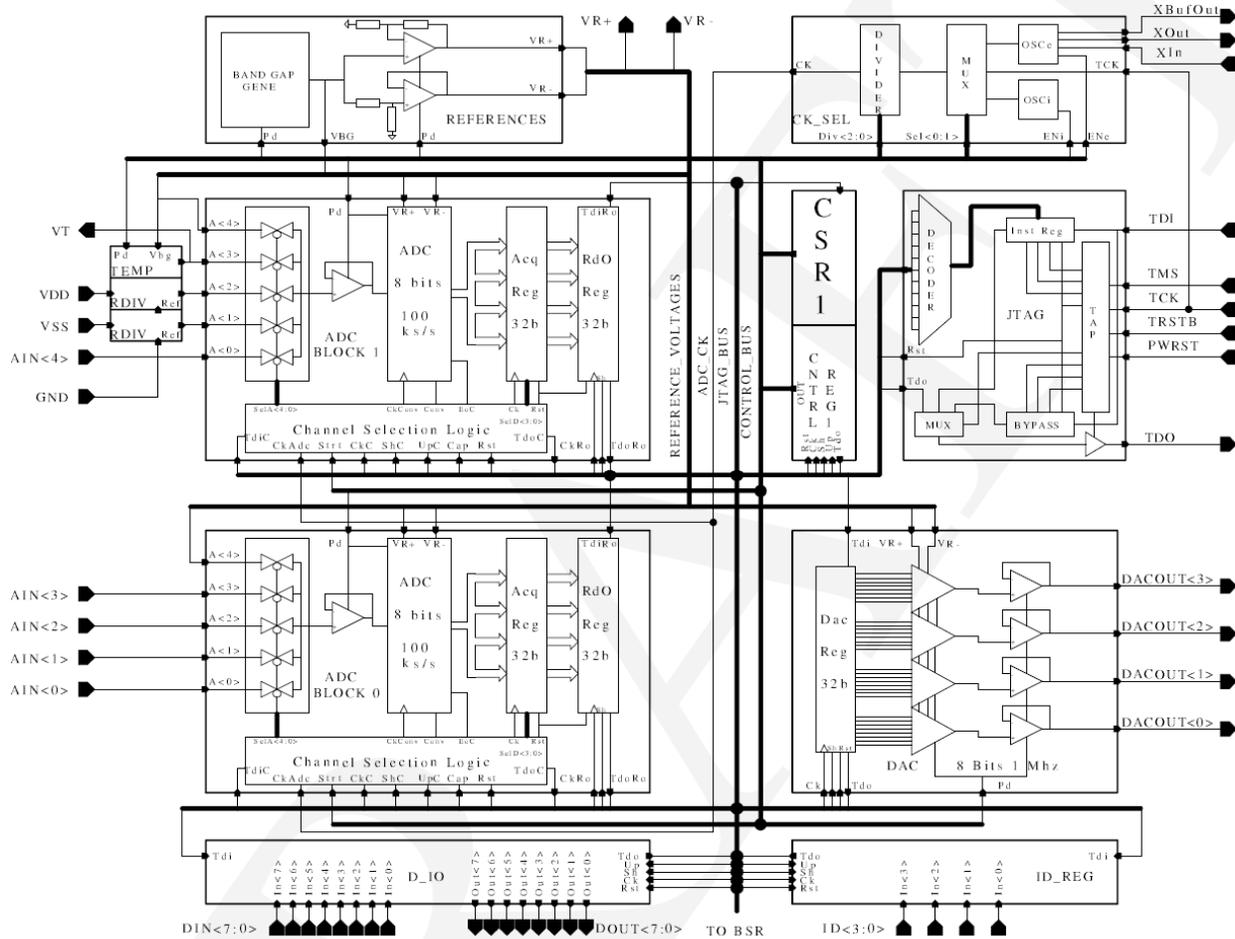
COSTAR Utilization Manual for STAR SSD upgrade (model Run99)

1. Introduction

The COSTAR chip is a circuit that allows the control of a number of analog and digital parameters. Its main features and subsystems are:

- Two 8-bit ADCs with 4 input channels
- One 8-bit DAC with 4 outputs channels
- Block of internal-reference voltage generators for ADCs and DACs conversion
- One temperature sensor
- Clock source and Frequency divider selector
- JTAG communication controller

2. COSTAR Block Diagram



3. JTAG Controller

The COSTAR chip is accessible using the JTAG protocol for communication. The state machine of the JTAG controller of COSTAR follows the norm 1149.1. The chip is located last in the JTAG chain of each hybrid after 6 Alice chips.

The controller is adapted to operate at a frequency of 20 MHz. It was verified up to 10 MHz. On PWRST or TRSTB active low, it generates an internal reset signal for the entire circuit. The BYPASS register is selected by default

Instructions	HEX-BIN Address	Register Name	Length in bits	In Use
EXTEST	00 – 00000	BSR	20	NO
HIGHZ	01 – 00001	BYPASS	1	NO
SMPL_PRLD	02 – 00010	BSR	20	NO
INTEST	03 – 00011	BSR	20	NO
CLAMP	04 – 00100	BYPASS	1	NO
CSR1	10 – 10000	CONTROL REG 1	8	YES
ADCTEST_0	11 – 10001	ADC TEST REG 0	4	YES
RO_ADC4_0	12 – 10010	RO_ADC4_0	32	YES
ADCTEST_1	13 – 10011	ADC TEST REG 1	4	YES
RO_ADC4_1	14 – 10100	RO_ADC4_1	32	YES
IN_OUT_REG	17 – 10111	IN_OUT_REG	16 ¹	NO
DAC4_0	18 – 11000	DAC4_0	32	NO
CSR2	1A – 11010	CONTROL REG 2	8	YES
ID	1B – 11011	Identification REG	8	YES
BYPASS	1F – 11111	BYPASS	1	YES

4. Modes of operation

(a) Normal

An 8-bit ADC generates continuously and sequentially, through a multiplexer, converting 4 analog inputs. The conversion result is loaded successively in one of the four 8-bit registers available for storage. During reading, the value of these four registers is transferred using JTAG protocol, LSB of channel 0 is send first. The module may be turned off to reduce the power consumption of the circuit.

After reset, a counter- selector position and analog multiplexer is set to the first channel. Once the conversion is allowed, the ADC converts in 9 clock cycles, typically 9 μ s ($f_{max} = 1$ MHz). At the end of the conversion, the result is saved in the storage register corresponding to the analog channel. On the clock edge after the cycle conversion is over the conversion of the next channel begins. ADCs dynamic is V_{RP} - V_{RN}.

Reading:

During the CAPTURE-DR phase of the JTAG protocol, the four storage data registers are copied into the read registers (readout), then routed to the outside of the circuit via the TDO output during the SHIFT-DR phase of JTAG.

¹ Length not confirmed, this is a register for 8 channels of input and 8 channels of digital output

Protocol for Analog reading in Normal operation mode:²

1. Set Control Register 1 with: Conversion off, f/8 and internal clock. CSR1 = x"32"
2. Set ADC Test Register with: Enable ADC counter and normal operation mode. ADCTEST_? = b"00xx"
3. Start the conversion: assert the conversion bit on Control Register 1. CSR1 = x"B2"
4. Wait for the 4 conversions to take place: min time = 40 μs. In Run 7 the scripts were waiting 10 ms
5. Stop the conversion: disable conversion bit on Control Register 1 CSR1 = x"32"
6. Read the result. Values in RO_ADC4_?

(b) Test

This mode is accessed via the ADCTEST_? register bit 2, each ADC block scans the output voltage of the Band Gap generator used to establish the reference voltages³. In this case, after selecting the routing of the Band Gap generator to the ADC and started the conversion, the result can either be saved successively in the four storage registers or continuously in the same register by selecting the desired channel in ADCTEST_?⁴.

Protocol for Analog reading in Test operation mode:²

1. Set Control Register 1 with: Conversion off, f/8 and internal clock. CSR1 = x"32"
2. Set ADC Test Register with: either successive storage or single register storage, Test operation mode or Single Normal mode when single register is asserted and desired channel when single mode is on.
ADCTEST_? = See ADCTEST_? Description to select desired configuration
3. Start the conversion: assert the conversion bit on Control Register 1. CSR1 = x"B2"
4. Wait for the 4 conversions to take place: min time = 40 μs. In Run 7 the scripts were waiting 10 ms
5. Stop the conversion: disable conversion bit on Control Register 1 CSR1 = x"32"
6. Read the result. Values in RO_ADC4_?⁴

5. Register Description

• **ADCTEST_0 and ADCTEST_1 register**

Bit	Name	Comments	Run7
3	DisCnt	1 = ADC counter blocked, selecting only one channel ⁴	0
2	SelBG	1 = Test Mode: VRN and VRP are in the input of the ADC ³	0
1	Cnt <1>	MSB counter selection of analog channels	0
0	Cnt <0>	LSB counter selection of analog channels	0

• **CSR1**

Bits	Name	Comments	Run7
7	Convert	1 = Start conversion	1 or 0
6	Div <2>	MSB divider clock frequency of the ADC	0
5	Div <1>		1
4	Div <0>	LSB divider clock frequency of the ADC	1
3	NU		0
2	NU		0
1	SelOsc <1>	2 = Internal Oscillator, 3 = TCK	1
0	SelOsc <0>	0 = no, 1 = External Oscillator	0

² ? could be 0 or 1 depending on the ADC conversion block that you want to access.

³ To determine which block scans VRP and VRN

⁴ The result will be stored in channel n-1 of RO_ADC4_? Where n is the channel selected on ADCTEST_?

Control Register 1 is used to start and stop the conversion, select the frequency divider and clock source. During the loading of the register, the previous value is present on the TDO serial output.

Div	Frequency division
0	f
1	f/2
2	f/4
3	f/8
4	f/16
5	f/32
6	f/64
7	f/128

SelOsc	Clock Source
0	No Clock
1	External Oscillator
2	Internal Oscillator
3	TCK

An oscillator period of 150 ns is integrated in the circuit. The divider set to f/8 produces a clock frequency compatible with the operation of the ADCs.

- **CSR2**

Bits	Name	Comments	Run7
7	NU		0
6	OffREF	1 = Band Gap reference voltages generator off	0
5	OffTEMP	1 = Temperature sensor off	0
4	NU		0
3	OffADC<1>	1 = ADC block1 off	0
2	OffADC<0>	1 = ADC block0 off	0
1	NU		0
0	OffDAC	1 = DAC block off	0

Control register 2 controls the power supply to different modules. During the loading of the register, the previous value is present on the TDO serial output.

- **RO_ADC4_0 register⁵**

Last TDO						First TDO	
Channel 3		Channel 2		Channel 1		Channel 0	
MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
$V_3 = V_{in} + VSS$		$V_2 = V_{in} + VSS$		$I_{bias} = \frac{V_{in} + VSS}{RL1}$		$I_{guard} = \frac{V_{in} + VSS}{RL1}$	

$$V_{in} = Code_{ADC} \left(\frac{VRP - VRN}{256} \right) + VRN$$

$$RL1 = 100 \text{ k}\Omega^6$$

⁵ Notice that in order to convert the values in block0 we need to know VSS beforehand, VSS is located in block1.

⁶ This value was used in the Labview interface, 150kΩ is another value used found in the slow controls data base of run 7.

- **RO_ADC4_1 register**

Last TDO						First TDO	
Channel 3		Channel 2		Channel 1		Channel 0	
MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
$Temp = CFA * Code_{ADC} + CFB$		$VDD = \frac{V_{in}}{Rdiv} + VSS$		$VSS = -\frac{V_{in}}{1 - Rdiv}$		$V_0 = V_{in} + VSS$	

$$V_{in} = Code_{ADC} \left(\frac{VRP - VRN}{256} \right) + VRN$$

$$Rdiv = 0.4$$

$$CFA = 0.36 \quad CFB = -5 \text{ to } -22^7$$

Power supply is measured using a voltage divider bridge with ratio $Rdiv = 0.4$. The real COSTAR reference is VSS. The VSS measurement is in fact a measure of GND compared to VSS.

Measurements of VDD and VSS are possible within the operating range of COSTAR: $VDD + 20\%$, $VDD - 20\%$, $VSS - 20\%$ and $VSS + 15\%$. ie: +2.4 V, +1.6 V, and -2.4V,-1.7V.

- **DAC4_0**

Last TDO						First TDO	
Channel 3		Channel 2		Channel 1		Channel 0	
MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
$V_3 = V_{DAC}$		$V_2 = V_{DAC}$		$V_1 = V_{DAC}$		$V_0 = V_{DAC}$	

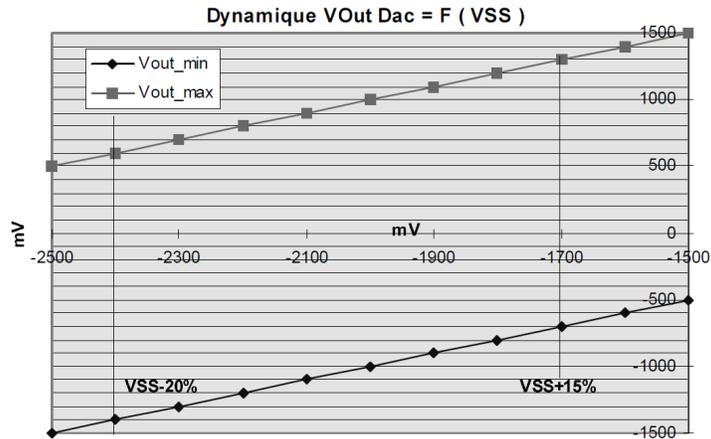
$$V_{DAC} = Code_{DAC} \left(\frac{VRP - VRN}{256} \right) + VRN + VSS$$

At reset the default value for the DACs is 127. The module can be turn off to save power, it is not in use for the SSD upgrade, in older version of the ladder card channel 0 was used to compensate the peristaltic pattern of the hybrid. Potentially channel 0 is wired on the flex cable pin 5. During the loading of the register, the previous value is present on the TDO serial output.

Each channel is capable of driving loads 2kΩ min. and 1 nF max. To a voltage output between VRN and VRP.

As VRN and VRP are stable with respect to VSS, VSS will cause a change in a identical VRN and VRP slip relative to the ground. The chart below shows the variation of a DAC output based on $VSS = 1V$ VRN and VRP = 3V. The terminals on VSS are the characteristics of the circuit.

⁷ CFA and CFB are individual values for each hybrid, please check the data base to know them



- ID

The ID register is used to read the cable identification number on the pad ID <3:0>. The 4-bit ID <7:4> is set to 1010. So far the modules have shown the lower part set high, putting the ID = x"AF"

- BSR

Last TDO				First TDO				
ID<3>	...	ID<0>	DIN<7>	...	DIN<0>	DOU<7>	...	DOU<0>
MSB		LSB	MSB		LSB	MSB		LSB

We can read the status of inputs and download test vectors that replace the output values. This is done by executing the SAMPLE-PRELOAD and EXTEST instructions. The CLAMP instruction sets the outputs to the value loaded into the BSR. The instruction HIGHZ sets the output bus to high impedance. Instructions CLAMP and HIGHZ select the BYPASS register.

6. Characteristics

Characteristics	Value
Global	
VDD power supply	+2 V +20%, -20% or +1.6V, +2.4V
VSS power supply	-2 V -20%, +15% or -2.4V, -1.7V
Idle current after RESET	6 mA
Temperature range	20°C - 80°C
Reference Voltages	
VRP	+3
VRN	+1
Stability	+/- 1 LSB
Dispersion	+/- 1 LSB
DAC	
Channels	4
Resolution	8 bits
Dynamic	VRP-VRN
Typical conversion time	< 1 μs Max 2 μs

Load	> 2 k Ω
Capacity	< 1 nF
Linearity	+/- 1 LSB
Dispersion between channels	+/- 1 LSB
ADC	
External Channel	5
Internal channel	3
Resolution	8 bits
Dynamic	VRP-VRN
Conversion frequency	Min 500 Hz – Max 1 MHz
Conversion time	9 clock cycles
Duty Cycle	Min. 40% Max. 60%
Linearity	+/- 1 LSB
Dispersion between channels	+/- 1 LSB
Temperature sensor	
Range	20°C - 80°C
Sensitivity	22 mV/C° or 0.36°C/ADC bit
Dispersion	+/- 1 LSB
Digital signals	
Logic levels	1 = VDD, 0 = VSS
Rising and falling time	< 50 ns
Output current	4 mA
JTAG frequency	Min 500 Hz – Max 20 MHz