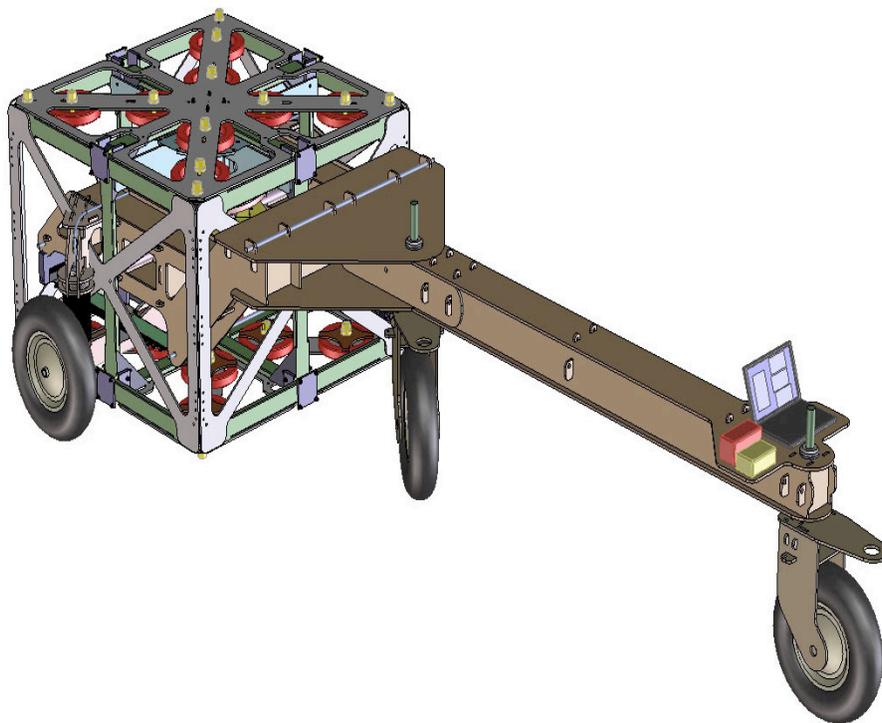


UXO Engineering Design

Annual report



1. Introduction

The design and fabrication of the UXO detector has numerous challenges and is an important component to the success of this study. This section describes the overall engineering approach, as well as some of the technical details that brought us to the present design.

2. System requirements and description

While the main specifications of the system and its expected performance have been described before, it is necessary to summarize the main system requirements to guide the engineering approach to the design and fabrication of the device.

Due to the nature of the device, it is important to minimize the metallic content of the structure: all elements are going to be made out of a combination of wood, plastics and fiberglass. The only areas with conductors, besides the driving and sensing coils, are going to be the associated with the data acquisition system, which we plan to position at a certain distance from the driver/receiver cube.

In addition, the system will be equipped with and powered by a battery capable of running the whole system from pulsing to recording data for a minimum of two hours. Appendix 1 (Larry please send it!) provides the basic calculations for sizing the battery.

A critical design decision is that to wire the sensors directly into the data acquisition system as opposed to processing the signals at the sensors and transmitting the resulting data via air or fiber optic. The choice of wiring the sensors allows a simplified installation and electronics configuration, and requires that the pre-amplifiers first seen by the sensor wires present a high impedance to prevent current flows that could be induced by the excitation field and result in measurement errors.

One of the main challenges to the data acquisition system is the very large dynamic range that it will be facing. This is driven by the specifications described earlier. Using $2nV/\sqrt{Hz}$ as the nominal performance of low noise amplifiers, one can calculate the noise floor of a good front end amplifier to be at least $1\ \mu V = 2nV \times \sqrt{200kHz}$, assuming a 200kHz noise band. The resulting amplitude of the excitation pulses correspond to peak-to-peak voltages in excess of 100 V. The resulting dynamic range, in excess of 160 dB is achieved by a combination of active switching and sensor configuration. Part of this dynamic range is provided by the configuration of the sensors and their location, where symmetry allows for cancellation of the drive signal while the response from UXOs is seen and adds in the two sensors. We have measured a drive signal cancellation of about 50:1.

The choice of noise floor was carefully made to consider all sources. In particular, we selected low noise pre-amplifiers and established their expected noise floor. We then designed sensing coils to have an intrinsic noise below that of the amplifiers, so that the sensors would not be the limiting factors. A full characterization of the system noise was made in several configurations, from single sensor, to the full 8 sensor pairs.

Particular attention is also required to ensure the portability of the system, not only does it need to move and scan across fields, but it needs to be easily transported, assembled and maintained.

3. System description

The system block diagram is shown in Figure 1. A logic board controls the drivers for the three coils that excite each of the three planes. The same board also triggers the data acquisition system, selects and pre-processes the data and interfaces with the main local computer system.

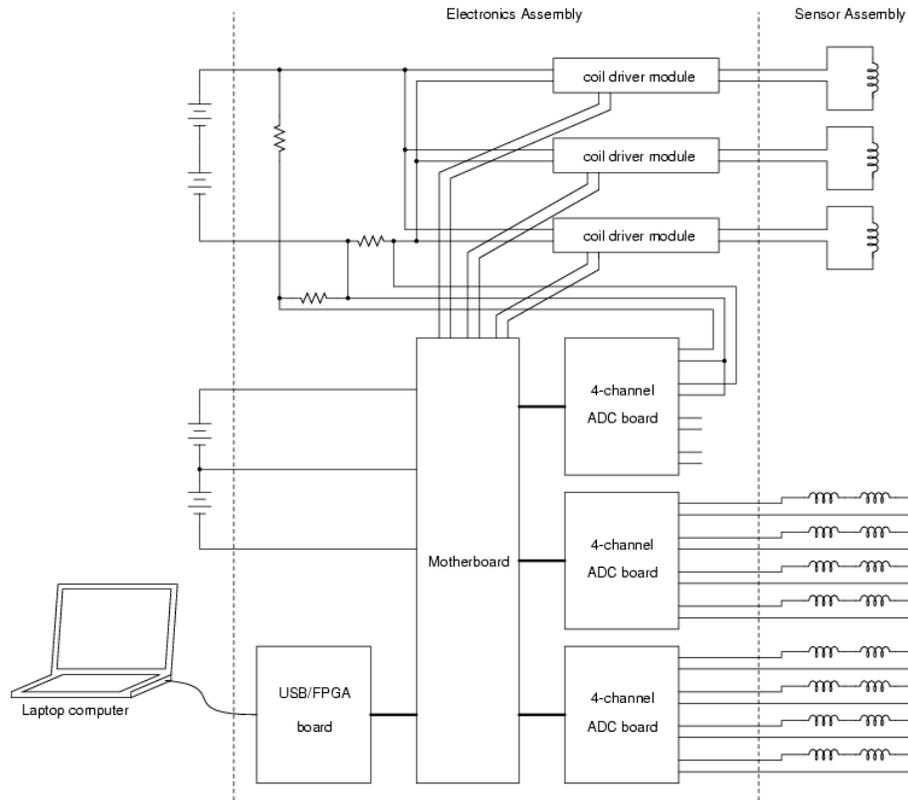
Particular care is given to the grounding of the system and its relation with drivers and sensors, as it can be a dangerous source of undesired noise, which could reduce the resolution of the system.

A local computer is connected via the USB port to the logic board. Such computer is going to initially perform all data processing, including the visualization of the results. The USB link is one of the current restrictions on the system, since the total data throughput of all channels at 16-bit resolution when digitizing at the full 500kS/s exceeds the capability of the USB bus.

We are therefore planning to have two modes of acquisition, one at high resolution, and one at standard resolution. In normal mode, we plan to perform stacking of multiple shots on board, and passing on the processed data to the local computer. When the data processing on the computer requires the full batch of data, we plan to reduce the duty factor of the drivers, so that the resulting data can be passed on to the local computer within the limitations of the USB bus.

UXO System Block Diagram

Larry Doolittle, LBNL
November, 2004

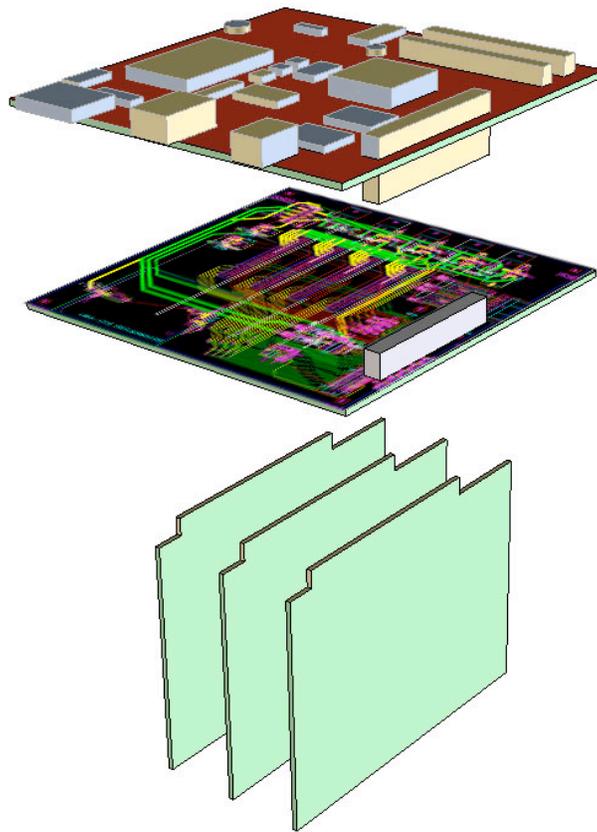


4. Data Acquisition and Processing System

The heart of the system is an FPGA-driven embedded processor. This programmable smart chip will drive all timing and system synchronization, interface with the data acquisition boards and after receiving the digital data, it will process and store in on-board DDRAM. This FPGA is also going to manage the data transfer to the main computer where the data will be stored in large sizes and displayed. Among the timing information generated, the processor will provide triggers for the pulsers, as well as gain switching information to the data acquisition system.

In order to minimize expenses and expedite system development, we adopted a standard development board based upon the Xilinx Virtex II Pro FPGA. This board (shown in red in Fig. 2) provides readily available network and USB connections, and allows for easy and simple loading of FPGA firmware on

board. It also contains a boot memory chip to load firmware on power-up. The logic board interfaces with a custom developed motherboard that carries all power and receives up to 4 data acquisition cards, each capable of 4 channels each. Only three are shown in Fig. 2, since we are currently planning to instrument only 12 channels and leave the extra capacity available for future expansion.. The data acquisition chain is based upon 16-bit digitizers capable of sampling up to 500 kS/s and described in detail in a later chapter of this report, together with the design of the low-noise analog front end signal processing.



5. Engineering approach

We have taken a step-wise approach to the engineering of the device. On one side, we want to arrive to experimental results as early as possible, on the other we don't want to compromise the chance of making an easy transition to a final design that can be transferred to industry for production and distribution. As a result, we have been using two 4-channel oscilloscopes to acquire data from the 8 sensor pairs, and the memory built in the scopes for stacking and averaging up to 100 acquisition events. This data is taken at 8 bits, while the 16-bit custom electronics is under development, and allows us to compare with the experimental results obtained last year on the proof-of-principle tests made with a much simpler system based upon smaller sensors that were not paired up to leverage the cancellation of the drive pulse.

At present we have completed the data acquisition at 8 bits and have started the bench tests of the 16-bit system with gain switching. The comparison with last year's data indicated an improvement of approximately one order of magnitude in device resolution.

A similar approach is planned for the firmware implementation, where we intend to add features and functionality incrementally, and slowly move on chip many of the functions and operations that we will be performing at first on the local computer.

6. System Modeling

In order to develop a good understanding of the system and a useful analytical tool, we modeled the system both with a mathematical model and with an equivalent circuit. Both models reflect the mutual coupling between drivers and objects, and include the first stage of analog processing. In the equivalent circuit we could also study noise behavior.

Insert Larry's notes here

7. Cart design and description

Insert Robin's part

8. Driver Design

The driver is based on a half sine generated by resonating a capacitor with the inductance of the drive loops. SCR switches, triggered by the logic board, control the waveform and are optimized to prevent bouncing of undesired effects from the turn-on or turn-off transients that could interfere with the detection of UXOs.

Insert Jimmy's part here

9. Conceptual design of the sensors

The sensors are critically damped loops, resonant at 20 kHz by the addition of an adjustable external capacitance. The final choice of diameter, wire size, number of turns was a compromise between sensitivity, self-resonance, internal resistance, and resolution. In the end, we settled for 6" ID, 500 turn sensors. While a larger diameter results in a higher sensitivity, it also reduces resolution as the signals are more distributed. Likewise, more turns offer a stronger signal, but lower the coil's self resonance which needs to remain above the desired operating band.

The performance of these sensors was compared to that of the original 3.5", 100 turns sensors used in the proof-of-principle system

Particular care is needed when tuning sensors, both individually and as a sensor pair. We built a board containing all passive networks used for tuning and critically damping. Each sensor is first tuned and individually damped. Then the sensors are paired, and their shields connected together to ground, while a balancing capacitor is added. All adjustments are done at board level. When we completed all sensor pairs, they measured very close to each other.

More comments if needed

10. Sensor fabrication

Insert Jimmy's part here

11. Electronics Design

Insert J-F' section here???