ALICE PHOS ELEC 2005-XX

Front End Electronics

for the

PHOS electromagnetic calorimeter[1]

Alice Note

Issue: [1]
Revision: [6a]

draft

1. Funding agencies: a.) Ministry of Atomic Energy and Ministry of Industry, Science and Technologies of Russian Federation, b.) Norwegian Research Council, c.) INTAS project 03-5747

Reference: Alice 2005-XXX
Created: 19 July 2004
Last modified: 25 Mai 2005

Editors: Hans Müller, Rui Pimenta CERN PH-AIO, Geneva, Switzerland

Qingxia Li, HUST E&I Department, Wuhan, China

contributing PHOS collaborators
B.Skaali, P.T.Hille - Univ. OSLO- Physics + D.Rohricht, J.Alme - Univ. Bergen-Physics
Qingxia Li, Xi Cao, Li Tan,Gang Su,Yinzhuang Liu, Guangxi Zhu- HUST,Wuhan, China
I. Sibiriak, A. Vinogradov, M. Ippolitov, V.Manko - Kurchatov Center, Moscow, Russia D. Budnikov, A.Kouryakin - RFNC-VNIIF Sarov, Russia
S.Sadovsky, M. Bogolyubsky -IHEP Protvino, Russia
J.Vallaeys - ISIMA Clermont Ferrand, France
Toru Sugitate, Particle- & Astro-Physics ,Hiroshima Univ., Japan
Hans Muller, Rui Pimenta - CERN PH-AIO, Geneva, Switzerland

Acknolwedgements for TPC electronics project
L.Musa, A.Junique, B.Mota, R.Campagnolo, C.Gonzales - CERN PH-ED

Project history

This document summarizes the CERN / Wuhan project of 2004 for design and prototyping of new Front-End Electronics (FEE) for the electromagnetic PHOS calorimeter.

The FEE project started at CERN early 2004, using the TPC FEC card by L.Musa and his CERN team as a template for the PHOS FEE card, in particular what concerns the grounding scheme, the use of the Altro chip and the readout backend. The special requirement for PHOS was to achieve high energy and timing resolution with APD diodes at a relatively large detector capacitance of 100 pF and to include individual APD bias voltage regulation on the 32 channel FEE electronics cards.The project was conceived from the beginning as co-design of FEE and Trigger Region Unit (TRU) cards, with fast-OR interconnections and with a common powering and water cooling scheme. The TRU and FEE share a common GTL bus segment with 14 FEE cards and 1 TRU card, which effectively segments PHOS modules into 8 TRU domains. Since two TRU domains are read out by one RCU, one PHOS module consists of 4 RCU partitions. The conceptual design of the TRU trigger was adressed first in order to define the interfacing requirements for the FEE electronics. The FEE prototype design, construction, test and revision were completed in 2004, followed by the design of the TRU in 2005. The first ideas for OP-amp-based signal shaper and fast-OR shaper were inspired early 2004 by Iouri Sibiriak. The 32 channel FEE card design for a 14 bit dynamic range parameters was frozen at CERN in Mai 2004. It was implemented with dual-gain, semi-gaussian shapers, 10 bit ALTRO digitizers, controller FPGA and a digital readout backend imported from the TPC. The chief electronic designer of the FEE card (Cadence schematics, components choice and procurement, power and grounding scheme) was Rui Pimenta. Cao Xi performed the Allegro layout of the 10 layer FEE card in Wuhan which was was finalized in August 2004. Li Tan & Gang Su organized the prototype production in China and delivered the first 8 FEE cards in time to CERN for the october T10 testbeam. Jerome Vallaeys wrote at CERN the first USB driver and PROM download utilities for the FEE cards. The 32-fold High Voltage Bias control logic for the FEE card was developed by A.Vinogradov. Qingxia Li joined the CERN team in April 2004 as first member of the HUST team at CERN in order to design and evaluate the first CW shaper prototype mezzanine which was tested in the August 2004 testbeam. He participated in all essential aspects of the FEE design project, including evaluation of first FEE electronics cards in the SPS testbeam. In 2005 Qingxia Li coordinates the volume FEE production and acceptance tests in Wuhan with his team which also took committement for the Phos Control and Monitoring (PCM) firmware, including APD bias control and USB communication. The remotely configurable PCM logic is an essential part of the FEE card and vital for the RCU-based readout. Still under development, the PCM will be documented later by the HUST team. The FEE prototying project, carried out at CERN within specially created Electronics PHOS lab was mostly financed by the Norwegian PHOS group (Bergen and Oslo) and by the INTAS Project project 03-5747 under leadership of B. Skaali. The mechanical design for the embedded electronics and cooling inside the PHOS spectrometer was worked out mostly by CERN in collaboration with D. Budnikov of Sarov, coordinator of the manufacturing of FEE cooling cassettes and of the embedded support structures in Russia.The beamtests and physics data evaluation with first FEE prototypes at the SPS with electron triggers were coordinated and orgainized by M.Ippolitov. Utilities for Root offline data evaluation were provided by A.Kouryakin. A very first version of an APD bias control screen was provided by P. T. Hille who als wrote his thesis on TOF resolution of PHOS. Johan Alme was responsible for the FEE readout via the DCS processor subsystem on the RCU. The Protvino team under S.Sadovsky maintained the operation of the testbeams and provided the LED mnitoring system. The important FEE card peripherals, T cards, APD diodes and CSP pre-amplifiers have been finalized and produced by

T.Sugitate and his team. The revision of the Version 1.0 FEE prototypes as well as RMS noise and time resolution measurements with blue LED pulsers were finalized by the PHOS CERN team by the end of 2004, followed by teh CERN / Wuhan FEE revision V1.1 as pre-version for production readiness in Mai 2005 in Wuhan.

PHOS FEE summary

The PHOS channel connectivity, it's readout and control methods, as well as the powering and cooling methods are designed for >10 year operation inside a closed volume in which both frontend, trigger and control electronics is embedded.

A PHOS module contains 3584 P_bWO_4 crystals in a cold zone of -25^0 C, separated by an isolation layer from the warm volume which encloses the electronics. Each crystal is glued to an Avalanche Photo Diode (APD) and a charge sensitive pre-amplifier (CSP) of ~ 1V / pC sensitivity with a maximum range of ca. 5 pC. The APDs are operated at moderate gain for the low noise and high gain stability required for achieveing best energy and timing resolution. With a nominal APD gain of M=50 and an intrinsic PWO light yield of 10 photoelectrons per MeV, ca. 200 electrons per MeV are generated in the APD by primary EM particles. The PHOS Charge Sensitive Amplifier (CSP) converts the charge signal over a 1 pF capacitor into a voltage step which is formed by the shaper into a semi-gaussian pulse-shape. After the CW shaper, the noise background of a dark detector is ca.600 electrons, hence EM particles with an energy of more than 3 MeV emerge from the noise background of a single channel.

In order to allow for inter-calibration to a level of <1 % for obtaining best energy resolution at high energies, the bias voltage of each APD can be set to a precision of 0.2 Volt / bit. With a gain dependence of 3% per Volt at gain M=50, the hardware gain calibration limit is 0.6%. For hardware gain calibration, 32 remotely controlled precision HV bias regulators are integrated on the Front End Electronics (FEE) cards together with the 64 shapers / digitizers, board controller, USB processor and an elaborate power regulation system which carefully avoids noise coupling from digital or High Voltage section to the analog signal section.The FEE electronics has been designed for a 14 bit dynamic range of the PHOS calorimeter in the range between 5 MeV to 100 GeV with energy resolution of 2% at 2 GeV and a timing resolution aiming for 1 ns at 2 GeV. Both goals are somewhat incompatible since high energy resolution at low energies is conditioned by low noise and consequently by a narrow bandpass for the charge signal, whilst best timing resolution is conditioned by a wider bandpass for the high frequency parts of the signal, which increases the noise. Some R&D on two competitive shaper approaches were conducted by the CERN / Wuhan team and later by Iouri Sibiriak of Kurchatov. On the FEE prototype, both the Kurchatov and CERN / Wuhan shapers had been implemented[1]. The CERN / Wuhan (CW) shaper is a second order CR-2RC bandpass for 80 kHz cutoff, achieving a 600 electron single channel RMS noise level. With 200 electrons per MeV, a single channel 3 MeV noise level is compatible with a 11 MeV noise term for the energy resolution of a shower distributed over 3*3. The test of two prototype FEE cards in the october testbeam with an electron beam up to 4 GeV allowed verification of all major design parameters. The results with the CW shaper led to a modest layout revision in order to remove suprious noise couplings which were present during the testbeam. The K shaper option will be revised & tested and may be subject of a future FEE card revision.

1. mutually exclusive implementation choice for CW or K shaper

Each CW shaper channel is split via a low noise gain buffer into high and low gain shapers for a total dynamic range of 1/16000 (14 bit) with two 10 bit digitizers. Four ALTRO digitizer chips with 16 ADC's and internal multi-event-buffers are required for a total of 64 high-gain/low-gain channels per FEE card. The choice of the Altro chip, combined with a board controller FPGA, allows that PHOS can re-use the readout backend protocol of the ALICE TPC via an external Readout Control Unit (RCU).

With a shaper bandwidth of < 0.5 MHz, the effective number of bits with the 10 bit Altro is 9.7 bits for sampling frequencies above the Nyqusit frequency of 1 MHz. Overclocking of up to 20 MHz may be applied in order to improve the offline TOF determination[1]. The TOF determination was so far based on offline fits to the Gamma-2 pulse-shape produced by shapers with different bandpass ranges, corresponding to 2 and 4 us peaking time. With preliminary blue LED pulser tests in November 2000 in the laboratory, a worst-case differential timing resolution of ca 2 ns in the region of 2 GeV was established with a CW shaper peaking time of 4 us (80 kHz bandpass). The TOF resolution is still under improvement, since it not only depends not only on the shaper time constant but also on the setup (LED pulsers, sampling rates, clock jitter, energy calibration[2]) and on the offline methods (clock phasing, sample binning and rising edge information). The final choice of the optimal shaper time constant as best compromise of energy resolution and timing resolution is kept open[3,4] until mass production is launched.

Each FEE card connects to 2 parallel rows of PWO crystals, allowing that 8 analog charge sums of quadratic 2 * 2 crystals can be generated on the 32 channel FEE card. These fast-OR signals are extracted from the input of the shaper and passed through a simple 100 ns RC-shaper. Eight analog sums per FEE connected via short differential cables of equal length to the Trigger Region Unit cards (TRU). A TRU card receives in this way 112 analog sums from it's 14 surrounding FEE cards. ADC's of 8 bit and 40..60 MHz sampling are used on the TRU to generate digital images of 448 crystal towers in space and time within a single FPGA. The trigger algorithm within the FPGA applies sliding window and peak finder algorithms for successive level-0 and level-1 trigger generation with programmable thresholds for simultaneous low, mid and high p_T trigger outputs (LVDS) at a decision rate of 40 MHz.

Inside a PHOS module, there are eight readout and trigger domains (TRU domains), each consiting of 14 FEE cards for a crystal region of 28 * 16. Each domain is read out by a custom, 200 Mbyte/s GTL+ bus of 1 m length[5] under mastership of an external RCU card. Each of the four external RCU cards masters two TRU domains via a custom GTL bus and each RCU with it's DDL data link to an LDC computer constitutes one PHOS readout partition.

1. the number bits at the pulse peak over a fixed dynamic range implies a 1/E dependence of the TOF resolution, hence efforts are underway to increase the effective dynamic range via overclocking
2. The energy calibration of the crystals used in the laboratory was not known better than 40%.
3. Timing constants for the CW shaper corresponds to a set 5 different R and C values per channel
4. The FEE card layout is unaffected by the shaping time choice
5. 60 cm bus and 40 cm flat cable

The power dissipation of embededd FEE/TRU electronics in the PHOS warm volume corresponds to ca. 0.9 kW, extracted via a (leakless) water cooling system which is standard at CERN. For this purpose, each FEE or TRU card is sandwiched in a copper cassette which are cooled by water-flown copper pipes. The use of under-pressurized water prevents from leaks inside the ectronics enclosure.

Control and monitoring access to the FEE card resources is implemented in programmable firmware logic on the FEE cards, named Phos Control and Monitoring (PCM). This slave logic allows that the RCU has address-mapped access to both control and data sections on the FEE cards. The address space includes Altro-chip internal registers, APD bias control registers, and registers for voltages, currents and temperatures. A USB port allows that an external USB master (lika a PC) may be used to emulate the RCU for production testing, local servicing and for updating of the Flash Prom.

The FEE revision from the V1.0 prototype to the FEE card V1.1 described in this document consists mainly in noise reduction measures, which substancially lower the initially measured spurious noise level per channel from 2.4 to 0.41 ADC counts (without detector). The signal traces between the input connector and the shapers have been equalized to the same length. A board switch was added, allowing to change the FEE card from USB test mode into RCU readout mode. The HV input was equipped with a HV clamping diode to protect from overvoltages above 390 Volt. The two shaper options (CW or K) have been maintained on FEE version 1.1 though the first K shaper implementation is considered obsolete. With the mathematical methods layed out in this document, the componet values for CW shaper time constants and gains can be re-calculated and changed if required.

The associated TRU trigger electronics for PHOS is subject of a 2005 project at CERN and will be documented separately

.Document Status Sheet

Table 1 Document Status Sheet

1. Document Title: Front End Electronics for PHOS electromagnetic calorimeter			
2. Document Reference Number: Alice 2005-XXX			
3. Issue	**4. Revision**	**5. Date**	**6. Reason for change**
1Draft	0	19.07.2004	Complete update with results from first FEE cards in testbeam, after November PHOS meeting in 2004
1Draft	1	22.1.2005	Summarizing all CERN/Wuhan FEE project information from 2004 in one document
1Draft	2	25.1.2005	Revisions, corrections, additions, replacments
1	3	15.3.2005	Updates, additions, corrections, Release
1	4	30.3.2005	Spellchecking, readability and last corrections/updates
1	5	22.4.2005	latest updates, connectors, power, T cards
	6a	25.05.2005	Addition of complemetary information and new chapters for Wuhan Review release, small correc tions in Rev 6a.

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Overview and FEE parameters

The PHOS electromagnetic calorimeter consist of 5 identical modules of 64*56 PWO crystals installed below the Alice TPC. Each module maps with one TPC sector an azimuthal angle of 20 degrees corresponding to 64 PWO crystals of 22 * 22 mm ^{2} * 180 mm.

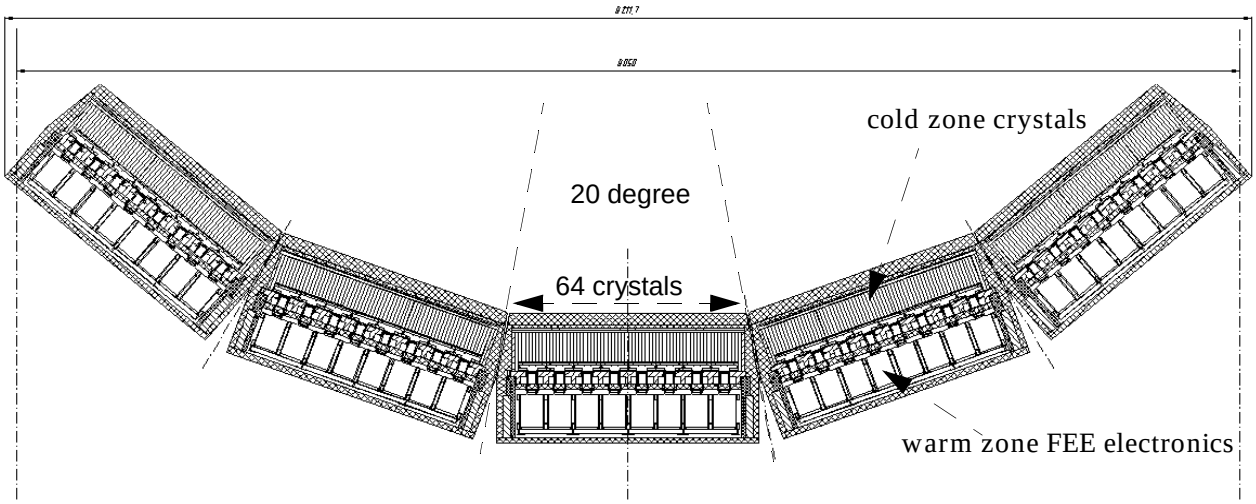

Figure 1 Arrangement of the 5 PHOS modules

Each 20-degree sector measures 1443 mm at a nominal radius of 4.6 m from the beamline center. A single crystal in the center of the module represents an angle of +- 0.135 grad. The non-radial arrangement of the crystals per module implies however a tilt of the incident photon angles up to max. 13 degrees (seen from the interaction point).

The pseudorapidity range of $\eta < |0.12|$ is covered by 56 crystals.

A single PHOS module represents a martix of 56*64 crystals as shown in Figure 2. The crystal

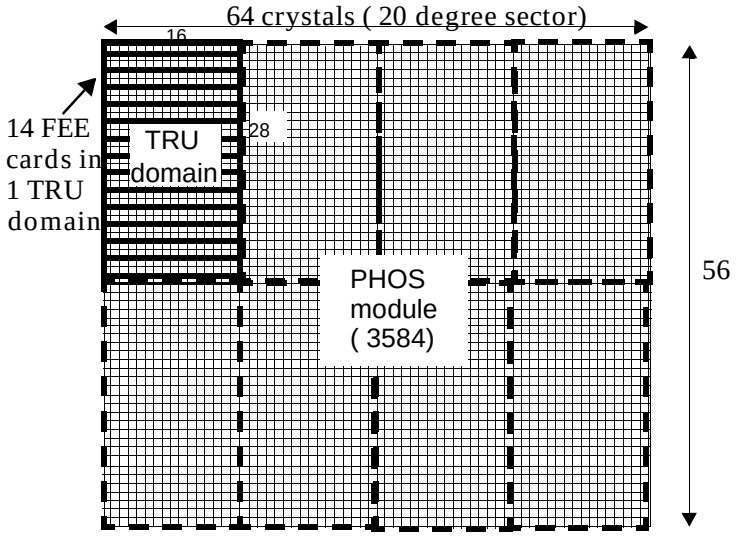

Figure 2 One PHOS module with 14 FEE cards per TRU domain. One of eight TRU domains consists of 16*28 crystals.

matrix corresponds geometrically to a matrix of electronics cards, divided in 8 TRU domains, each containing 14 FEE cards and 1 TRU card as shown in Figure 2.

The FEE electronics was designed and implemented along the following guidelines:

- maximim linearity of the APD charge conversion into a semi-gaussian pulse
- individual HV bias settings per APD channel with 0.2 Volt/bit granularity
- compromise of low APD gain M for low excess noise factor, stability against temperature and a hardware gain intercalibration limit of max. 0.6% (for M=50)
- RMS noise of 600 electrons per channel for a dark detector
- APD gain setting to 0.2 Volt precision via software controlled high voltage regulation per channel on the FEE cards
- dual gain shaper with gain ratio 1/16 for a 14 bit dynamic range
- second-order Bessel filter for linear transfer characteristics, low noise and analytically reproducable Gamma-2 pulse-shape.
- use of a 10 bit ADC with less than 0.4 bit measured quantization noise
- sampling rates up to 20 MHz above the Nyquist frequency, i.e >1 MHz for a PHOS shaper bandwidth <0.5 MHz.
- monitoring of temperatures and LV voltages and currents on the FEE cards in order to detect long-term-drifts, current variations due to high rates or due to firmware changes and to detect misfunctions
- remotely reprogrammable firmware in the embedded FEE electronics
- differential, high-current LV cabling, separate for analog and digital supply lines
- analog sum output for TRU trigger cards for up to 33 GeV from 4 crystals
- water-cooled, fully embedded electronics packaging

For a quick overview, the following tables summarize mechanical (Table 1), electrical (Table 2) and offline parameters (Table 3) of the PHOS electronics ..

Table 1 PHOS FEE, geometrical and mechanical data

PHOS component	Dimension	Remarks
PHOS Matrix	56 * 64 crystals	3584 crystals / module
P_bWO_4 crystal **Chapter 1.1**	22 * 22 * 180 mm^3 inorganic scintillator crystals 440 nm (blue) and 530 nm (green) light decay time 25 ns @ -25 C . Radiation lenth X_0 = 0.89 cm. Max. incident photon angle per crystal <13 degrees	radiation lenght for 20 cm ~ 18 100um stainless steel wrapping Moliere Radius 2.0 cm crystal weight: 721.3 g Light yield for 2004 production (Apatity) ~ 12 pe / MeV
double strip unit footprint	45.1 * 180.4 mm^2	2 * 8 crystals, 2 T-cards
T-cards and connectivity **Chapter 13**	170 * 50 mm^2 8 Crystals / T-card 8 CSP cables / 1 base connector	Base connector: 37 pin 2.76 mm AMP / Tyco Board Mount Connector (747 470-2) 6-pin CSP cable 1.27 mm with Molex 51021-0600 header and crimp terminal 50079 CSP connector on T-card: 6-pin Molex 53047-0610
Feedthrough flat cable T-card<>FEE **Chapter 13.1**	ca. 13 cm long 2 Flat cables 40 wire CERN SCEM 04.21.22.340.3 reduced to 37 pin 1.27mm pitch	Cable T-card side: 37 pin fem. 3M 8337-6009 CERN SCEM 09.21.20.130.9 FEE side: solder to intermediate PCB adapter
Warm Volume	1310*1490*245 mm^3	Encloses 112 FEE and 8 TRU-cards, 8 GTL bus strips, the RCU and Trigger OR is outside
IPCB intermediate signal adapter **Chapt. 13.4**	Left and Right adapter PCB for flat cable to FEE connector: max 90 * 630 mm PCB strips with mounting holes	FEE connector on adapter PCB Samtec LS2-130-01-S-D 14 connectors @45.4 mm pitch
FEE card **Chapt 2.1**	32 channel front-end electronics cards HUST / CERN CERN No. 0000042476 V1.1 349 * 210 mm^2	10 Layer PCB, FR4 (or S1155 Halogene free) Weight +copper cassette: 1.2 kG Input: two 60 -pin connectors Samtec LS2-1-30-01-S-D-RA1

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GTL bus strips **Chapt 9.1.1**	50 line terminated GTL+ Data bus, 54*630 mm 26 line terminated GTL+ Control bus, 30(43)*630 mm	Data strips CERN design Ref EDA-00711-V1 Data Contr. strips CERN design Ref. EDA-00712-V1 CTRL
TRU **Chapt 11**	Trigger Region Unit (TRU) 349 * 210 mm^2 Level-0 and 3* Level-1	14 octal analog sum cables of equal length connect 1 TRU with 14 FEE cards
TRU domain **Chapt 14.1**	16*28 crystals = 14 FEE cards 59*36 cm	1 of 8 local trigger domains of a PHOS module
CSP Preamplifier **Chapter 1.4**	19 * 19 mm^2 attached to PWO crystal, APD on back side	Discrete logic on PCB, with Molex connector 53047-0610
APD **Chapters 1.3 & 1.1.4**	Hamamatsu S8664-55 (S8148) 5 * 5 mm^2 ceramic, 10.6 mm	glued to PWO with Quick Stick, n= 1.7

Table 2 Electrical parameters PHOS FEE electronics

Component	Properties	remarks
CSP preamplifier (-25 C) **Chapter 1.4**	0.833 V / pC or 0.133 uV / e- 64 mW ENC = 200 e + 3.2 e / pF * C_{in}(pF) -> 520 electrons at C_{in}=100 pF linearity range 0.1 mV- 5.0 V U_{csp}[uV]=M*0.533 / MeV +69	C_f= 1.2 pF Input JFET : 2SK932 $C_{in, FET}$ = 10 pF (CSP) C_{Det} = 100 pF (CSP+APD) M= APD gain
APD diodes (-25 C) **Chapter 1.3**	APD light yield: for nominal crystal L.Y =10 ~4 pe- / MeV @ gain = 1 200 pe - / MeV @ M=50 (Excess Noise factor F = 2.27)	S8664-55 Hammamatsu (S8148) M=50 for 320V @ -25 ^{0}C C_{APD}= 90 pF Breakdown Voltage > 400 V
RMS noise after shaper for APD at -25 C **Chapter 6.4**	2nd order CW shaper 620 e- @ 4us peaking time 730 e- @ 2 us peaking	APD operated at 320 Volt and C_{DET} = 100 pF T = -25 C: I_{dark} <1 nA, M=50
Dynamic range **Chapter 4.1**	5 MeV.....81.92 GeV (= 2^{14}) -> 14 bit	design ratio High / Low-gain = 16 / 1, measured: 16.3 / 1 (see Figure 43)
CSP linear voltage ranges for C/W shaper **Chapter 3**	<u>C / W shaper:APD-gain M=50:</u> 5 MeV - 5.12 GeV : 0.137 mV - 0.1407 V (shaper gain=7.2) 80 MeV - 81.92 GeV: 2.19 mV - 2.245 V (shaper gain =0.45)	Gain for high energy range is set to 80 GeV max. single channel (= 100 GeV for a central γ) Gain ratio = 16 -> LSB set to 5 MeV
Zero-pole cancellation **Chapter 3**	pole-zero time constant at shaper measured = 67 us. Undershoot low Energy < 0.8% Overshoot high Energy 0.5 - 2.5 %	pole-zero cancels shaper signal undershoot due to auto-discharge time constant of CSP and due to ground-level offsets (linearity)

Table 2 Electrical parameters PHOS FEE electronics

Component	Properties	remarks
C/W Shaper CERN/Wuhan **Chapter 7**	Filter Order: n=2, bandwidth (-20 dB) 500 kHz τ_{peak} = 4.1us f_c = 79 kHz (τ_{peak} = 2.05 us f_c = 159 kHz) high gain = 7.2 (low Energy) low gain = 0.45 (high Energy) Dynamic range 14 bit pedestal low Energy : 26.5 ADC pedestal high Energy: 23.5 ADC Linearity <<0.5 % APD nominal gain M= 50 RMS noise w.out detector 3.1 MeV (0.62 ADC counts) differential timing resolution: <= 2 ns @ 400 ADC counts (~ 2 GeV) (preliminary)	second order Bessel low-pass with preceeding RC high pass, -20 db < f_c < -40 db pole-zero compensation, fully differential output to Altro ADC Gamma-2 with 4.1 us (2.05) peaking time. Measured τ_{peak} distribution 3.984 +- 0.044 us. CSP linearity range 0.1mV..2.4V
K Shaper (Kurchatov) **Chapter 2.2.2**	Filter Order n=2 τ_{peak} = 2.1us APD nominal gain= 100 common attenuation stage followed by gain 1 for high Energy and gain 16 for low Energy	dual stage Bessel low-pass skewed-differential output to Altro, requires > 2* times CSP linearity range up 5 V Note: to be revised
channel rate @ E_{cut}>30 MeV Pb-Pb **Chapter 10.1**	200 Hz	see Figure 80 for Pb-Pb @ 5 TeV
digitizer **Chapter 9**	Altro-16, ST Microelectronics 16 * 10 bit, ENOB = 9.7 bit for input BW < 1MHz.	Based on 10 bit, 25 MHz ST Microelectronics ADC cell TSA 1001. 15 mWatt / ADC noise < 0.4 ADC cnt. measured on FEE card without detector
Energy calibration **Chapter 4.1**	LSB = 5 MeV 5 MeV / bit for CW shaper with nominal APD gain M=50	1 ADC bit = 0.97 mV
Sampling rate **Chapter 10**	Shaper Bandwidth < 0.5 MHz Nyquist frequency 1 MHz 1..20 MHz selectable over-sampling @ 10..20 MHz	Readout Bandwith *increases* with sampling rate Readout Strobe (L1) latency *decreases* with Sampling rate

Table 2 Electrical parameters PHOS FEE electronics

Component	Properties	remarks
Signal sampling latency for Altro strobe L1	f_S = 10 MHz L=1.4 us after interaction f_S = 9 MHz L=1.26 us f_S = 8 MHz L=1.12 us	Altro pre-sampling pipline: max. P=14 clocks. With P=14 and level-0 latency L0L =1.4 us, pedestal time is L0L-L.
Samples per event	Max 256 samples	512 available but due to special Altro selection for PHOS, data memory above 256 may contain errors
digitization buffer (MEB)	4 buffers 1024*40 bit or 8 buffers 512*40 bit	with special Altro selection for PHOS, 8 buffers are default
digitization ranges Chapter 4.1	high gain: 5MeV - 5.12 GeV low gain: 80MeV - 81.92 GeV	digital resolution (bit-value / 1024) < σ / E
FEE power consumtion Chapter 16.2	FEE (32 channel) card 5.2 Watt (add 2 Watt for 32 CSP)	112 FEE cards + 8 TRU PHOS module dissipation ~ 1 kWatt. (add 40m differential LV cable 300 W)
CSP power consumtion Chapter 1.4	+12 V - 4.2 mA -6 V - 2.2 mA	3584 CSP's generate 215 Watt heat in the cold volume
Readout partition	1 RCU and 1 DDL link (Tx, Rx) 2 GTL readout branches 14 FEE and 1 TRU readout branch 2 * 448 channels of 2*10 bit	

Table 2 Electrical parameters PHOS FEE electronics

Component	Properties	remarks
Supply voltages and currents **Chapter 16**	+13.5 V analog, 0.14A -7 V analog, 0.12A +6 V analog 0.32 A analog return 0.73 A digital return 0.45 A +3.3 V analog, 0.34 A +3.3 V digital, 0.31A +4.2 V digital, 0.14 A	LV daisy chain connector Phoenix TMSTBP 2,5/ 8-STF-5,08 +13.5 V-> 12 V Bias + CSP -7 V analog-> -6V shaper,CSP +6 V analog ->5V shaper, Bias +3.3 analog ->1V, 2.5V Altro +3.3 V digital ->2.5V FPGA, Altro, GTL +4.2 V digital ->3.3V Flash, USB, FPGA, Eprom
Fast OR signal shaping **Chapter 2.5**	Analog Sum of 2*2 crystals FWHM = 100 ns differential	8 way differential, terminated flat cable of 50 cm length, 150 OHM differential, Samtec FFSD-08--D-20.00-01-N Pulsewidth adapted for 4 samples @ 40 MHz in TRU max. pulse amplitude of 2.5 V corresponds 4*10 GeV
HV Bias input voltage **Chapter 2.3**	390.0 V +-0.2V 0.65 mA for 32 channels	each channel 20 uA. above 395 V protection starts shunting current
APD Bias regulation **Chapter 2.3**	10 bit between 200-390 V (~ 0.2 V per bit)	Regulation of 32 HV channels via 32 registers in Board controller, no HV readback

Table 3 Offline parameters of PHOS FEE electronics

Observable	value	Remarks
Energy resolution σ/E Chapter 4	a_{noise} = 13 +- 0.7 MeV $b_{stochastic}$= 0.0358 +- 0.002 (3.58 % $GeV^{0.5}$) c_{const}= 0.0112 +- 0.003 (1.12 %)	valid for 3*3 crystal cells See Chapter 4
Timing resolution (differential between channels) **Chapter 5**	Not yet available with particles With 2 ns blue LED pulser and 10 bit digitization, offline result for τ ~1... 2 ns @ 2GeV was achievd with M=50, 4 us CW shaper,10 MHz sampling rate	2 ns = worst case laboratory measurement with blue LED . Apart from shaping time choice on FEE card, the timing resolution can be improved by: • use both ADC's for effective 14 bits • exploit overclocking above 1 MHz • use of faster LED and pulser • determine TOF at rise time and not at peak time • improve sampling-clock stability
Pedestal **Chapter 3**	CW-shaper: 25 ADC counts[a] low Energy, 37 ADC counts high Energy	Measured with board revision V1.0
RMS nois, single channel **Chapter 6**	CW shaper 4 us peaking time RMS(pedestal)=0.62 ADC counts[a] =3.1 MeV	CW shaper APD gain M=50

a. 1 ADC count = 5 MeV for CW shaper

1 PHOS electronics in the cold zone

The electronics of the PHOS EM calorimeter is fully embedded inside the cold and warm enclosures of 5 distinct PHOS modules of 56 * 64 = 3584 crystals. Low-noise preamplifiers and APD diodes are attached to the PWO crystal ends and operated in the cold volume at a temperature of -25 C. The digitization, control and trigger electronics is fitted below the crystal matrix in a separate, warm volume. Figure 3 depicts the design details of a double strip unit,

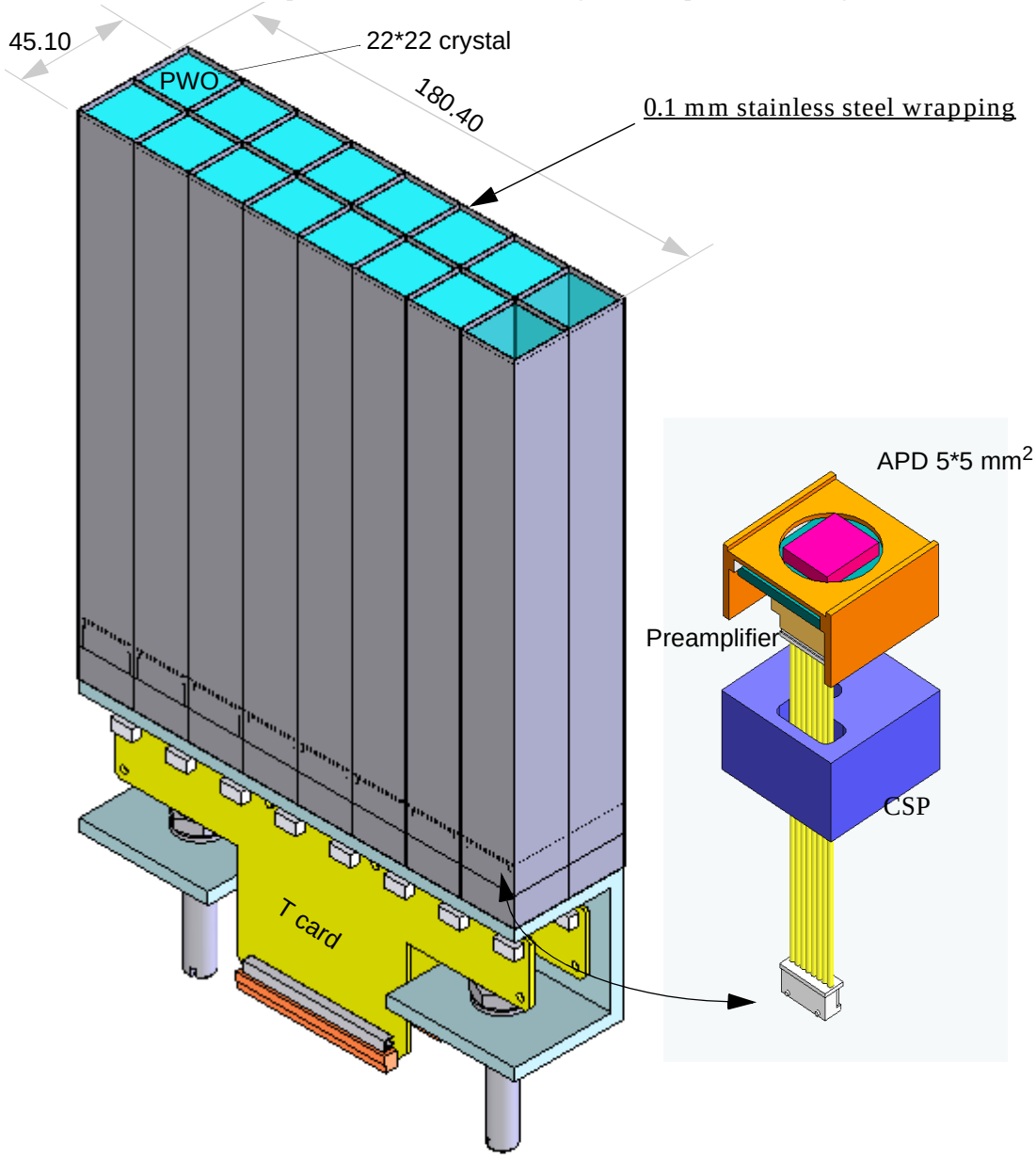


Figure 3 double strip unit consisting of 2*8 PWO crystals with APD/preamplifiers connected to T-cards

consisting of 2*8 PWO crystals.

Figure 4 is the photo of a single PWO crystal on which the APD / CSP combination is mounted.

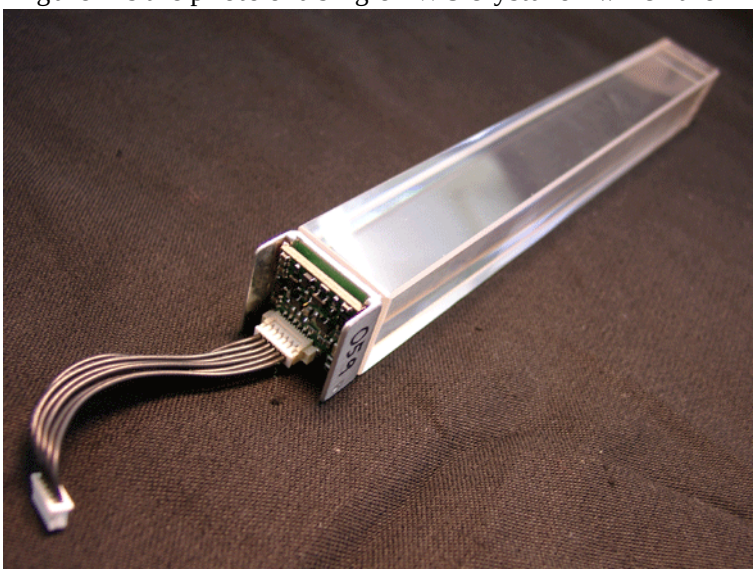


Figure 4 Photo of a single PWO crystal mounted with APD/CSP

The APD diode is glued to the Crystal on one side and soldered to the CSP on the other side. A 6-conductor cable provides both HV and LV connections to the CSP in addition to the analog signals for the FEE electronics. Figure 5 is a photo of a view into the crystal (like from an

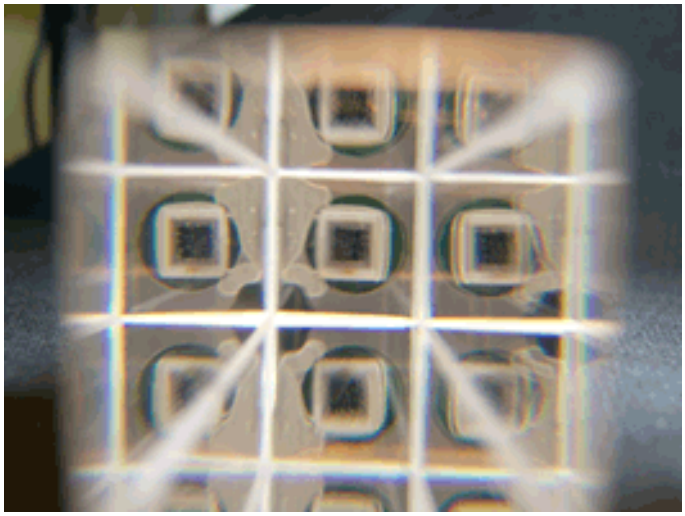


Figure 5 View of a central photon entering aPWO crystal, the single APD is mirrored n times.

incident photon). The single APD on the far side of the crystal is symmetrically reflected n times. The PWO crystals are mechanically mounted first in units of 8 crystals called *single strip units*. Since these are connected to the FEE cards in parallel rows of *double strip units* like depicted in Figure 3, fast analog OR's of 2*2 quadratic cells can be generated on the FEE cards.

One double strip unit (2*8 crystals) in the cold zone corresponds to one double flat-cable passing throught an isolation layer (see Figure 87) to the Front End Electronics (FEE) card. Two double strip units correspond to one FEE card for 32 crystals (2*16). Figure 6 is a photo of a

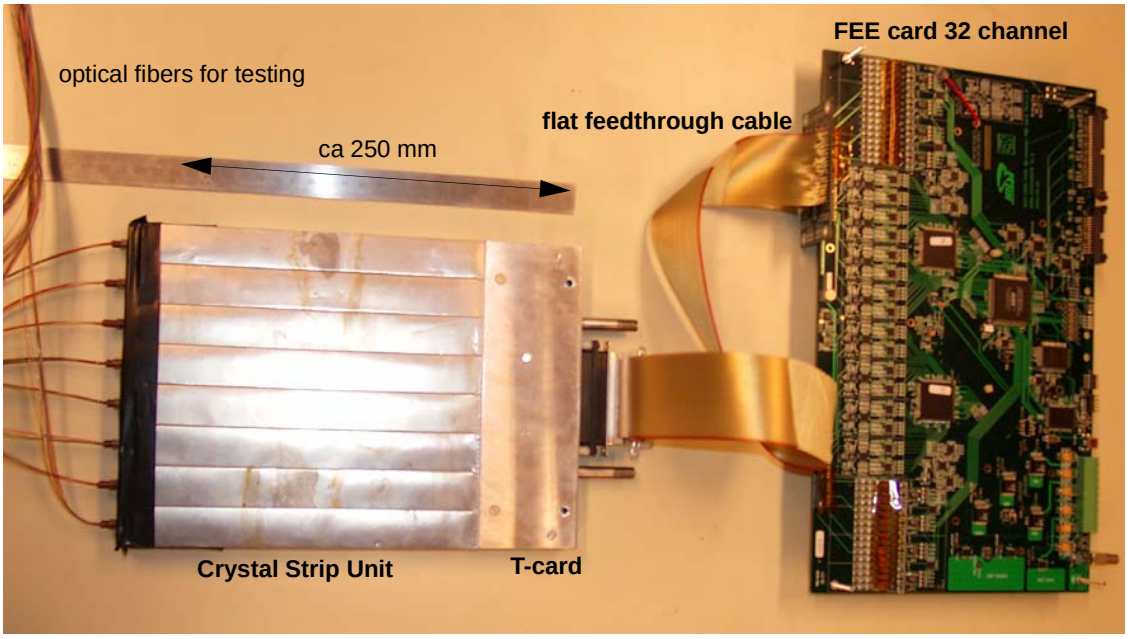


Figure 6 strip unit assembled with T-card and FEE card. (Optical fibers are

crystal strip unit with T-card and mounting screws, connected via flat cable to a FEE card.

1.1 P_bWO_4 crystals

As described in [1] the electromagnetic PHOS calorimeter is constructed from synthetically manufactured, inorganic $PbWO_4$ scintillator crystals which emit mainly two lines: 420 nm (blue) and 480 -520 nm (green) with decay times in the order of 10 ns. With a radiation lenth X_0 = 0.89 cm, PWO has a Moliere radius of 2.2 cm for 95% transverse electromagnetic shower distribution. The incident photon angle per crystal is smaller than +-13 degrees. Each crystal has a size of 22* 22 * 180 mm of which 180 mm (equivalent to ~20 X_0) was chosen as a compromise in price and absorption efficiency of electomagnetic showers, for optimal energy resolutions up to 10 GeV.

The PbWo4 crystals have the following properties: :

Table 4 $PbWO_4$ crystal properties (synthetic Apatity production >2004)

Density	8.28 g / cm^3	(compare with Pb 11.35)
Radiation lenght X_0	0.89 cm 7.37 g / cm^2	approx. conversion length via process e->2γ, or γ-> e^+ e^-
Moliere Radius R_M	2.2 cm	95 % of shower cone located in a cylinder with R_M
dE / dx per mip	13 MeV / cm	cosmic muons through 18 cm PWO leave 234 MeV.
interaction lenght	19.5 cm	
critical Energy E_c	8.5 MeV	Radiation region E> E_c
Decay time	5-10 ns	room temperature
Peak emission	420 (f) nm = 2.9 eV (blue) 480-520(s) nm =2.5 eV (green)	f =fast component, s=slow component
refractive index	2.16	along ζ axis
light output	10 - 12 MeV / MeV	improving per year
hygroscopy	no	
melting point	1123° C	

The average light yield for PWO crystals was under permanent improvement between competitors[1] and is obviously a function of crystal growing axis and annealing and doping. The manufacturing quality for PHOS crystals in Russia (Apatity) improved from 7 to 12 ph.e. / MeV from 2001- 2004. Since the light yield for PWO is a strong function of temperature and roughly a factor 2.5 higher at -25 ^{0}C than at 25 ^{0}C [Figure 7], it was decided to operate PHOS at -25 ^{0}C in order to have the same amount of photo-electrons per MEV as with two APD detectors at room temperature. .

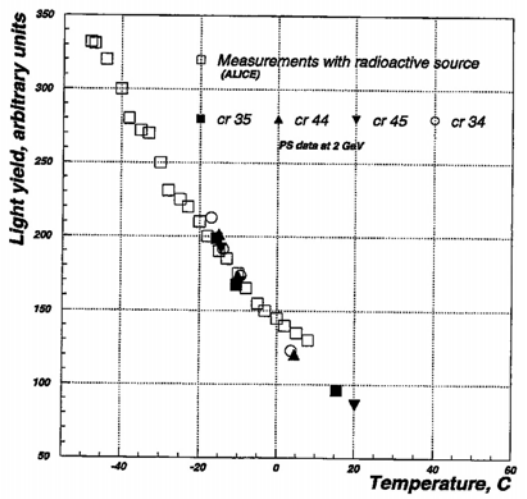


Figure 1.1: Light yield of $PbWO_4$ crystals vs. temperature.

Figure 7 Light yield dependence on temperature [1]

1.1.1 Electromagnetic showers in PbWO4

The energy of an electromagnetic particle is converted inside the dense PbWO4 crystals into electromagnetic cascades (showers), with successive separation into a.) electromagnetic pairs due to Bremsstrahung of electrons yielding photons, and b.) photon pair production into electrons and positrons. This shower process is described in lenght by the radiation length X_0, a property of the material, which is related to the mean free path of a photon, before it produces a pair by X_p=9/7 X_o The PHOS crystals represent 20 radiation lenght, hence the energy of an incident photon is split into a very large number photons and electrons with their energy reduced over 20 radiation lenght until the critical Energy E_c is reached and the ionizing processes (compton and photoeffect) pervail which produce the scintillation light (2.9 and 2.5 eV). The longitudinal EM shower maximum [4] is at

$$t_{max} = \ln\left(\frac{E_o}{E_c} \cdot \frac{1}{\ln 2}\right)$$

1. PWO manufacturers: a.) North Crystals Company, Apatity, Murmansk Region, Russia.(Alice PHOS 22 * 22 * 180 mm^3 b.) BCTP, Bogoroditsk, Russia (CMS Ecal 28.52 x 220 x 30.02 mm) c.) SICCAs, Shanghai Institute of Ceramics, Shanghai, China, (PrimEX 22 * 22 * 230)

The 95% containment is at t_{max} + 9.6 + 0.08Z i.e. for a primary photon with E_o=10 GeV, the shower maximum is at ca 7.4 radiation length (6 cm) and 95 % are ca 20 radiation length (18 cm). The leakage of energy below 10 GeV is hence less than 5 %.

1.1.2 Timing of PWO scintillation light

The PWO emission spectrum consists of a blue component with maximum at 420 nm and a green component with maximum at 500 nm. Ca. 5...10 ns after excitation, the luminescent intensity decreases rapidly by two orders of magintude. The decay can be described as superposition of several (4) exponential decay components of different amplitude and decay constant of which the fastest is 2-3 ns and accounts for 20-30% of the light yield. Globally, after 40 ns only a very small fraction of the initial luminescence is still observeable. The decay time is normally measured at room temperature, with lower temperature, the total luminescence decay time gets slower, ca. 20 ns per 25 Kelvin.

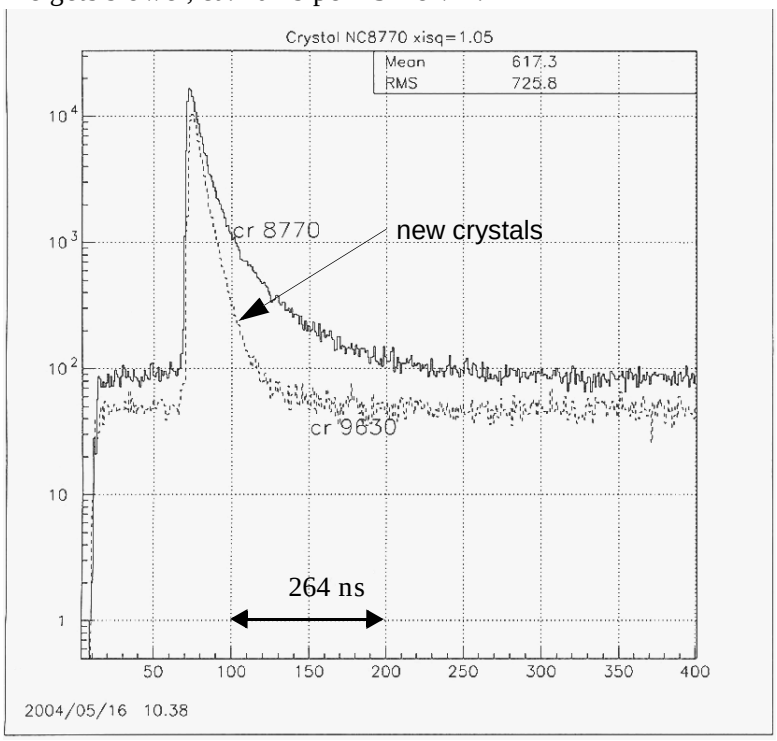


Figure 8 PWO decay kinematics of scintillation light luminance with new (9830) crystals at room temperature The decay time has been improved and most light is produced within 25-30 ns after excitation (logarithmic scale) At room temperature, the crystal gets ~ 30 % slower. (Curteousy M.Ippolitov , Kurchatov)

For the APD charge integration by the CSP this means that an idealized output step funcion for a delta(t) charge input function is only an approximation and would have to be replaced by a charge generation process consisting of several slopes. The observable effect is that the CSP risetime flattens towards the maximum and the peaking time of the semi-gaussian output pulse is delayed by the amount of the risetime delay of the input signal.

This is an indication that the rising slope of the shaper's semi-gaussian output carries the best time information of the initial charge generation process.

1.1.3 Synthetic growth of PWO crystals

The natural form of synthetically produced PbWO4 cristals is the natural Stolzite, a crystal of quadratic and bi-pyramidal structure with natural colors: yellow, red, brown. The other natural form of PbWO4 is Raspite, however it's different crystal structure turns into Stolzite when heated above 400 C. The industrial production of Apatity synthetic PWO crystals for PHOS is based on the Czochraski method: Two metallic Oxides PbO and WO3, powders of very high purity, are mixed in proportion 1:1 and heated to the melting point i.e above 1123 degree C. An original crystal seed is then inserted and rotated at ca. 15 rotations / minute and pulled out vertically at 5mm / hour. After ca. 60 ..75 hours, a round crystal of ca 25 cm length is grown (see Figure 9). In a subsequent annealing process, the crystals are re-heated in specifically chosen atmospheres in which transparency and colors are optimized.

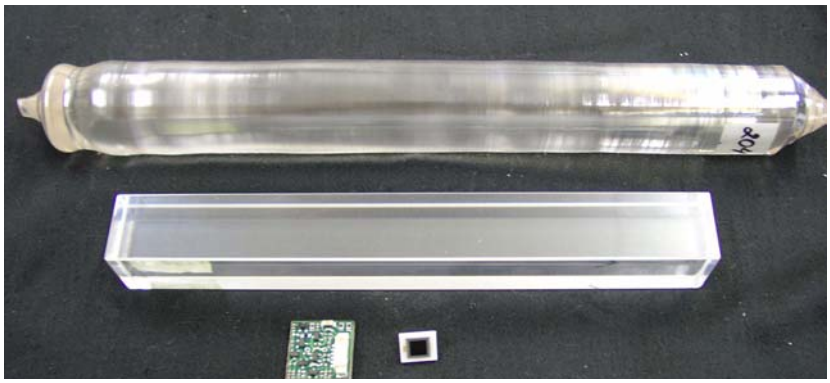


Figure 9 PWO crystals:
Top: synthetic raw crystal
Middle: rectangular cutout crystal after polishment
Bottom: comparative size of APD and preamplifier.

1.1.4 PWO light yield with APD diode

The number of electrons produced by an APD by a 1MeV electromagnetic particle in the PWO crystal at temperature 25°C at APD gain M=1 can be estimated by comparing with the light yield mesaurements performed using an EMI 9814b[1] PMT photomultiplier [1] covering the PWO full exit window. For average crystals with LY =10, one obtains, by putting detector surfaces and quantum efficiencies in relation:

$$N_{APD} = N_{PMT} \times (S_{APD}/S_{PMT}) \times (E_{APD}/E_{PMT})$$

$$=10\times (25/484) \times (0.7/0.25) = \underline{1.45e/MeV} \quad (LY=10, +25\ ^{o}C)$$

1. http://www.electron-tubes.co.uk/menu.html

Where:

- N_{APD} - quantity of electrons in APD;
- N_{PMT} - quantity of electrons in PMT;
- S_{APD} - area of APD S8148 (5 * 5 mm^2)
- $S_{PMT} = S_{PWO}$ area of PMT covered by the PWO window 22 *22 mm^2
- E_{APD} - quantum efficiency S8148 @ λ=420 nm (M=1) = 70 %
- E_{PMT} - quantum efficiency EMI 9814b @ λ= 420 nm = 25 %
-

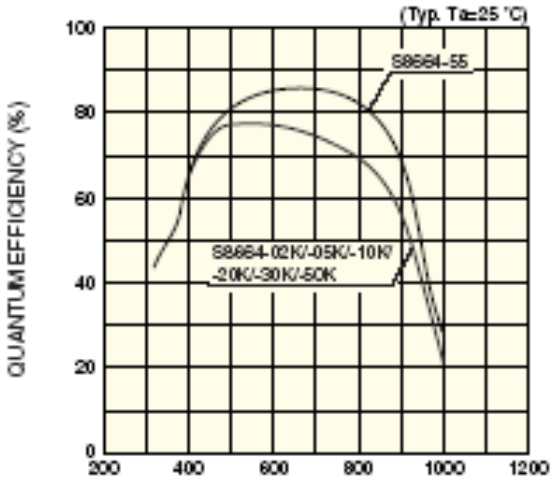


Figure 10 Quantum efficiency of APD in dependence of wavelenght. The Hamamatsu APD S8148 is equivalent to S8664-55. For 420 nm, the quantum efficiency is 70 %

At -25°C the PWO light yield increases by a factor between 2.5 to 3. (see Figure 7) We interpolate the temperature factor here for an estimation to 2.75.

$$N_{APD}(-25°C, M=1) / MeV = 2.75 \times N_{APD}(+25°C, M=1) \sim \mathbf{4\ e^-/MeV}$$

Equation 1 Photoelectrons per MeV for a crystal with LY=10 @ -25 ^oC

With the above, the CSP preamplifier voltage step for 1 MeV photons with APD gain M and feedback capacitor C_f=1.2pf is at -25 C is equal to Q / C_f: hence with e =1.6 10^{-19} Coulomb

$$U_{csp}/(MeV) = M \cdot N_{apd} \cdot e/C_f = M \cdot 0.533 \cdot \mu V$$

Equation 2 CSP output Voltage per MeV

By including the CSP's intrinsic ENC noise of 520 electrons for a detector capacitance of 100 pF, this becomes

$$U_{csp} = \lfloor M \cdot 4/(MeV) + 520 \rfloor \cdot e/C_f = \lfloor 0.533 \cdot M/MeV + 69 \rfloor \mu V$$

Equation 3 CSP output Voltage per MeV including ENC

The CSP output Voltage per MeV as function of the APD gain is shown graphically in Figure 11

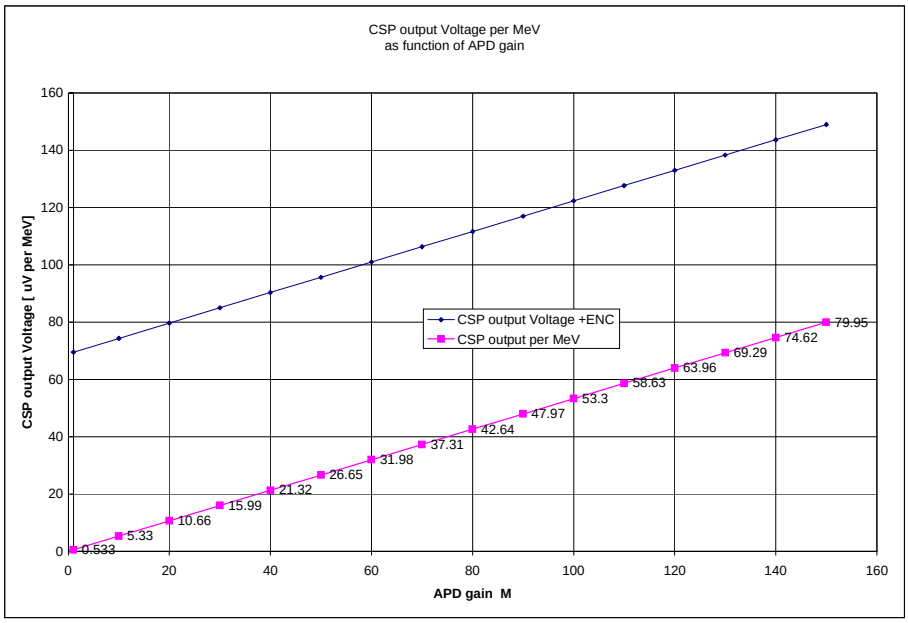


Figure 11 CSP output Voltage as function of APD gain in uVolt per MeV for Crystals with a nominal Light Yield of 10.

The CSP's intrinsic ENC is a constant offset (69 uV). For shapers designed for M=50, the relevant figure is 26.7 uV / MeV

1.2 FEE/CSP signals with LED pulser

A blue Kingbright L-7104PBC LED, driven by a 2 ns risetime Philips pulser was operated in front of a crystal / APDpair at an ambient temperature of -25 Volt[1], in order to emulate the situation of scintillating (blue) light.

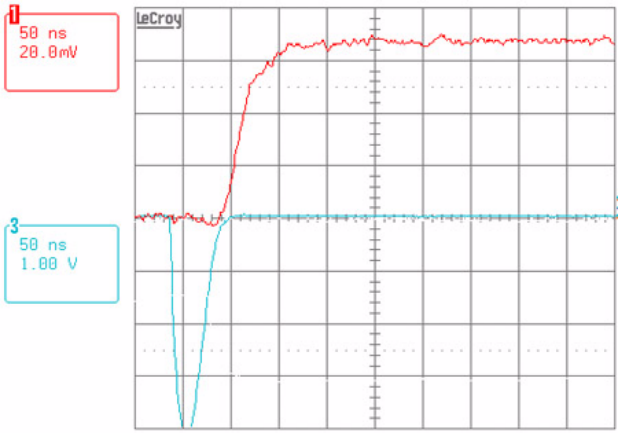


Figure 12 CSP output relative to a 2 GeV equivalent LED pulse. Top: CSP voltrage corresponding to 0.833 V /pC Bottom: Pulser output for driving blue LED.

1. deep freezer compartment of a standard refrigerator

Figure 12 shows the measured CSP output step function for a blue LED for an equivalent of ca 2 GeV. The 2 GeV equivalence is based on the testbeam measurements with the **same FEE card channels** where 2 GeV electrons had their peak amplitude at ADC channel # 400 (the APD gain had been set such that 2 GeV electrons peak at ACD channel 400, this corresponds for the 14 bit dynamic range to a least significant ADC bit of 5 MeV). Based on this equivalence, the blue LED pulser light intensity was tuned to the same peak amplitude of ca 400 ADC counts with a bias Voltage setting close to the testbeam setting. With this, the CSP output voltage of U_{csp} = 65 mVolt corresponds to an Energy 2.1 GeV (effective 425 ADC counts of Figure 15).

The a priory unknown APD gain value of the testbeam can be determined: With 65mV / 2.1 GeV follows 31 uV / MeV. With Equation 3 the APD gain was ~ M=58 , a value which is also compatible to the nominal gain specified by the manufacturer (see Figure 16 for a bias voltage of 330 Volt, slightly extrapolated from -20 C) Figure 13 shows that the gain between 320 and 350 Volt varies by a factor 2.

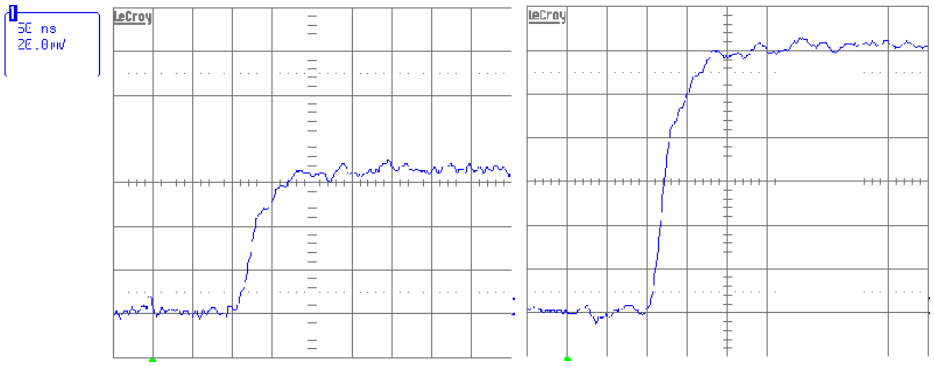


Figure 13 CSP output for same APD pulse withdifferent bias Voltages
Left U_{bias}= 320 Volt
Right U_{bias}= 350 Volt
The agin difference is amost 100 %

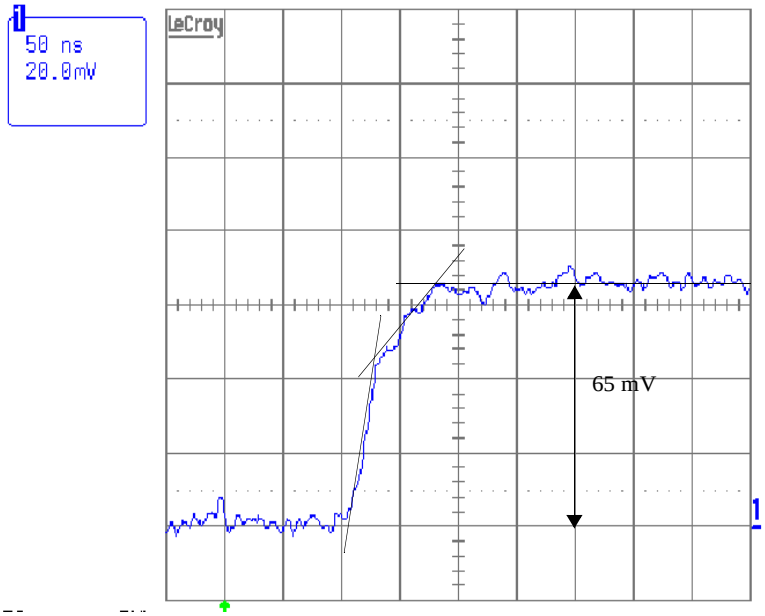


Figure 14 CSP output for blue LED with 2.1 GeV equivalent light .

The CSP voltage output for a blue LED puser and U_{bias}=320 Volt is shown in Figure 14. The integrated voltage of 65 mV corresponds with Equation 3 to an APD gain of M ~ 58. The CSP risetime consists of two parts: LED luminescence risetime (~ 25 ns) and falltime (~ 50 ns)

Note: The Luminescence decay time with real EM particles and new PWO crystals is faster (Figure 8) compared with the above LED pulser measurement, hence the secondary slope is steeper. Timing measurements with LED's (and particles) should only use the information produced by the initial risetime.

The measured CW shaper output, produced by the shaper's "ballistic effect", i.e. a semi-gaussian amplitude which is strictly proportional to the CSP step voltage, is shown in Figure 15. The low energy channel is shown with a vertical scale of 5 MeV / bit. With 25 ADC counts pedestal, the peak amplitude corresponds to 2.1 GeV. With 10 MSamples/s the peaking time is ca. 4 us

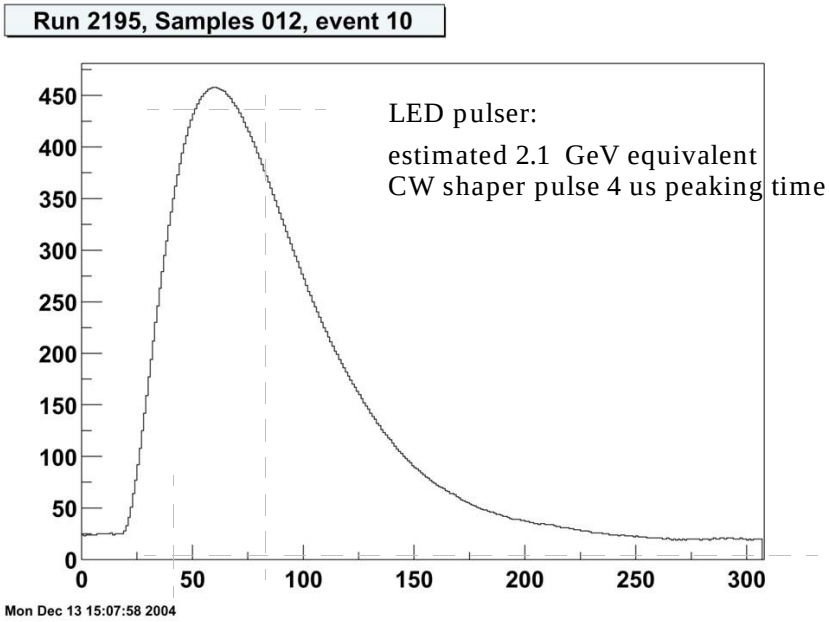


Figure 15 Semi-gaussion C/W shaper output of above CSP signal.

1.3 Avalanche Photo Diode (APD)

Avalanche Photo Diodes cannot be used as single photon detectors, however have a very high quantum efficiency and a gain between 10 and 100 defined by the reverse bias voltage (order of 300-400 Volt). APD's consist of a reverse-biased p-n layer in which a high internal field provides avalanche multiplication of carriers. The p side is attached to another p++ doped layer for gamma conversion, covered by a very thin Si3 Ni4 transparent window for light. The APD response for light pulses is about 10 ns

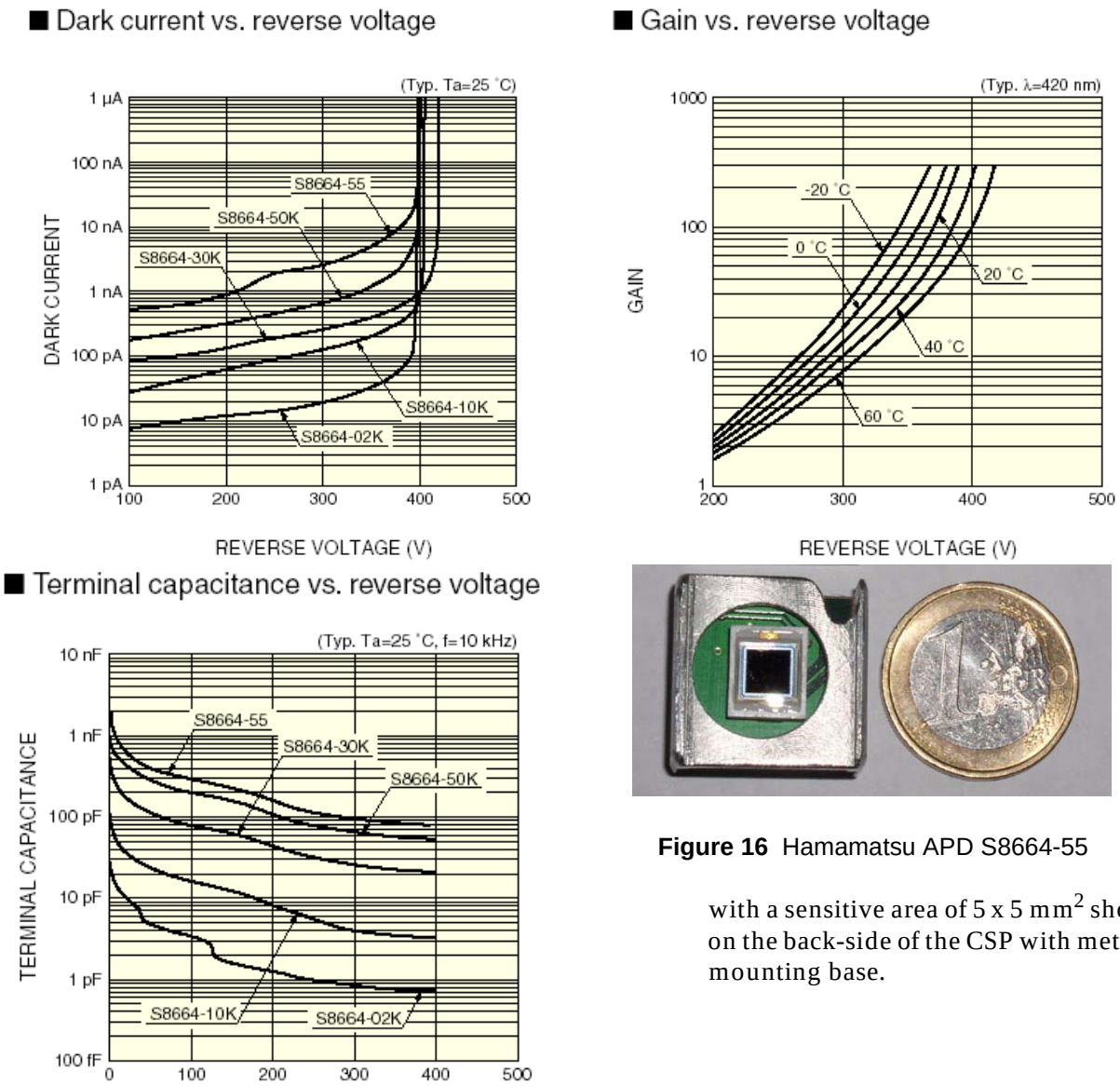


Figure 16 Hamamatsu APD S8664-55

with a sensitive area of 5 x 5 mm^2 shown on the back-side of the CSP with metallic mounting base.

Contrary to the initial choice of PIN diodes for PHOS [1], APDs were chosen since PIN diodes show a strong sensitivity for the punch-through of charged particles like muons (nuclear counter), whilst this effect is quasi neglegible for APD's [12] due to their comparatively much thinner depletion layer (6 um, compared to 280 um for a pin diode). The chosen Hamamatsu

S8664-55 (S8148) is a Si APD diode in ceramic package with sensitive area of 5*5 mm^2. At -20 C the nominal gain M= 50[1] corresponds to a reverse bias Voltage of 320 Volt, with a terminal capacitance < 90 pF (see Figure 16) The dark current is a strong exponential function of temperature, hence the data sheet value of 4 nA at +25 C can be extrapolated to a value in the order of 1nA for -25 C

1. For operation at -25 C we extrapolate to M=55 for 320 V

The APD factory gains are however not applicable at -25 ^{0}C for PHOS, considerable spreads in gain have been measured at the PHOS operating temperature (Figure 17).

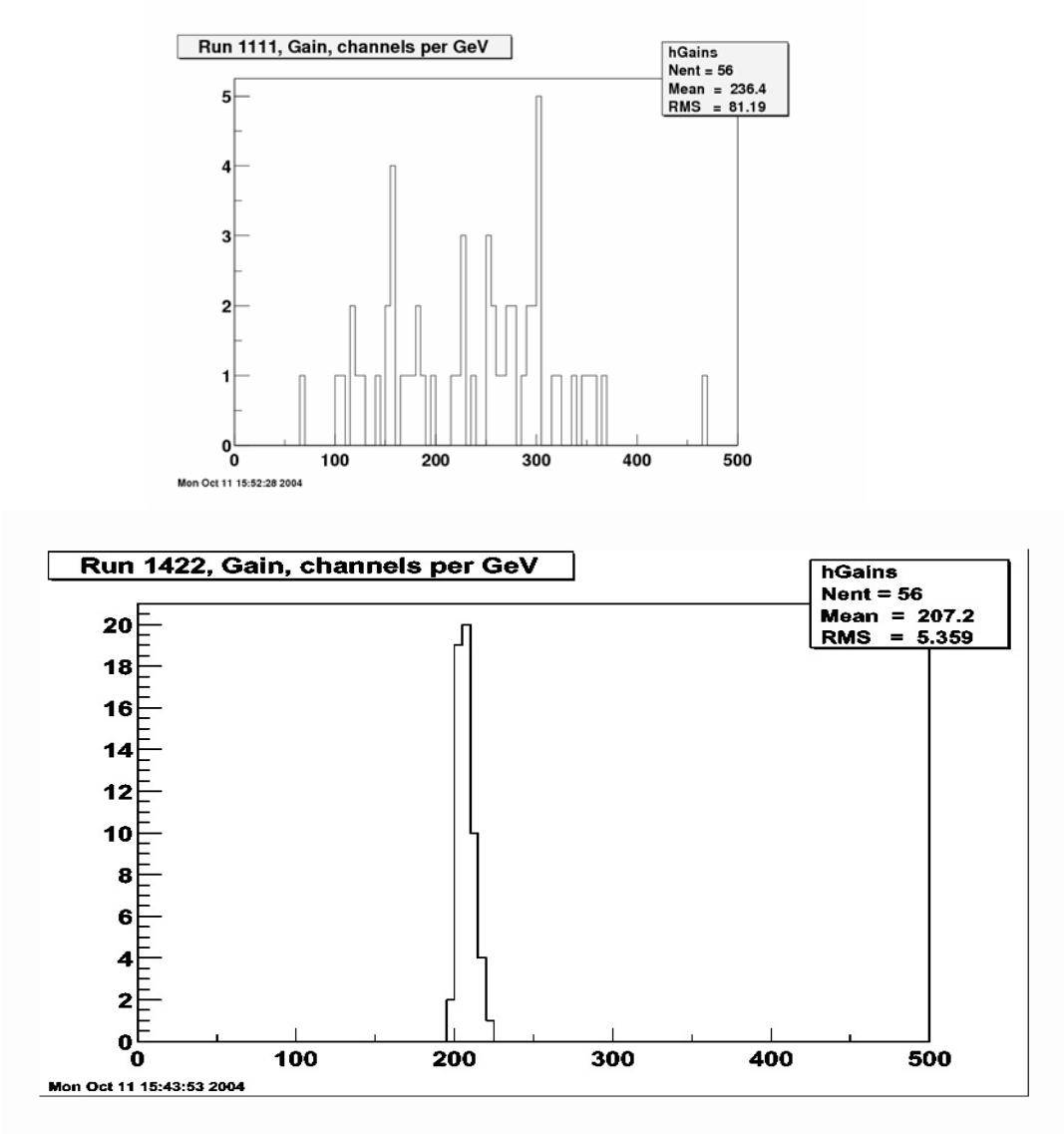


Figure 17 APD gain hardware calibration of 58 channels with 2 GeV electrons
TOP: uncalibrated, very large spread of relative gain. BOTTOM: calibrated to 5.3% via hardware APD bias control on FEE card (2004 october test beam)

For the hardware gain calibration, individually programmable reverse bias voltages are generated on the FEE for *each* APD in a range 200...390 V. The Voltage settings are programmable via a 10 bit DAC under control of the PCM controller (see Chapt 8 .). The result of APD gain calibration with the FEE-card-resident Bias control logic is shown in the bottom of Figure 17. (In this example a calibration level of only 5% was reached due to unavailability of fast online calibration tools during the 2004 october testbeam.)

1.3.1 APD gain choice for PHOS

A compromise between a high signal gain, noise and signal stability is required. With a practical APD gain range between 10 and 200, we have chosen a nominal value M=50 in combination with the CW shaper gain. This choice has a 15 % lower excess noise than M=100 which has a direct effect on the stoachstic term of the energy resolution. More importantly, a low gain keeps the gain dependencies on temperature and voltage low (see Table 5). These dependencies have an important impact on the constant term of the energy resolution, in particular the programmable gain inter-calibration is limited if the gain setting is too high: With a gain dependence of ~3.2 % per Volt at APD gain M=50, the bias logic can achieve with 0.2 Volt / bit an intercalibration precision of 0.6 %. Shown in Figure 18 is the percentual gain dependence on bias voltage as measured by CMS for room temperature: a factor 2 in APD gain increases the dependency by a factor 2. i.e with gain M=100, the gain dependence is 6.6% hence the APD intercalibration precision would be 1.3 % per set bit.

In view of the large numbers of crystals, fast online calibration tools are needed for a complete intercalibration via Bias control hardware of the FEE.

.. The major APD characteristics for PHOS are summarized in Table 5.

Table 5 APD parameters S-8664-55

M=50 T=- 25 C parameters	Value	Comment
active area	25 mm^2	
terminal capacitance (Figure 16)	90 pF	for detector capacitance add 10 pF for FET input
Dark current (Figure 16)	< 1nA	estimated from 3 nA @ +20 C
Quantum Efficiency (Figure 10)	70 %	M=1 and 420 nm
gain dependence on bias voltage 1 / M * dM / dV (M=50)	3.3 % per Volt room temperature	M=50
gain dependence on Temperature 1 / M* dM / dT (M=50)	-2.2 % per degree room temperature	M=50

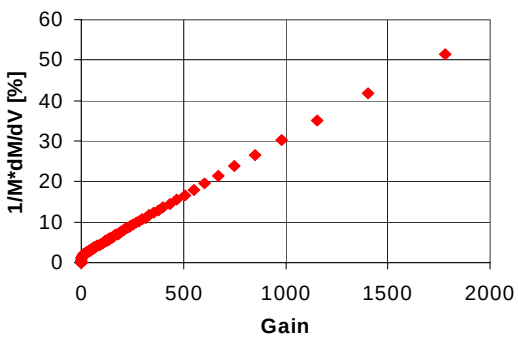


Figure 18 Gain-Voltage coefficient of CMS

1.4 Charge Sensitive Preamplifiers (CSP)

The charge sensitive preamplifier CSP [11] produces an output voltage step which is proportional to the charge Q produced by the APD on its input capacitor. The voltage step U_{out} is inversely proportional to the feedback capacitor C_f. Figure 19 shows the principle:

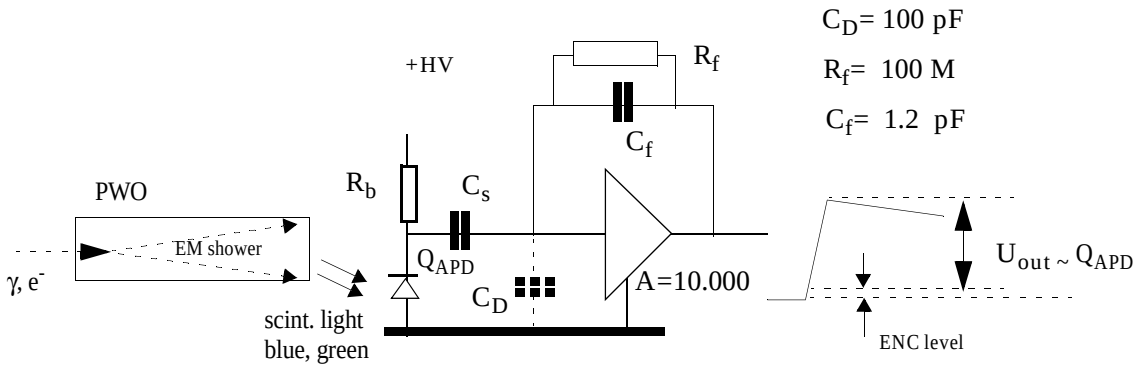


Figure 19 Charge Sensitive Preamplifier (CSP) principle

the input charge Q_{APD} isgiven by the number of electrons on the detector capacitor C_D, produced by scintillation light in the APD sensitive area (see Equation 1) and multiplied by the APD amplification gain M. The APD is reverse biased to 320..350 Volt via a very high resistance R_b. The high voltage is decoupled via C_s from the input of the pre-amplifier. The charge Q_{APD} ,due to the high gain A of the amplifier, is effectively charged on the feedback capacitor C_f. The input of the amplifier is however virtually at ground potential, therefore the Voltage at the output of the amplifier is given the charge on C_f. hence:

$$V_{out} = \frac{Q_{APD}}{C_f}$$

The charge Q_{APD} produces a voltage step V_{out}. like shown in Figure 12.

In order to be ready for a next measurement after about 5 us (200 Hz maximum channel rate assumed), a discharge resistor R_f is used in parallel with C_f and dimensioned to discharge the capacitor with a time constant of 1 us. This auto-dischcharge method has as side-effect that the CSP signal is subject to an operator which needs to be cancelled by the shaper (see Equation 16 of chapter 7) in order to cancel baseline movement for every signal.

The input stage is a J-FET transistor (2SK932) . For the noise calculation, the parallel noise

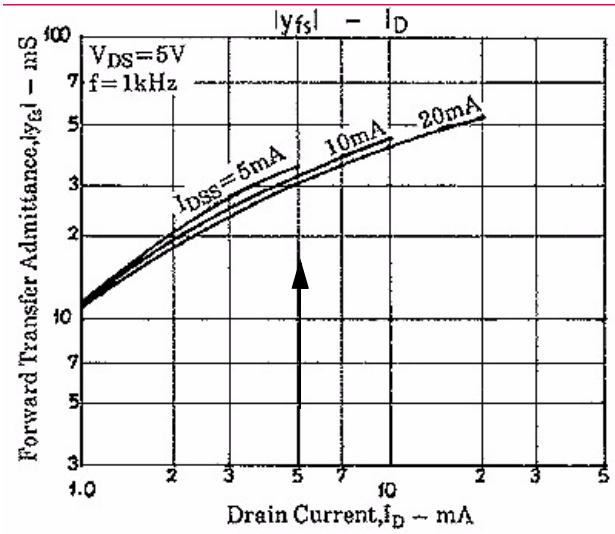


Figure 20 Forward admittance of the 2SK932 input stage J-FET.

equivalent of the J-FET can be estimated from its forward admittance curve of Figure 20.

The Kurchatov/Bergen design of the CSP preamplifier was tuned for amplitude independent rise-time as shown in Figure 21.

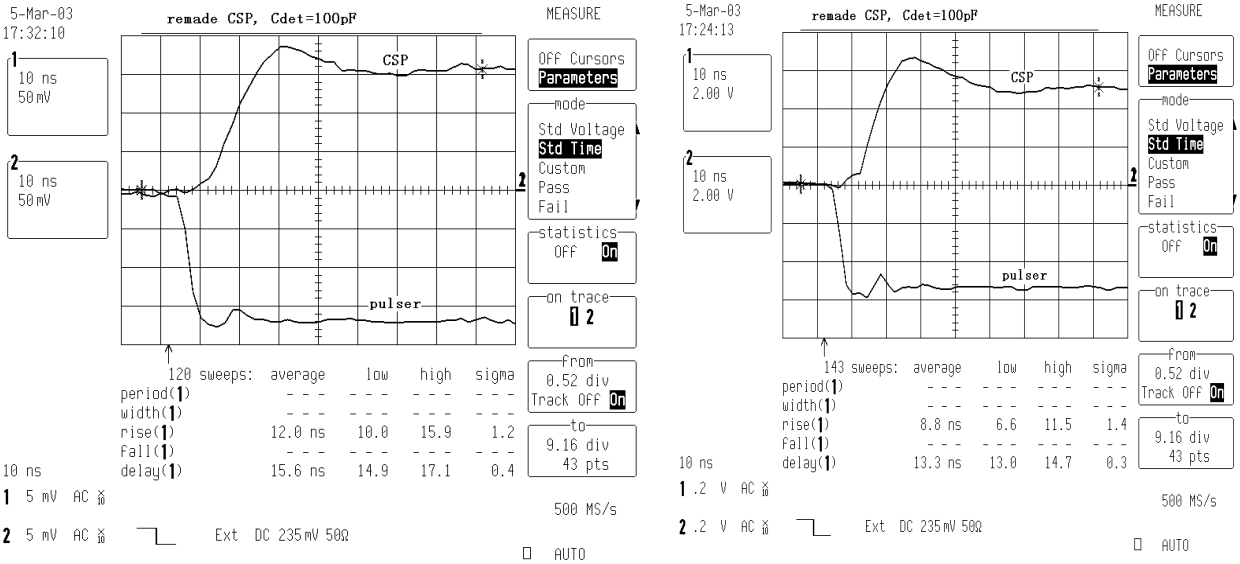


Figure 21 Tuned CSP for risetime 9...13 ns over dynamic range (max 5 Volt) with 4 ns input signal (from [14])

The CSP preamplifier dissipates ca. 60 mWatt, hence the total heat dissipation of all 3584 CSP's inside the cold volume of a PHOS module amounts to 215 Watt

C5 only
for test

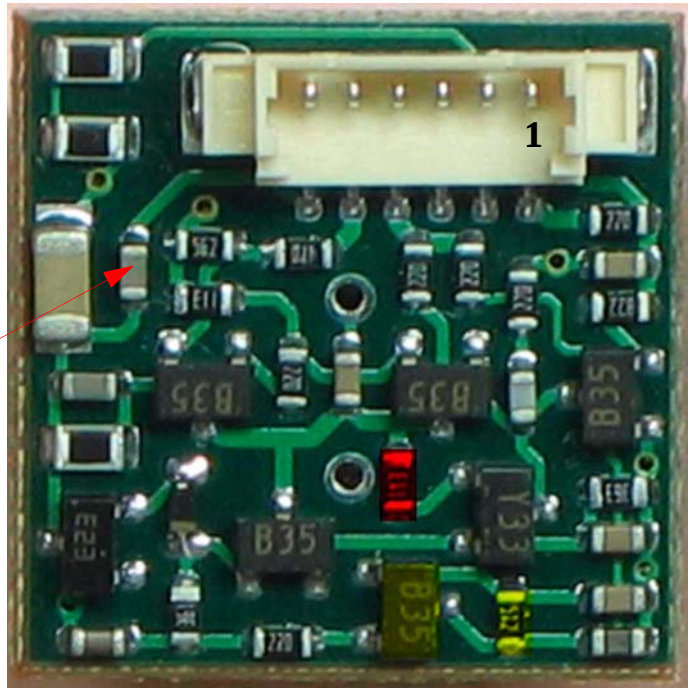


Figure 22

Photo of CSP preamplifier with 6 pin Molex connector. The test capactitor C5 is only to be mounted for testing.

Pinout Molex 53047

1..... -6 V, 2.2 mA

2..... HV Bias

3..... Gnd

4..... +12 V, 4.2 mA

5..... CSP-Out

6..... (Test in)

Figure 23 shows a CSP mounted together with a PWO crystal. The APD, soldered to the CSP

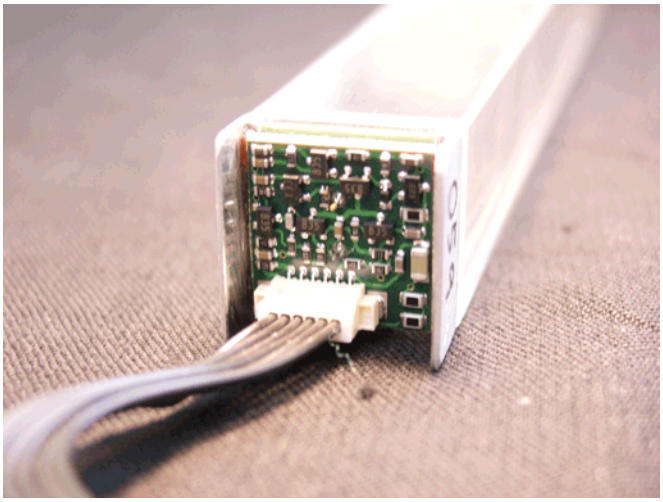


Figure 23 Preamplifier and APD attached to PWO crystal

backside, is glued to the crystal.

The parameters of the Bergen / Kurchatov CSP, tuned for equal risetime (9.. 13 ns) over the full dynamic range are:

- sensitivity = 0.833V / pC or 0.133 uV / e-
- open loop gain 10000
- feedback capacitor effective C_f=1.2 pF
- Output Voltage for APD gain M=50: 26.7 uV per MeV + 69 uV(ENC) (see Figure 11)
- rise time 15 - 20 ns over full range (see Figure 21)
- discharge time constant: nominally 100 us via 100 MOhm resistor
- "ENC = 200 e + 3.2 e / pF * C_{in}(pF)
- "DC output level = -0.5V
- Full swing over energy range: 2.4 Volt for CW shaper, 5 Volt for K shaper
- "power = 12 V (4.2mA), -6V (2.2mA)
- "power dissipation = 64 mW
- power dissipation of all CSP's in 1 Module = 230 Watt

2 FEE electronics in the warm zone

The overview block diagram of the PHOS FEE electronics, including CSP preamplifiers, TRU trigger unit and RCU Readout Control Unit is shown in Figure 24.

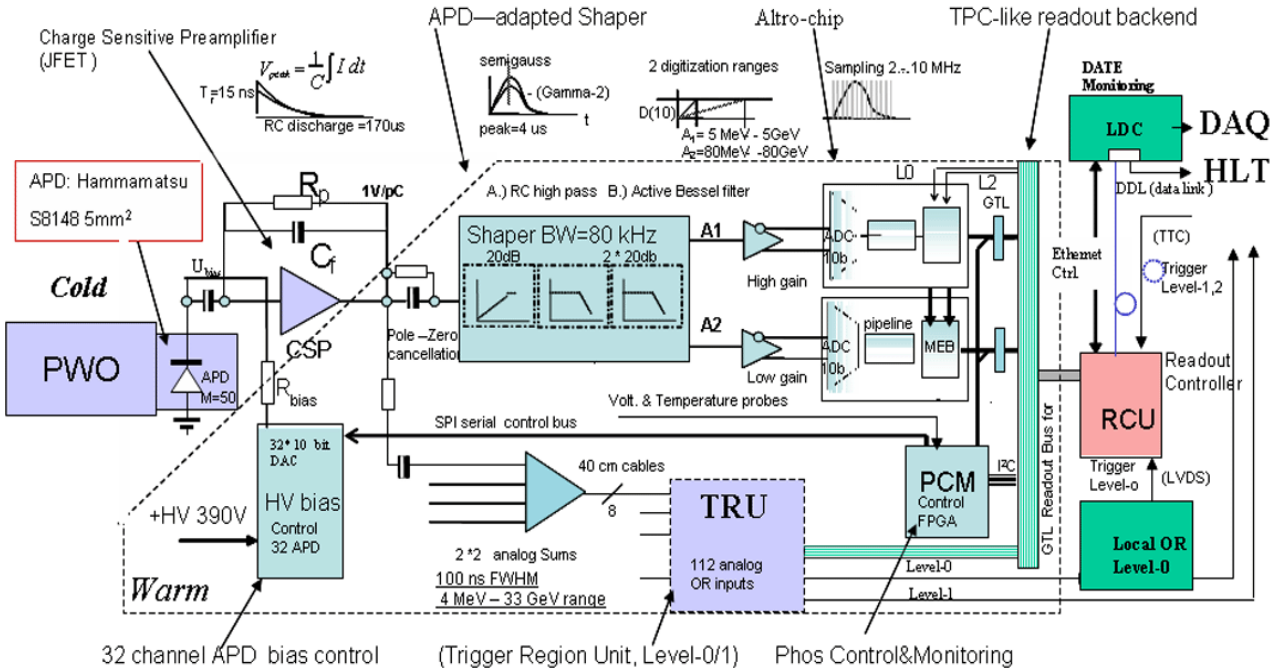


Figure 24 Global overview over all PHOS electronics. FEE electronics is within the dotted area (warm).

The APD and Charge Sensitive Preamplifier (see Chapter 1) are situated at the crystal ends in the cold zone. The output of the CSP is a voltage step proporional to the input APD charge with ca 15 ns risetime and ca. 100 us discharge. The gain of <u>each</u> APD diode is regulated to very high precision by programmable high voltage controllers on the FEE card. The CSP signal is passed to a shaper which produces a semi-gaussian output pulse, represented analytically by a Gamma-2 function. The shaper's second order cutoff characteristics of -40dB provides signal over noise separation, and corresponds with 80 kHz bandpass to a semi-gaussian peaking time of 4 us of the semi-gaussian output pulse. The 16/1 gain ratio of the high/low gain shapers corrsponds to two ADC ranges: 5 MeV..5GeV and 80 MeV .. 80 GeV, each of which is digitized by a 10 bit ADC with sampling frequencies selectable between 1 and 20 MHz. The digitizers are Altro-16 chips [3] with built-in zero-suppression and pedestal memory and in particular with integrated Multi-event buffers for pipelined event storage under control of external L1 and L2 timing signals. The common GTL+ readout bus of the ADC's is mastered by an external Readout Control Unit (RCU) which reads, under timing signals of the TTC network, events from the Multi-Event Buffers (MEB). Whenever a level-2 trigger is received by the RCU, it transfers data in an event-coherent way from all MEB buffers of all buffers to a local event buffer in the RCU[1]. From here, PHOS event-data are sent via the 200 Mbit/s optical DDL to the Local Data Concentrator (LDC). The RCU also masters a custom serial bus protocol, (similar to I2C) for control and configuration of the FEE electronics. For this purpose, a programmable

Board Controller (BC with PCM logic) on the FEE electronics cards can be addressed like I2C slaves, providing access to a number of memory-mapped control and status registers. These allow for voltage and temperature monitoring or serve as HV Bias settings of the 32 APD gain control channels. The PCM transmits the settings of the HV Bias via an onboard serial bus (SPI) to the precsion HV bias control.

Analog sums with fast shaping time of ca 100 ns are created for each 2*2 crystal quadlet. These signals are generated on the FEE and transmitted via short cables to the Trigger Region Unit (TRU) where they get digitized and processed. Also the TRU is mastered by the RCU using the same GTL readout bus as the FEE cards. Temperature and current monitoring as well as localized shutdown features allow that in case of FEE board problems, individual cards can be disabled without damage or without affecting others. For local interventions, the FEE electronics cards are also equipped with a processor-based USB port, providing diagnostic access to all data and status registers.

1. the new RCU allows for sparse data scan, i.e it will read out only those MEB buffesr with significant data.

2.1 Front End Electronics card FEEC

A 32 channel FEE card (Figure 25) was designed in collaboration between CERN and HUST University of Wuhan as a 10 layer board. It contains 32 dual-gain shapers, four Altro-ADC's [3], PHOS Monitoring and Control firmware (PCM), eight analog OR's and 32 High Voltage

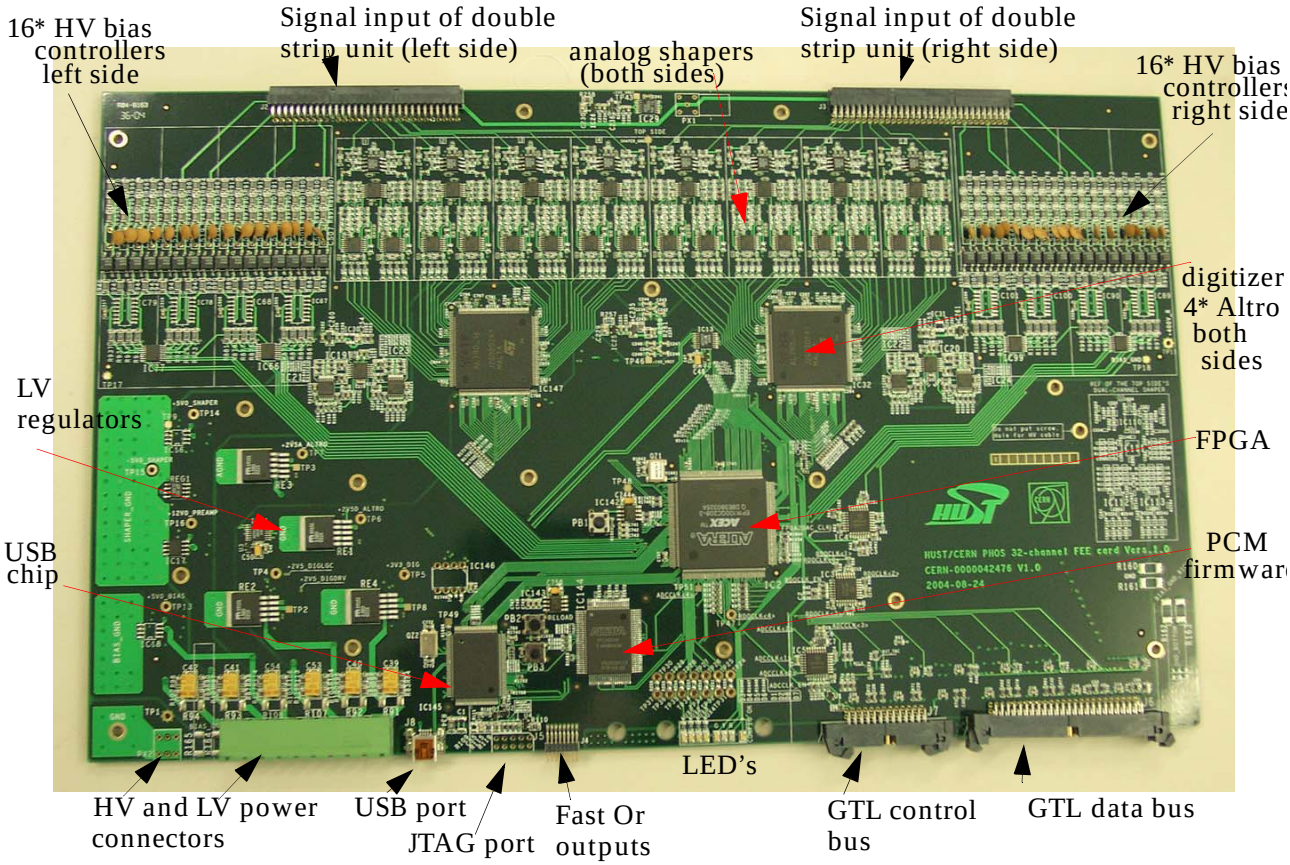


Figure 25 PHOS 32 channel FEE card HUST/CERN version 1.0

bias controllers.

The card dimensions (210 * 359 mm^2) and connectivity correspond to the geometrical requirements inside the PHOS Calorimeter. The following peripheral connectors are available (see Appendix 2):

- LV connector Phoenix `MSTB 2,5/ 8-GF-5,08`: a 6-way power connector with 4 analog and 2 digital supply voltages for the LV voltage regulator section. Corresponding daisy chain cable connector: Phoenix TMSTBP 2,5/ 8-STF-5,08
- HV connector: dual LEMO connector (Lemo EPY.00.250. NTN) for daisy chaning of the input High Voltage (390.0 V) for the 32-fold Bias controller.
- Mini-USB connector for service, diagnostics and firmware upgrade (Mini-USB Lumberg `2439-2301`)
- JTAG connector for PROM-loading (10 pin / 2-row standard 2.54 mm)
- Fast OR output for Trigger Unit, 8 * differential (8 pin / 2-row standard, 1.0 mm) Samtec `FTSH-108-01-L-DH-A` `corresponding to a 16 wire flat cable of 50 cm lenght, Samtec` FFSD-08-D-20.00-01-N
- GTL control bus (26 pin Samtec EHT-113-01-S-D-RA) and GTL data bus (50 pin EHT-125-01-S-D-RA)
- Signal input: left and right frontend connectors (LV, HV and signals) 60 pin Samtec LS2-1-30-01-S-D-RA1

The 14 bit dynamic range (5 MeV - to 80 GeV) is implemented as 2 overlapping gain channels, each digitized by a 10 bit ADC. With a gain ratio 16 / 1 = 2**4, the dynamic range is 2**(10+4) = 14 bit.

The analogue part of the FEE cards consists of two banks of 32 semi-gaussian shapers with two implementation options: CERN / Wuhan (C / W) and Kurchatov (K).(see chapters and 2.2.1 2.2.2)

The shaper logic is repeated on the PCB as dual-channel layout macro, on which either the CW or the K shaper option can be mounted (Figure 26) .

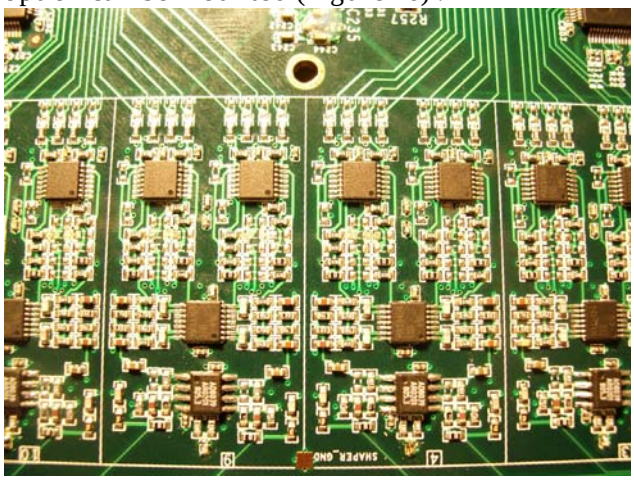


Figure 26 Photo of analog shaper macros on the FEE cards, each can be quipped as either CW or K shaper (shown here CW shaper)

The digital part of the FEE card consists of 2 banks of 32 ADC's of 10 bit with selectable sampling rates between 1 and 20 MHz. The ADC's are implemented as four Altro-16 chips [3] with integrated multi-event-buffers, zero suppression, pedestal memory and processing chain (see Chapter 9.1 .) The choice of using the Altro allows the use of the TPC readout backend via the RCU master and PCM slave logic.The FEE card contains 32 remotely programmable high-voltage controllers of 0.2 Volt / bit for the APD bias voltages.These are implemented in 2 blocks of 16 HV controllers at the left and right sides of the front-end connector.

Figure 27 shows the four superimposed routing layers of the PHOS FEE card.The shaper

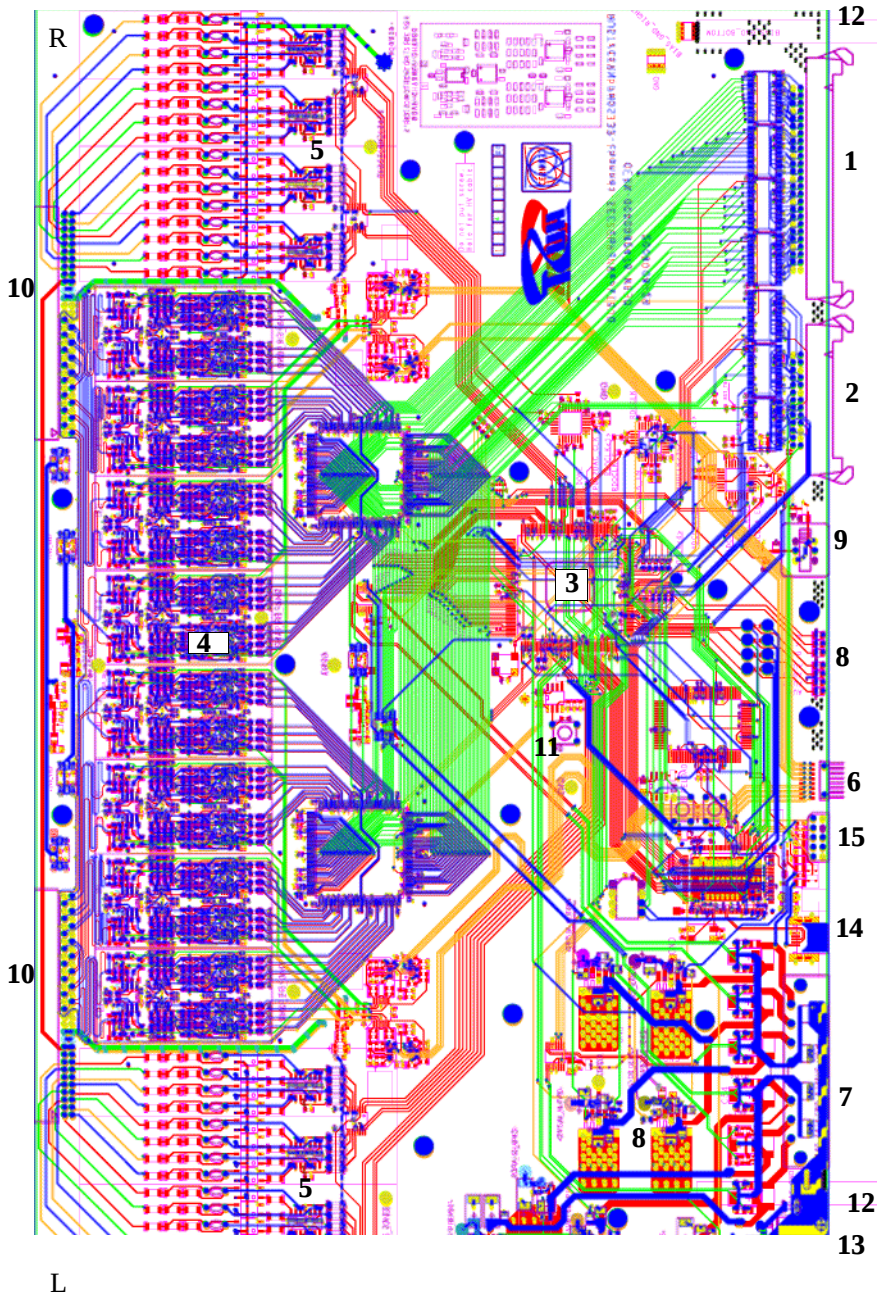


Figure 27 Superimposed 4 Routing layers of the PHOS FEE card (Version 1.1)

1. GTLdata bus connector
2.GTL control bus connector
3.PMC FPGA
4.Shaper macro
5.HV APD bias control
6.Fast OR connector
7.LV power connector
8.Status LED's
9.Run / Test switch
10.Signal connector
11.Reset pushbutton
12.Cooling pipe
13.HV connector
14.USB connector
15.JTAG connector

macros and Altros are placed on top / bottom of the FEE cards. The traces between the signal connectors and the shaper macros are equalized in lenght. The High Voltage controllers are placed on the left and right sides, not overlapping with the shaper signals. Each Altro chip receives 16 shaper signals which are read out by a 40 bit digital bus. For local servicing of FEE cards in the laboratory the control and status registers can alternatively be mastered by dedicated diagnostic software on a PC connected to the USB port.

The Top and bottom Silk layers of the FEE cards are shown in Figure 28

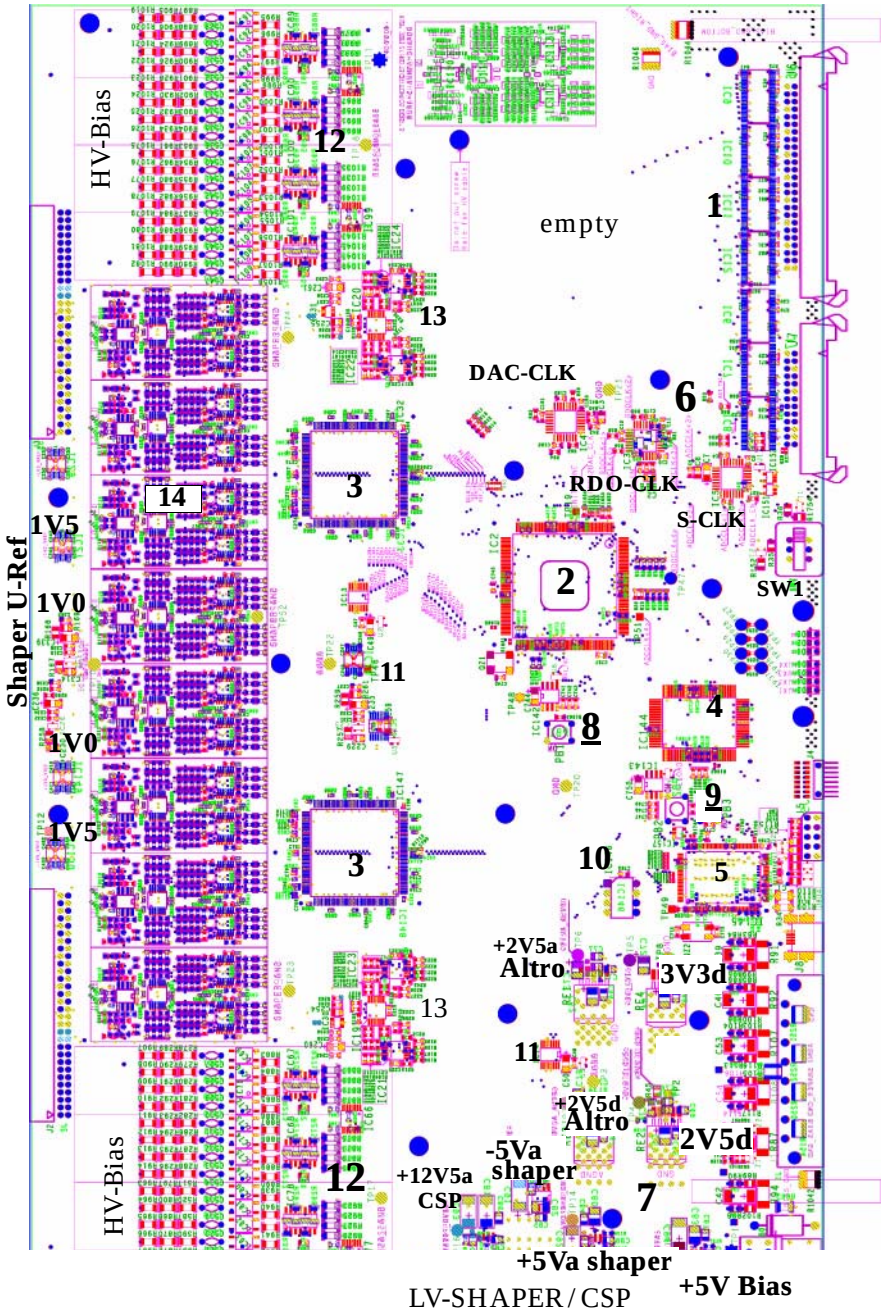


Figure 28 Merged Silk layers of top and bottom FEE card

1.GTL transceivers
2.PMC FPGA
3.ALTROs (Top + Bottom)
4.Flash
5.USB controller
6.Clock drivers
7.LV regulators
8.Reset FPGA and USB
9.Reload
10.Eprom USB
11.Temperature Sensors (T + B)
12.Bias DACs
13.Fast Or shapers
14.Dual g. shapers (T+B)

The details of the 10 layer PCB stacking are depicted in Appendix 13

2.2 Semi-gaussian shaper

For 32 channels with 14 bit range, 2* 32 semi-gaussian shapers of high and low gain are required. The PHOS shapers are built in discrete logic from a RC high-pass and a second order active low-pass with a common cutoff frequency f_c, corresponding to a integrator time constant $\tau = 1/(2\pi f_c)$ (see Chapter 7). The ENC noise analysis for this CR-2RC type shaper (see chapt 6.4) results in an optimal integrator constant for $\tau \geq 2\ \mu s$.

The second order implementation was chosen in view of globally 13% better noise suppression compared to a first order version. For the 2nd-order implementation, the corresponding peaking time τ_p of time response pulse is the order of the filter (n=2) multiplied with the integration time constant, hence the peaking time of the output pulse for $\tau = 2\ \mu s$ is

$$\tau_p = 2^* \tau = 4us.$$

The shaper constitues a bandpass with a -20 dB/octave high-pass, followed by a 2nd order low-pass of -40 dB /octave. A differential driver polarizes the shaped time-response pulse into two skewless, complementary signals of 1 Volt maximum swing, corresponding to the 10bit analog input range of the ALTRO ADCs.

The analytic solution of the combined CSP / shaper circuitry is analytically obtained as **semi-gaussian** time response:

$$Vout(t) = \left[\frac{n^n Q \cdot A^n}{C_f}\right] \cdot \left[\frac{t}{\tau_p}\right]^n \cdot e^{-n\frac{t}{\tau_p}}$$

Equation 4 General form of analytic shaper time response of order n

where n is the order of the integrator stage, *A* the open loop amplification factor of the CSP, Q the charge at the input of the CSP, C_f the CSP feedback capacitor and τ_p the peaking time of the pulse $V_{out}(t)$.

In general, a second order (n=2) shaper generates a Gamma-2 time reponse of time constant τ_p,

$$\mathbf{Vout(t) = Q * Gain\ factor * \Gamma_2(t,\tau)}$$

with a peak amplitude proportional to the APD charge Q and a time position of the peak amplitude which is amplitude independent. This is mathematically due to the linearity of the CSP - Shaper chain and conditioned by a delta-function like APD charge collection time. For an integral charge collection time in the order < 35 ns (see 1.1.2), no amplitude dependence is observed however the peaking time of the output pulse is delayed by the charge collection time. The primary charge generation time can hence be determined from the output pulse shape.

The offline determination of Time Of Flight (TOF)(see chapter 5) depends on the linearity between the APD charge stimulus and the ballistic effect of the shaper, producing a semi-gaussion pulse in a very linear relation with the charge integral. The shape of the semi-gaussian output carries the charge timing information, which can be recuperated offline with very high precision.

By defining t_0 as the time at the peak amplitude of the shaped pulse, the output pulse is decribed by Equation 6.

$$Vout(t) = \left[\frac{4Q \cdot A^2}{C_f}\right] \cdot \left[\frac{t - t_0}{\tau}\right]^2 \cdot e^{-2\frac{t - t_0}{\tau}}$$

Equation 6 PHOS shaper response function

Using low tolerence values for shaper resistors and capacitors of the shaper, the measured time response of the pulse is very well described by the above analytic form. Figure 29 shows the

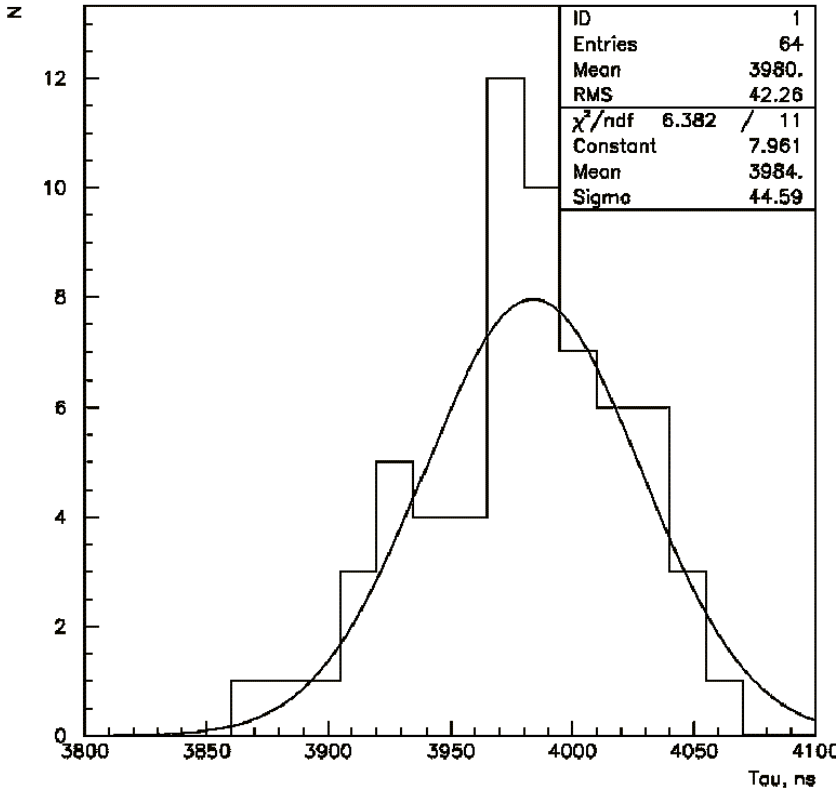


Figure 29 Measured distribution of τ for all 64 shapers of one FEE card: 3.98 us mean

measured distribution of shaper peaking times over all 64 shapers of an FEE card. It corresponds in a narrow band of 0.044 us to the design value of 4 us.

The analytic form of the CERN / Wuhan shaper is shown in the following sub-chapters

2.2.1 CERN Wuhan shaper

The schematic diagram of the CERN / Wuhan shaper is shown in Figure 30. A low noise buffer

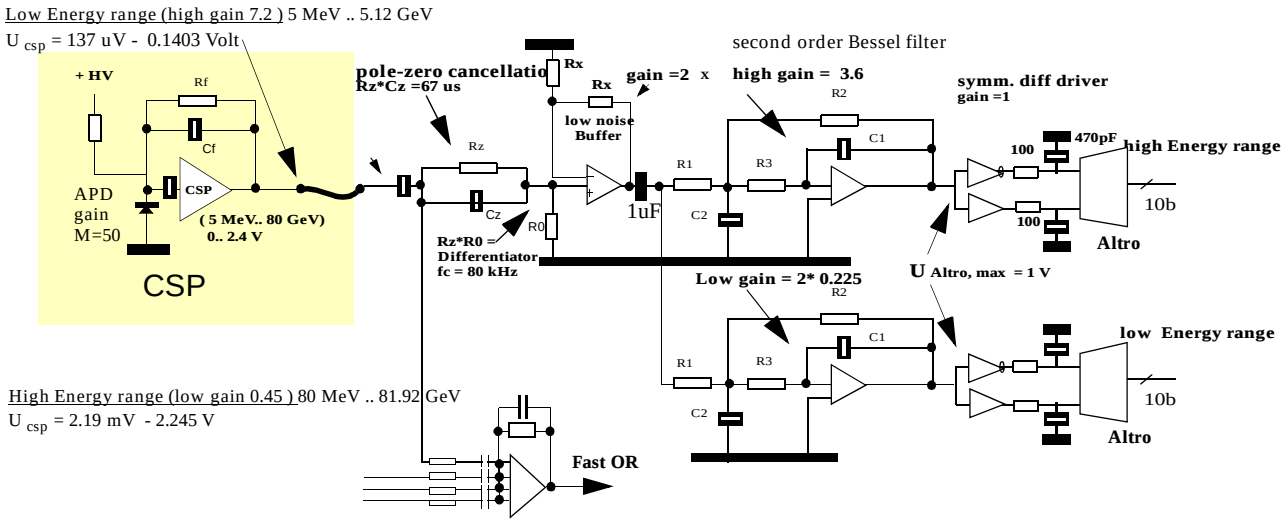


Figure 30 Schematics of the CERN Wuhan shaper (C/W)

of gain 2 separates the combined RC differentiator / pole-zero network from two active Bessel filters of gain ratio 16. The high gain shaper passes the low energy signals from 5 MeV to 80 GeV into the 1 Volt input range of the 10 bit ADC. With a total gain of 7.2, the low energy range shaper features an optimal RMS noise of 0.62 ADC counts (Figure 60) with connected detector at APD gain M=50.

The high energy range shaper applies an attenuation of 0.45 in order to fit high-energy CSP signal amplitudes of up to 2.4 Volt into the 1 Volt ADC window. (The RMS noise is irrelevant for the high Energy range). A skewless, fully differential output stage with high frequency RC filter connects the shaper to the ADC input. The fast OR shaper signals are derived from the shaper input signals.

The shapers were initially designed with Matlab [15] according to the filter methods described in chapter 7 For the high energy range with target gain =0.45 the analytic form of shaper time pulse fuction (Equation 7) is shown in Figure 31: superimposed with a mathematical

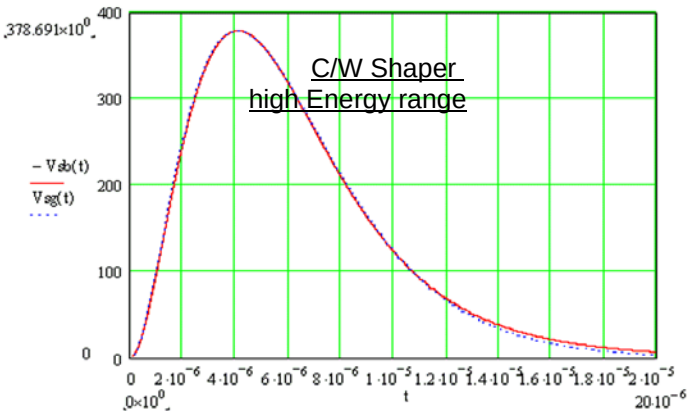


Figure 31 Calculated transfer response for C/W shaper [15]: Superimposed semi-gaussian time response of order 2 (Vsg(t)) with shaper B of gain =0.41, covering the high Energy range 80 MeV- 81.92 GeV in 1024 bit

$$V(t) = 2.798 \cdot 10^3 \cdot \left[\frac{t}{4.06\mu s}\right]^2 \cdot e^{-2\frac{t}{4.06(\mu s)}}$$

Equation 7 Analytical C/W shaper equation High Energy range

Gamma-2 function.

The same analytical output is shown for the low Energy range with gain =7.2 in Figure 32 and Equation 8:

$$V(t) = 47.4 \cdot 10^3 \cdot \left[\frac{t}{4.1\mu s}\right]^2 \cdot e^{-2\frac{t}{4.1(\mu s)}}$$

Equation 8 Analytical C/W shaper equation Low Energy range

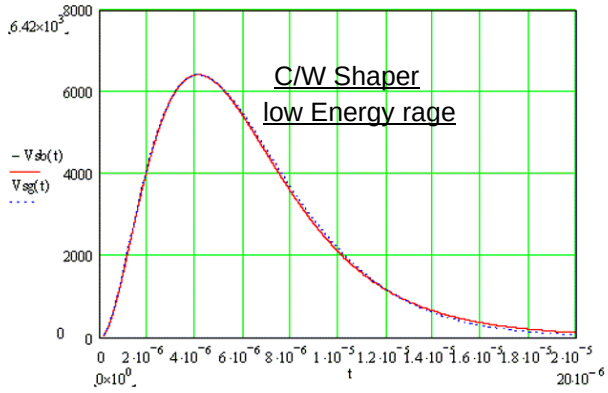


Figure 32 Calculated transfer response for C/W shaper [15]: Superimposed Semi-gaussian order 2 (Vsg) with shaper B output (Vsb) of gain =3.35, covering the low Energy range 5 MeV- 5.12 GeV in 1024 bit

These design values have been tuned after verification in the testbeam including the pole-zero cancellation. The obtained gain and RC values are shown in chapter 7.2 . The measured gain ratio is 16.3

2.2.2 Kurchatov shaper

On the FEE cards V 1.0 and V1.1 a simple 2us shaper option is available as alternative implementation option. This Kurchatov shaper is depicted in Figure 23. It uses less active components and replaces parallel differential amplifiers by skewed differential amplifiers. With a common attenuation of 0.22 in the input stage, the K-shaper requires twice the linear output swing of the CSP at a nominal APD gain of 100. With shorter integration time constant (wider bandpass) and with attenuation of low Energy signals, the RMS noise is ca 900 electrons (see 6.3) . A revised K shaper is subject of ongoing R&D and will be documented at a later time [23] i

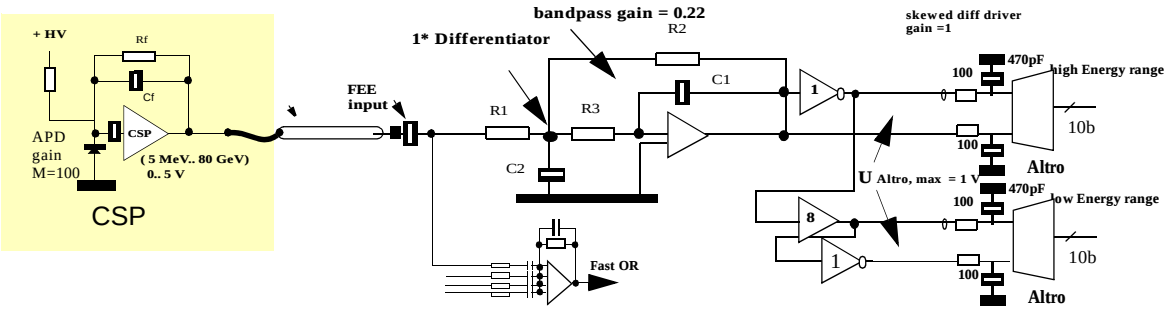


Figure 33 Schematics of the Kurchatov shaper (K)

2.3 High Voltage, APD bias control

The large spread of APD gain at T = -25 C of up to 300 % makes gain control of APD necessary. The FEE cards implement therefore 32 individual high-voltage bias controllers for all connected APDs (see Figure 34).

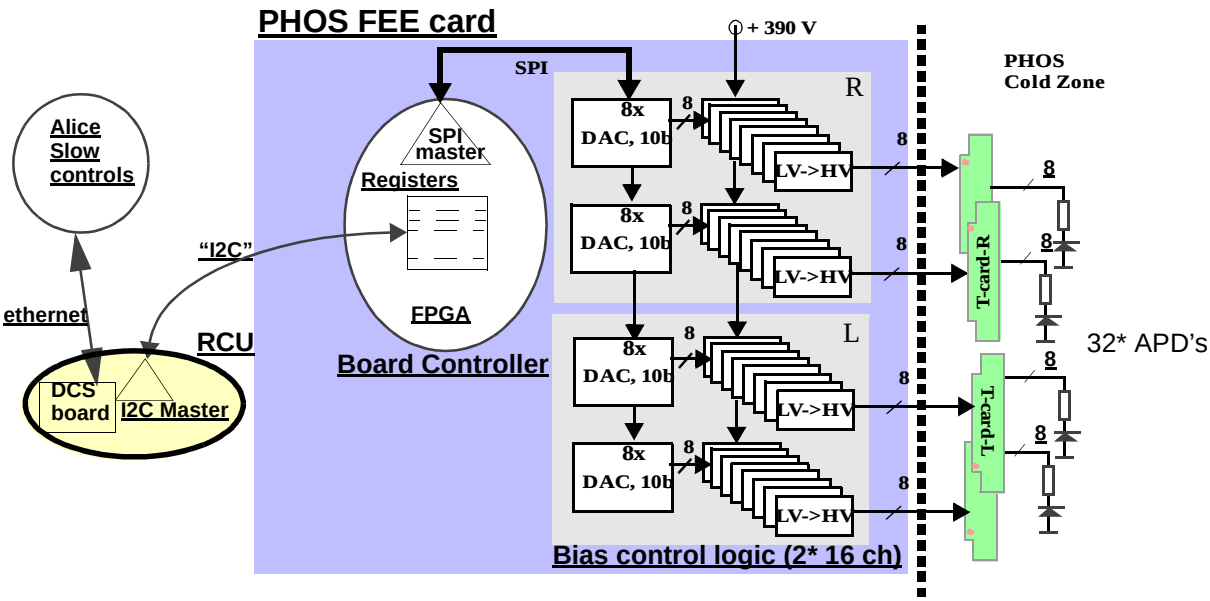


Figure 34 Principle of HV Bias controller

A single LV->HV converter cell is shown in Figure 35

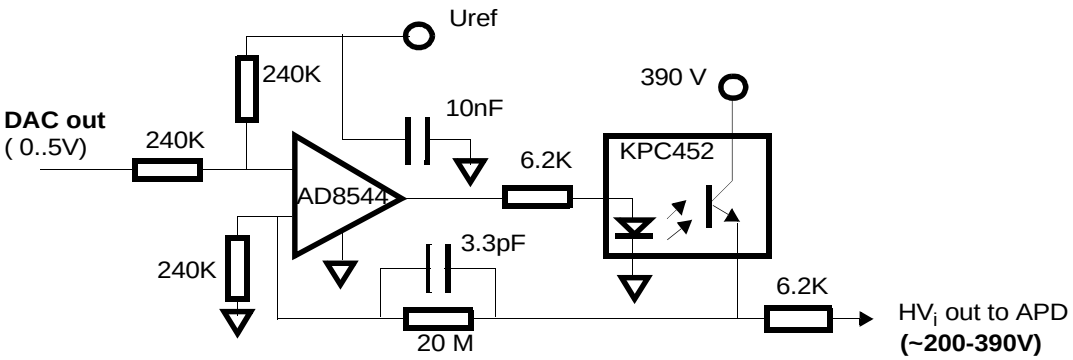


Figure 35 PHOS LV-HV adapter (one of 32)

32 individual precision voltages in a controlled range between 200 and 390 Volt are derived from a common input Voltage of 390 Volt [24]. The controller circuit for HV_i regulation via optical couplers is depicted in Figure 35. Each APD bias is set via a 10 bit digital value, converted by a 10 bit DAC for a slope of ca. 0.2 Volt / bit. The maximum Voltage corresponds to the input voltage (390 V). Each DAC is controlled via the Motorola SPI serial bus, mastered by the PCM controller FPGA.

Each individual APD has a nominal leakage current of 1nA (-25 C), however each converter circuit requires a current of ca. 20 uA per channel for a bypass resistor in order to operate in a stable way.

With 32 HV supply channels, a single FEE card requires a minimum of 0.64 mA @ 395 Volt.The DAC settings are controlled remotely, via the RCU, though the slow control system. The RCU operates as networked master which can address (via the I2C protocol of the FEE readout backend) all registers of the PCM board controller. The 32 DAC registers are simply mapped into this register set.

. The Bias regulators are grouped into two 16 channels at the left and right extremes of the FEE

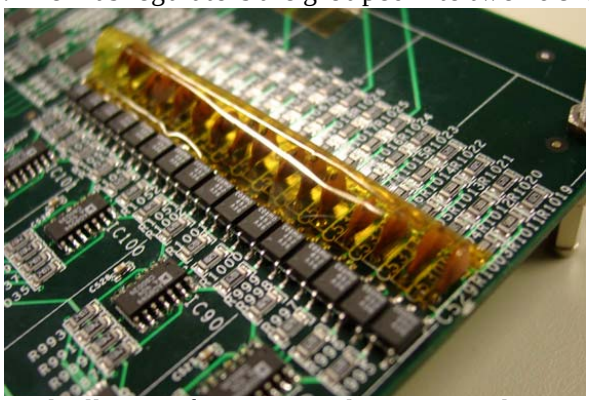


Figure 36 Photo of the right side block of 16 Bias controllers on the FEE card.The high voltage traces to the FEE connector do not cross with any signal. A capton foil protects the upstanding ceramic capacitors from touching the cooling cassette and pipes which will surround the FEE card.

card, allowing for HV signal routing to the FEE connectors without crossing signals. The total current drawn from the 390 V primary supply per FEE card is 0.65 mA such that 14 FEE cards can be alimented from a single, daisy chained HV supply line of max 10 mA. With 8 FEE domains per PHOS module, this corresponds to a single, 8 channel HV ISEG supply[1] (compare Chapter 15

2.4 Readout Backend

The digitizer and readout backend of PHOS FEE electronics is closely related to the Alice TPC electronics [10] and hence uses the 10 bit ALTRO-16 chip[1] [3] developed for the Alice TPC. The Altro ADC contains zero-suppression logic as well as an 8-deep multi-event buffer (MEB). A GTL+ bus, mastered by the external RCU, is used for MEB readout under timing of the level-2 trigger rate.

A single RCU partition has two GTL branches, i.e. covers 28 FEE cards and 2 TRU cards. New features of the RCU allow for sparse data readout, allowing to skip the readout of empty buffers and leading to significant reduction of the required readout bandwidth. The 40 bit wide GTL bus implies that groups of four 10-bit ADC's inside the Altro chips can be read in parallel, hence with 16 ADC's per Altro chip, digitized samples are read out in four consecutive bursts.

The 40 bit wide GTL+ data bus is used together with a 26 bit wide control bus, which interconnects TRU domains (14 FEE cards) with the RCU module. The latter masters the MEB readout as well as control and setup of the FEE cards via the control bus which contains the I2C protocol as a subset.

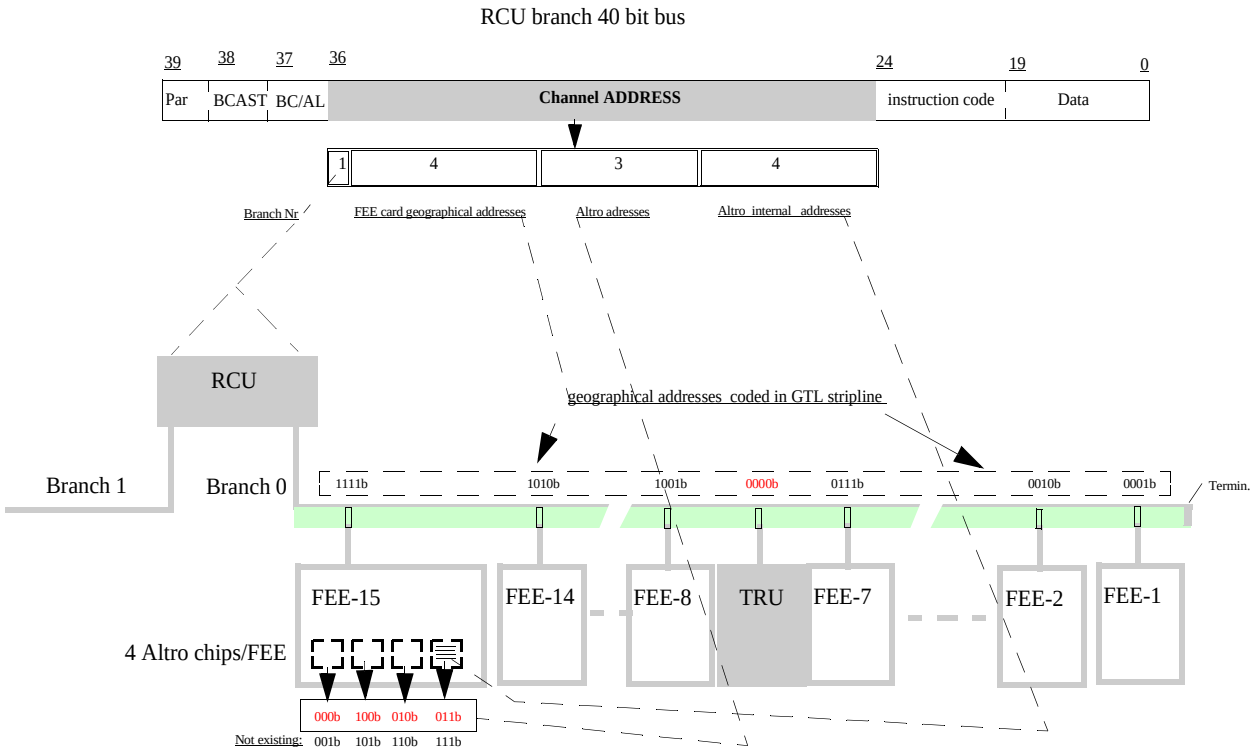


Figure 37 Address scheme of 14 FEE cards and one TRU card via the 40 bit GTL bus

1. ISEG EHQ 8605p_156-F (8-ch floating ground)
1. commercially available via ST Microelectronics

The TRU module is connected to the same GTL bus as the FEE cards, hence is seen by the RCU like an FEE slave. The RCU address mapping for the PHOS FEE cards is depicted in Figure 37. The channel address field in the 40 bit frame contains a 4 bit geographical address by which FEE cards are selected. These addresses are allocated to fixed posistions on the GTL bus.

Note: The TRU is placed at the special address 0 which is geographically *in the center* of the GTL bus.

The TRU card may also act as RCU master if connected to an external USB2.0 master (any PC with appropriate software).

2.4.1 Channel mappings

For each FEE card, there is a fixed relation between Altro chip High and Low gain channel addresses of the connected 32 crystal channels. Figure 38 shows this mapping in a geographical way: one FEE card maps with two rows of 16 crystals. The crystals are numbererd with their CSP preamplifier numbers.

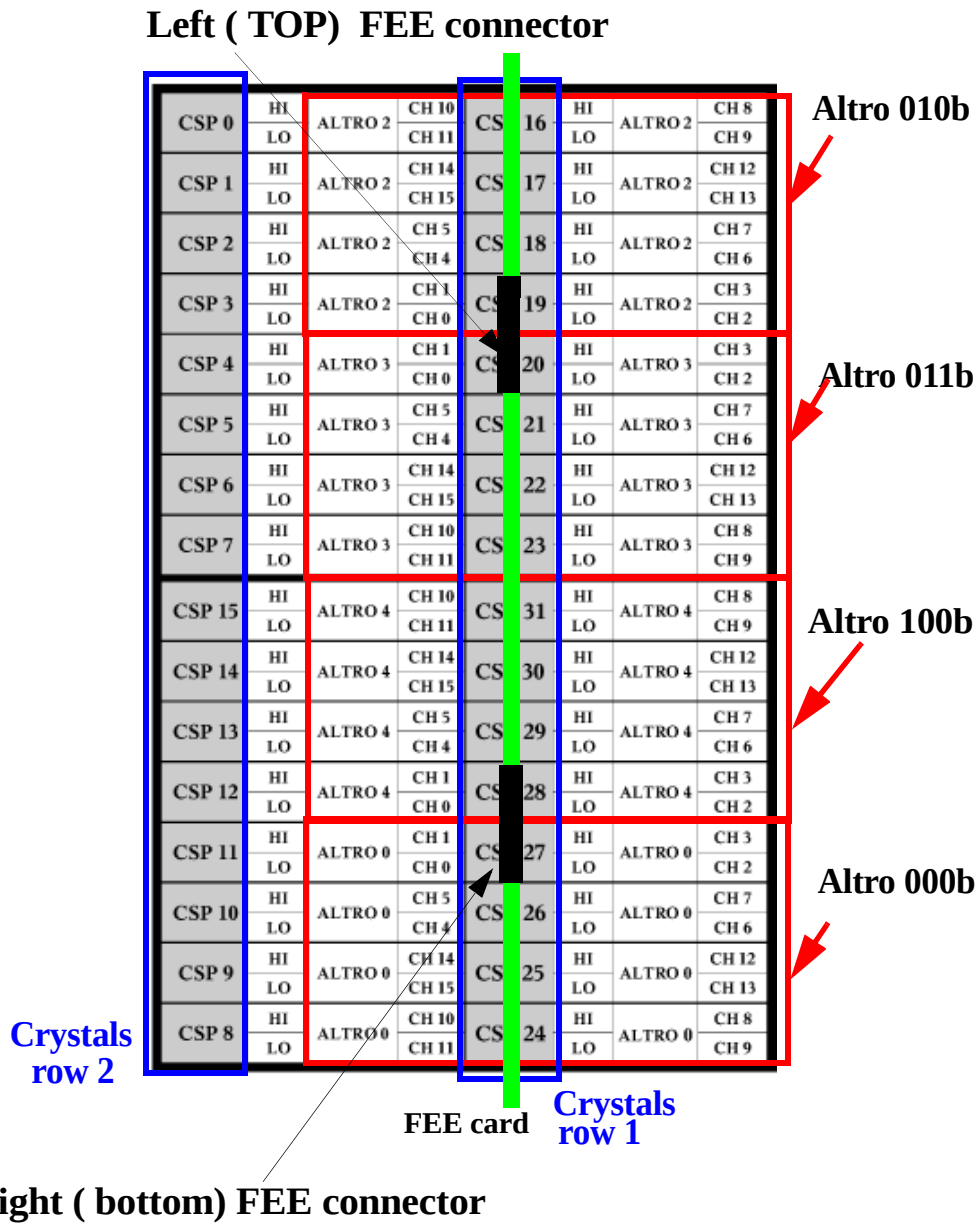


Figure 38 Channel mappings Altro - PHOS crystals (CSP)

2.5 Quad analog sums for TRU trigger

Since 80% of the PWO scintillation light is generated withing less than 35 ns (see Figure 8), a relatively precise charge TRU trigger can be based on 100 ns analog sums based on 2*2 cells. The TRU alogorithm generate charge sums over a 4*4 sliding window based on 2*2 analog or inputs.

In order to generate 2*2 analog sums, the FEE cards split the CSP preamplifier output signals into semi-gaussian and in fast-OR channels. The latter are generated by simple RC shaper (see Figure 39) with 100 ns FWHM on the FEE cards. With eight analog sums per FEE card, a TRU trigger card receives 112 analog sums from 14 FEE cards (for connectivity see Figure 97). In this way, one TRU card receives summed charge signals from 14*32 = 448 crystals.

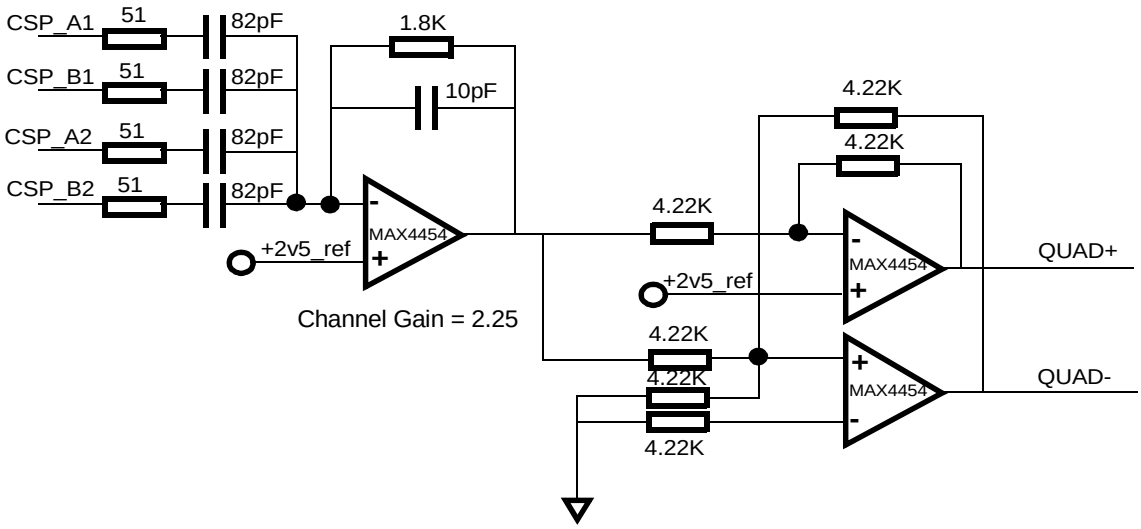


Figure 39 Schematic diagram of simple Fast Or shaper. There are two RC time constants for fall and risetime which combine 4 CSP signals into s summed signal. A differential line driver allows to send the quad charge signal over a 50 cm diffrential cable to the TRU trigger card.

Figure 40 A shows the time relation between the CSP output and the analog sum signal. .

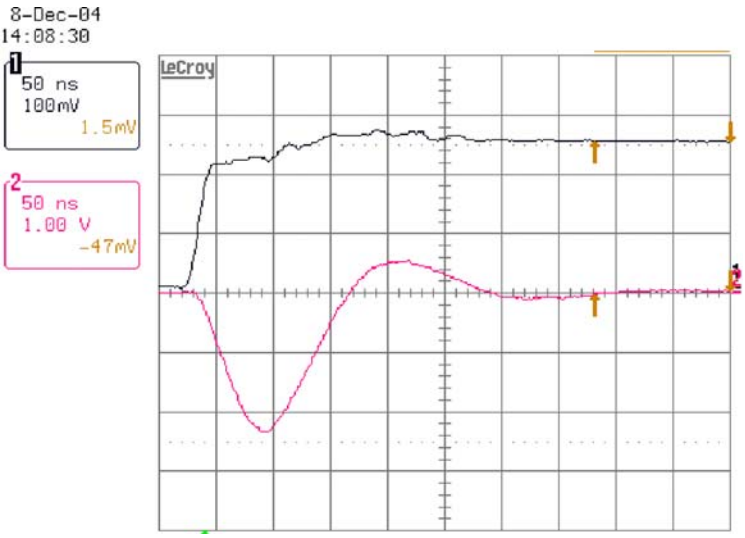


Figure 40 A Direct Fast-OR signal on the FEE card relative to one of four CSP outputs is shown. The CSP signal corresponds with 250 mV and ~ 25 uV / MeV[1] to ~ 10 GeV per crystal. The Fast OR output Voltage from 4 equal CSP signals of 4*10 GeV is 2.25 Volt

1. Equation 3

The latency between the risetime of the CSP signal at the FEE card input and the FOR is ca 75 ns, hence with ca 1 m cabling before and after the FEE card the FOR signal is available at the TRU input at ca 80 ns after the APD charge conversion. Differential flat cables[1] of equal length (50 cm) connect the FOR output of the FEE cards to the TRU input. With 10ns APD charge response and another 10 ns for the scintallation light after excitation, the FOR signal is ca.100 ns after interaction available at the ADC of the TRU. This ADC has a 12 bit range for 2 Volt

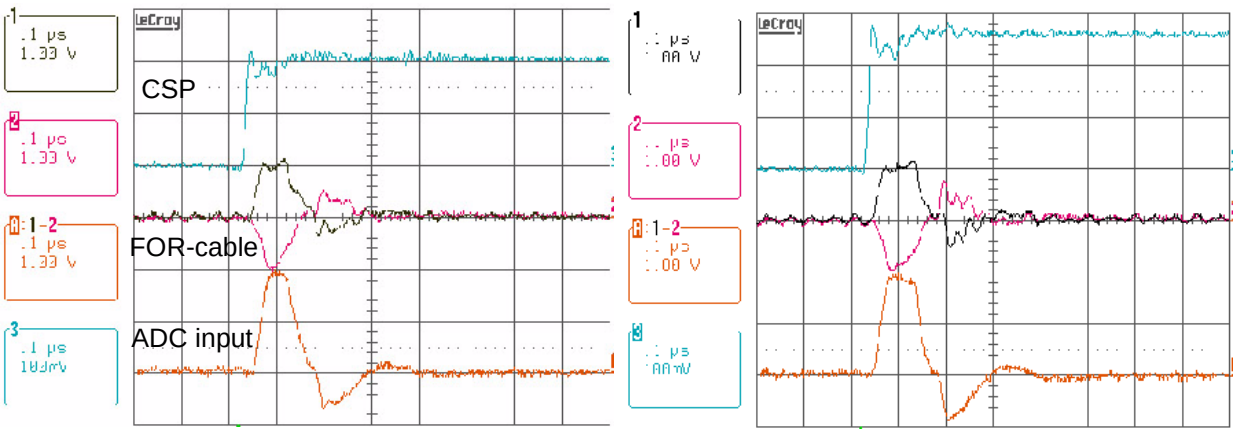


Figure 41 Relation between 1 CSP, differential cable and ADC input of FAST Or. LEFT: 32 GeV equivalent input. RIGHT: A 10 GeV higher CSP voltage saturates at 2 Volt at the ADC.

input. Figure 41 LEFT shows that a 2 Volt pulse at the ADC of the TRU corresponds to 200 mV CSP Voltage, hence with 4 CSP's and ~ 25 uV / MeV, the maximum TRU range is 32 GeV. Input pulses of higher Energy than 32 GeV saturate the FOR logic on the FEE card and hence produce a pulse of the same 2 V amplitude at the ADC input of the TRU.

1. SAMTEC FFSD-08D-20.00-01-N

3 Linearity

The energy and timing measurements are based on linearity between the energy of the electromagnetic shower and the peak amplitude and position of a semi-gaussian pulse. Explicitly, the linearity is a feature of the design methods applied for the FEE shaper (see Chapter 7) Implicitly this linearity relies on charge integration within a very short time and on the linearity of the output voltage swing of the CSP over the maximum ADC range. With a PWO scintillation decay time (Figure 8) of ca. 10 ns, photoelectrons generated by the APD are converted into a step voltage over the charge integrating capacitor of the CSP like shown in Figure 12. The range of the CSP Voltage swing for a nominal APD gain of M=50 for two shaper gains is composed of two ranges (compare chapter 4.1 :)

High gain : 5 MeV - 5.12 GeV: U_{csp} = 137 uV - 0.1403 Volt <u>shaper gain = 7.2</u>

Low gain : 80 MeV - 81.92 GeV : U_{csp} = 2.19 mV - 2.245 Volt <u>shaper gain = 0.45</u>

The maximum linear CSP range is therefore 2.245 Volt. The linearity of the C / W shaper was measured in Figure 42 for the high energy range: showing that the linearity is better than 0.5%.

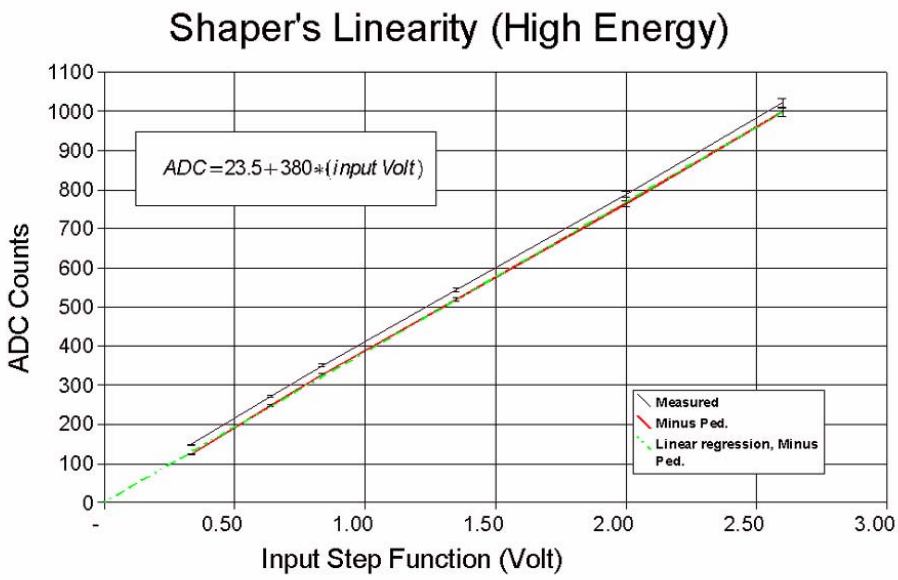


Figure 42 C/W linearity in high signal range, measured with pulser step input

After a pedestal subtraction of 23.5 ADC counts, the curve passes through zero.

The CSP capacitor is auto-discharged with a time-constant of 100 us, which is small compared to the maximum channel counting range (200 Hz see 10.1) The pole-zero cancellation on the FEE cards corrects for the linarity deficit which is generated by the auto-discharging of the CSP capacitor, i.e cancels the signal undershoot. The mathematical linearity correction is handled in chapter 7

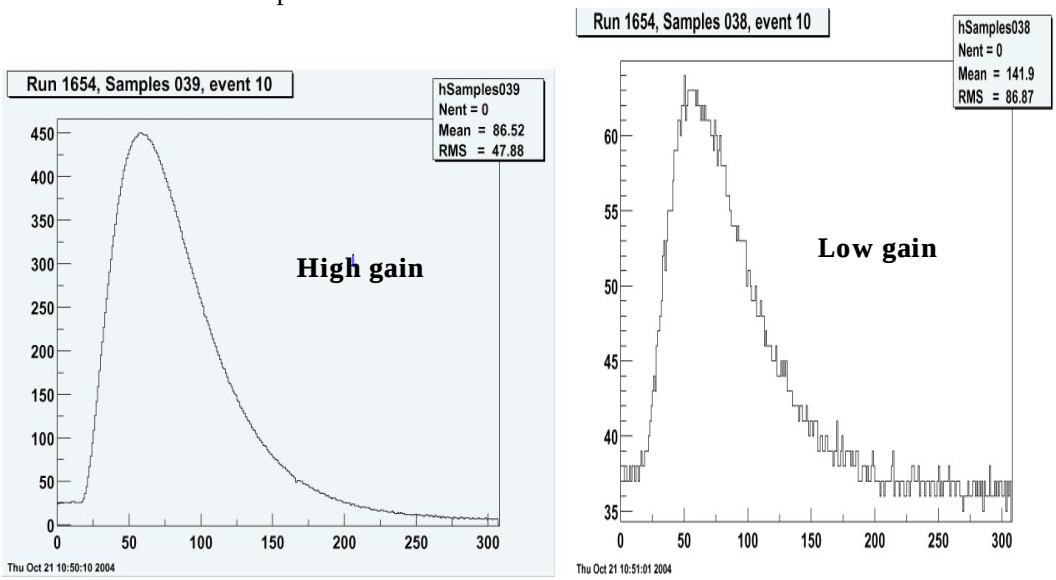


Figure 43 High and low gain channel of the same pulser input.

The dual gain outputs for the same input signal are shown in Figure 43. The measured gain ratio for pedestal-corrected amplitudes is 425 / 26 = 16.3.

The digitized semi-gaussian signal output of a LED pulser test signal, recorded after the CW shaper is shown in Figure 44 with and without pole-zero cancellation. The signal corresponds to the CSP signal shown in Figure 14.

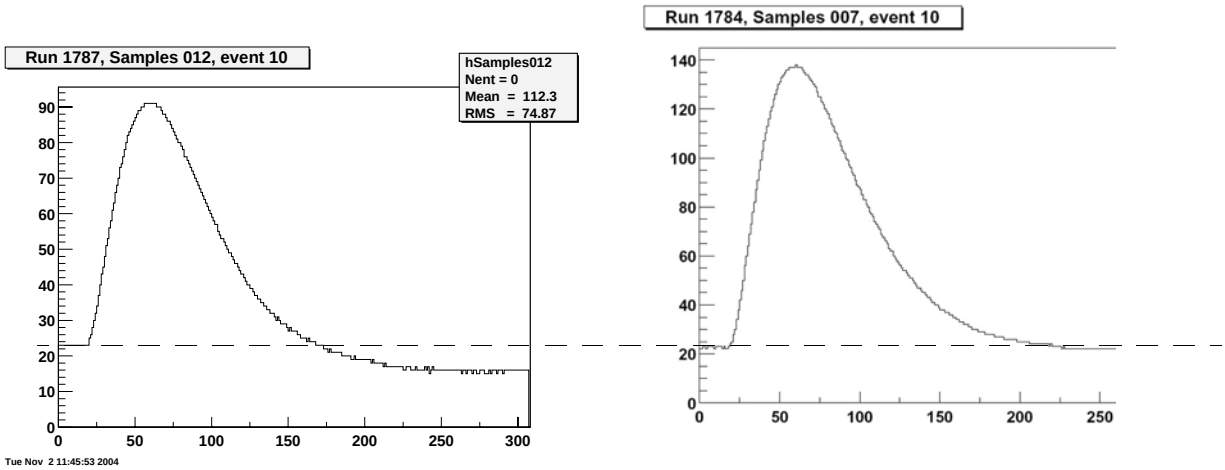
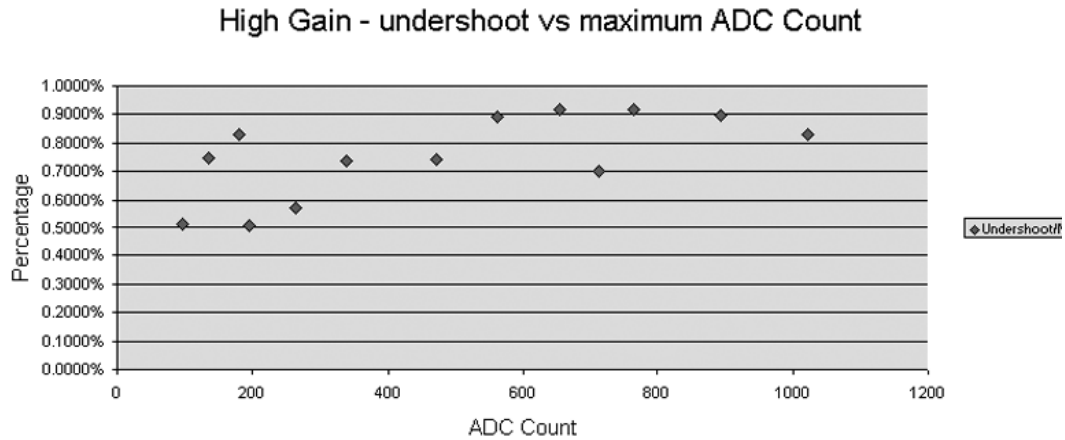
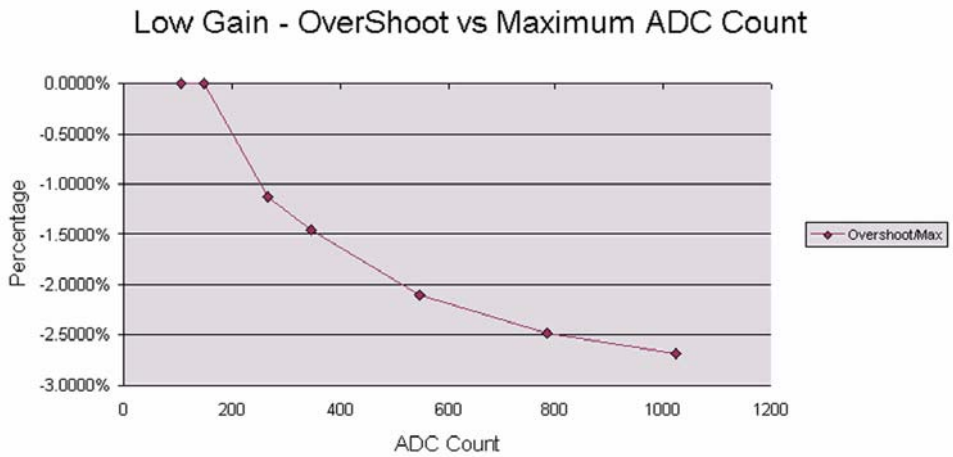


Figure 44 Digitized Shaper output LEFT: without RIGHT: with pole-zero cancelletion

The high gain underhoot for CSP signals < 0.14 V is cancelled by the pole-zero compensation of the shaper to a level below 1 %. (Figure 45,) For the low gain range an





Low signal range: underhoot ~ 0.8 %

High signal range: overshoot up to 2.7

Figure 45 Pole-zero correction Wuhan/CERN

amplitude-dependent overshoot up to 2.5 % of the max CSP signal of 2.3 Volt[1] is measured.

1. probably indicating a slight baseline upshift in the CSP for signal amplitudes above 2 Volt

4 Energy resolution

The PHOS energy resolution σ/E in dependence of EM shower energy was measured [19] with a 16*16 PWO prototype matrix during the CERN SPS testbeams 2002 ... 2004 (see Figure 46)

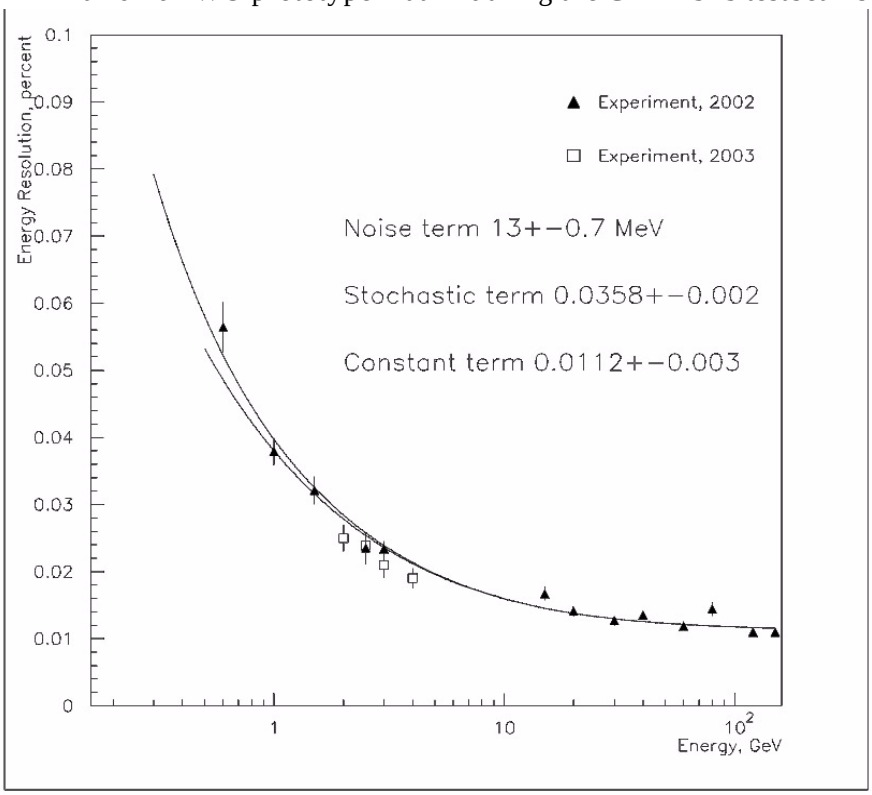


Figure 46 Testbeam Results of PHOS Energy resolution 2002 and 2003

The σ/E dependence was fitted with the standard parametrization for calorimeters (Equation 9) ..

$$\frac{\sigma}{E} = \sqrt{\frac{a}{E} + \frac{b}{\sqrt{E}} + c}$$

Equation 9 Standard parameteization of calorimeter energy eesolution

The noise term "a", important for the low energy range, is largely due to electronics noise generated by parallel and serial noise sources at the capacitance of the APD and the CSP input (J- FET) It is a function of the APD dark current and of the FET input noise voltage(see 6.4) Other contributions like pileup and radioactivity are neglegible for PHOS. The σ/E noise term is integrated over 3*3 crystals (since showers are 99% shared in this range) and therefore compatible with the triple single-channel RMS noise.

The stochastic term "b", dominant in mid-energy rangs, is due to statistical effects of shower fluctuations, and quantum efficieny but in particular due to APD execess noise (see Chapt 6.1 .)

The constant term "c" important for the high energy range , depends on quality and detection losses of the calorimeter, on inter-calibration, non uniformities, non-linearity, instabilities in temperature and high voltage, as well as rear/front light leakage. It follows that the inter-calibration of all channels, i..e equal response (product of light yield * APD gain) should be better than 0.5 %.. The programmable APD gain adjustement at -25 ^{o}C with FEE electronics (see Figure 17) clearly simplifies the PHOS calibration. The preliminary determination of coefficients from the data of Figure 46 with 2003/2003 beam test results were estimated as:

- a_{noise} = 13 +- 0.7 MeV
- $b_{stochastic}$= 0.0358 +- 0.002 (3.58 % $GeV^{0.5}$)
- c_{const}= 0.0112 +- 0.003 (1.12 %)

The analog electronics processing chain (from APD to ADC) aims primarily to minimize the noise contributions and maximize energy and timing resolution. Both are only in limits compatible since a low noise shaper bandpass removes high frequency timing components which are needed for the timing information.

4.1 Dynamic range

Table 6 shows the power of 2 values of the nominal PHOS energy equivalence for the two gain ranges. The APD gain is here a priory a variable which requires calibration on a channel-by channel basis until this gain equivalence is obtained (compare Figure 17).

The two ranges cover a total effective range between 5 MeV and 100 GeV with a single channel digital resolution (ADC-count /1024) which lies (apart from the 5 GeV crossover point) well below the σ/E requirement of the calorimeter (see Figure 47.).

Table 6 ADC bit significance in dynamic range

Bit value of peak signal	**1**	2	4	8	16	32	64	128	256	512	1024
High Gain range MeV	**5**	10	20	40	80	160	320	640	1280	2560	5120
Low Gain range MeV	**80**	160	320	640	1280	2560	5120	10240	20480	40960	81920
digital reso-lution %	-	-	-	0.8	1.6	3.2	6.4	12.8	25.6	50	100

Note: The step in the digital resolution at 5 GeV scales with the combined gain before the ADC and is shown here for a nominal APD gain of M=50 and the CW shaper gain ratio of 1/16. Within the CSP linearity range it can be shifted up to 10 GeV for APD gain M=100. For larger shifts, the shaper gain has to be reduced in linear proportion.

Two 10 bit digitization ranges are implemented with fixed gain ratio of 16/1 for the two shapers: high gain for the low energy range 5MeV-5 GeV[1] and low gain for high energy the range 80 MeV -80 GeV. The dynamic range is consequently 80.000/5 = 2**14 (= 14 bit).

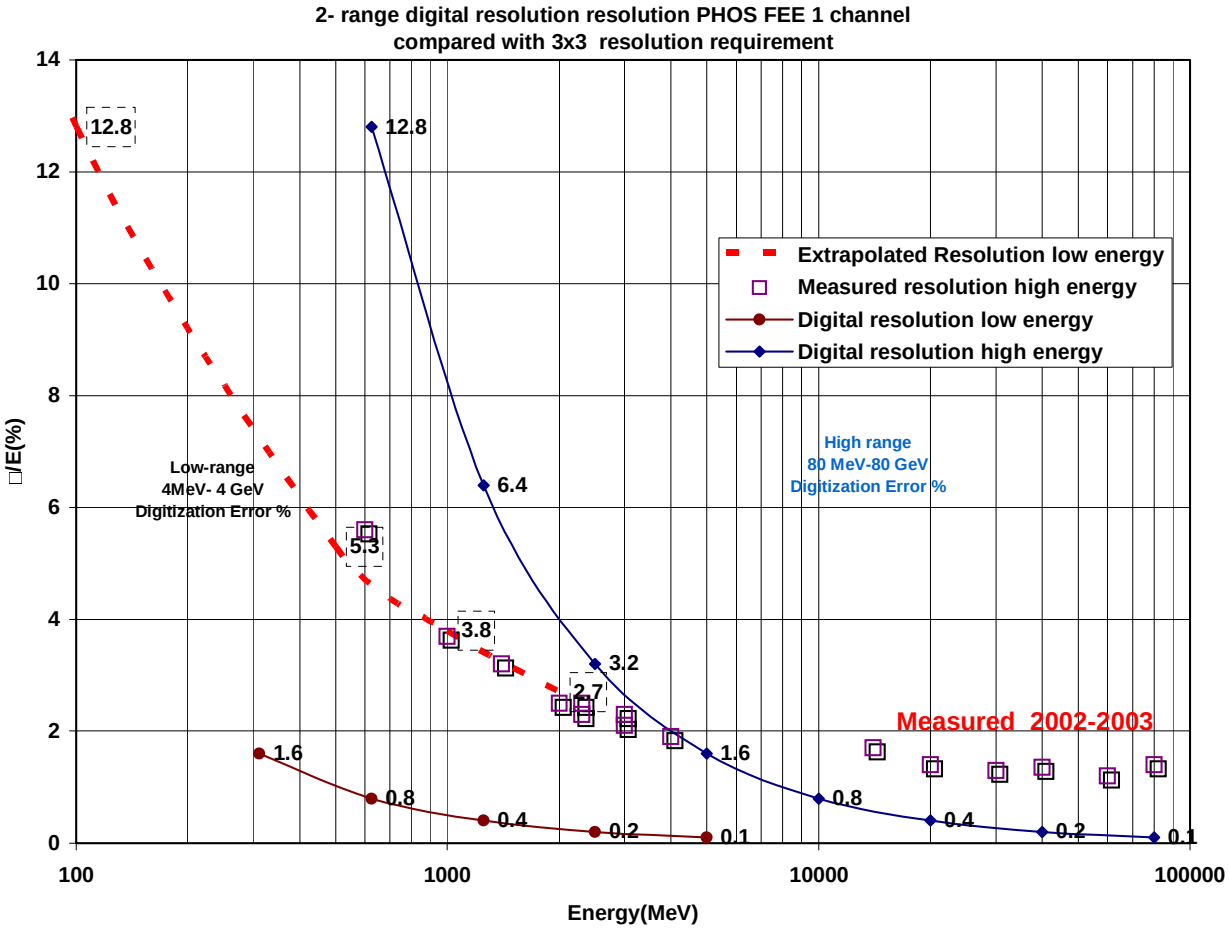


Figure 47 two range single channel digital resolution compared with full calorimeter resolution

This implies an equivalence of 1ADC bit = 5 MeV for the high gain range and 1 ADC bit =80 MeV for the low gain range.

1. The range selection was chosen starting from the requirement that 100 GeV central photons correspond to ca. 80 GeV deposited energy in a single crystal. By selecting 80 GeV as the maximum 10 bit value of the high energy digitizer, the digital resolution is near 5GeV equal to the energy resolution, hence the maximum 10 bit value of the low energy range is set to 5 GeV as crossover point for the two ranges. Based on this, the LSB setting for the digital channel resolution corresponds to 5 MeV which is above the RMS noise floor of 3.2 MeV.

5 Time resolution

Neutrons and anti-neutros contribute via annihilation for a large contamination of photons and hadrons. In order to separate the parasitic processes from primary photons, time of flight separation is needed. For hadron separation, shower distribution cuts are appropriate.

Figure 48 shows the situation as described in the Alice Technical proposal chaper 11.7.4. . The

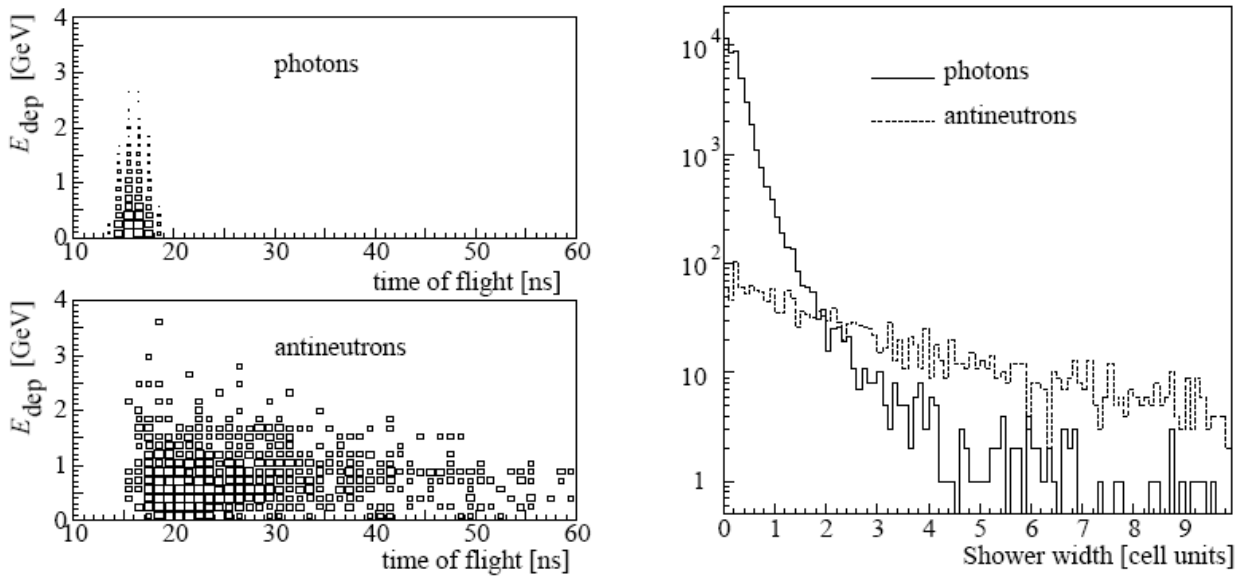


Figure 48 (from Alice Technical proposal) Left: Deposited energy E_{dep} vs. TOF for photons and antineutrons (TOF resolution 1 ns) Right: shower width distributions for photons and antineutrons (GEANT simulation).

time of flight method was estimated to require a timing resolution of ca. 1 ns at 1 GeV. An approch to implement time measurement in hardware on the FEE electronics was however far too expensive. It was concluded that TOF resolution of the order of 1 ns could be obtained by offline determination from the digitized shaper pulse.

For optimal TOF determination, the Gamma-2 CW shaper pulse characteristics and linearity have been carefully evaluated [15] and confirmed with testbeam data (see 2.2 . and Figure 44)

More recent simulated spectra [1] of photons and background compared to neutrons and antinutrons for 1 (left) and 2 ns (right) TOF resolution (Figure 49) show suppression levels

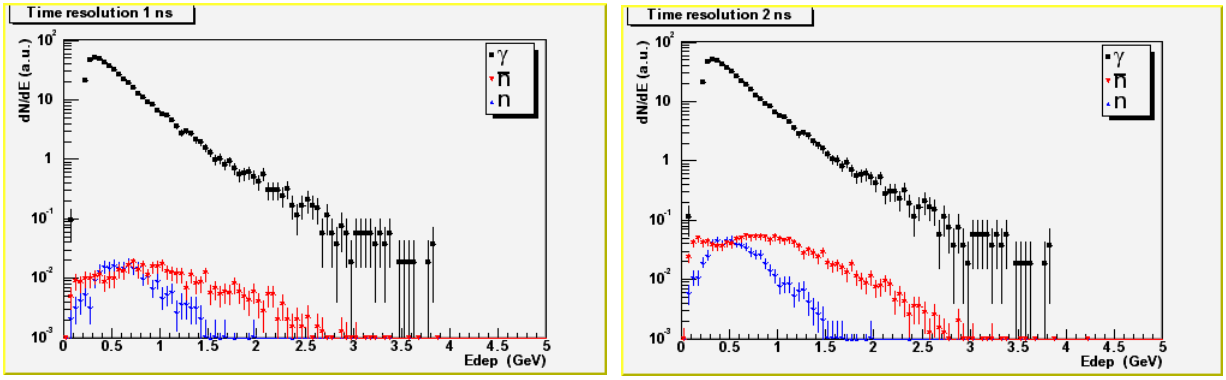


Figure 49 recent simulation by D.Peressounko for TOF separation of neutron and antineutrons from gammas

against photons and background. Without TOF cut, the antineutron contamination would amount to ca 10% between 1 and 3 GeV, with 2 ns resolution ~2 % and with 1 ns < 1 %, i.e. the systematic error in photon identification depends strongly on the TOF resoluution and resolution of 1 ns is desirable.

The FEE card electronics aims to maximize the timing resolution within the limits given by the energy resolution (Chapter 4), both requirements are somewhat contradictory. For the CW shaper, the bandpass can be adapted by recalculation the R-C components. (see method desribed in 7.1)

The following features have been implemented for an optimal timing resolution:

- the shaper reproduces an analytically described Gamma-2 function
- the pole-zero cancellation corrects linearity and eliminates signal undershoot
- the shaper time contstant is selected to minimize the total ENC noise
- the low-energy shaper amplifies the signals
- a strictly symmetrical interface between shaper and ADC preserves time resolution

1. Dmitri Peressounko (dmitri.yurevitch.peressounko@cern.ch)

The instrumental time resolution of the detector with preamplifiers was improved in 2004 testbeams to a level of 0.5 ns above 1 GeV (Figure 50) .Figure 51 shows the pulser-based differential time resolution

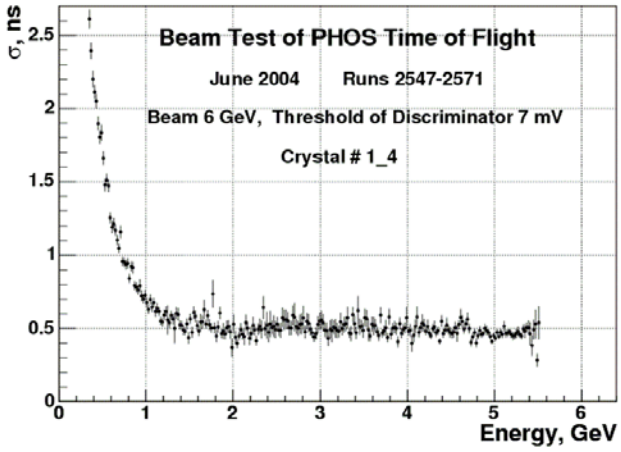


Figure 50 Instrumental timing resolution of PHO detector without FEE electronics

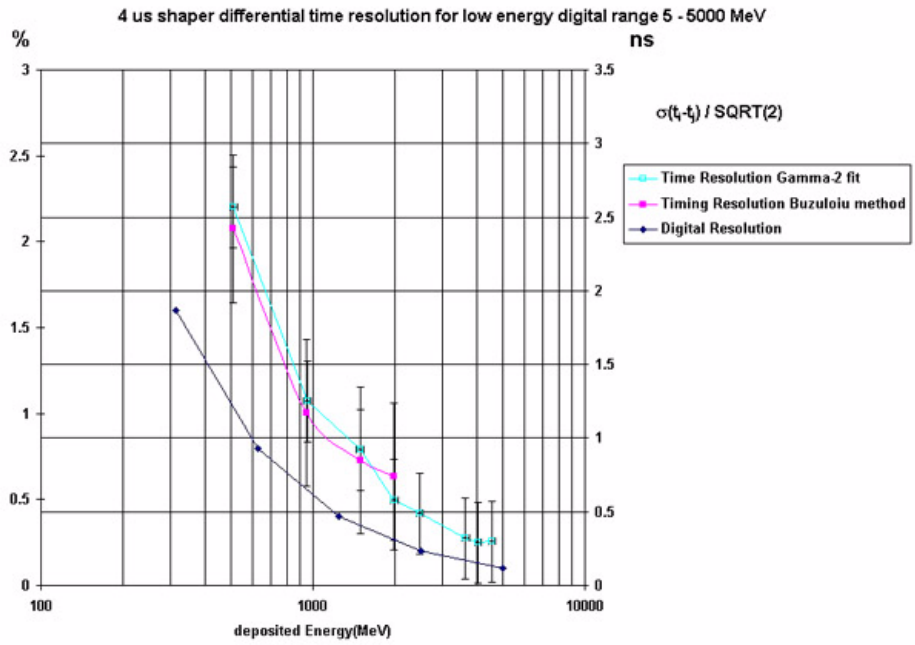


Figure 51 Measured differential timing resolution with pulser for the 4us CW shaper.

Comparison with the digital resolution ADC_{signal}/ADC_{max} shows that timing resolution is dominated by the number of available bits, i.e shows a 1/E dependence.

between two channels of the FEE electronics with CW shaper, measured with two different methods: Gamma-2 fit and Peakfinder. These pulser measurements correspond to an equivalent energy setting of 1024 ADC counts = 5 GeV. Each measurement is a Root fit with $\Gamma_2(t, \tau=4us)$ for timing differences between neighboring FEE channels with 4 us CW shaper. The measured timing resolution is proportional 1/E .The 1/E dependence originates from the digital resolution (analog signal input / max analog signal input) of the 10 bit ADC, resulting in 0.1% for Emax = 5 GeV (bottom curve) As a consequence, lower energy eqivalence per bit (i.e. higher APD gain) shifts the timing resolution over the E scale, however this would modify the dynamic range. A better approach is the use of more bits, either by making used of both ADC's for the full 14-bit range, or by overclocking and obtaining more effective bitts.

At 2 GeV , the pulser-based FEE card timing resolution with 4us CW shaper is ca 800 ps.

5.1 Measurement of differential timing resolution with step pulse on FEE

The differential time resolution consists of measuring a common light stimulus of one channel

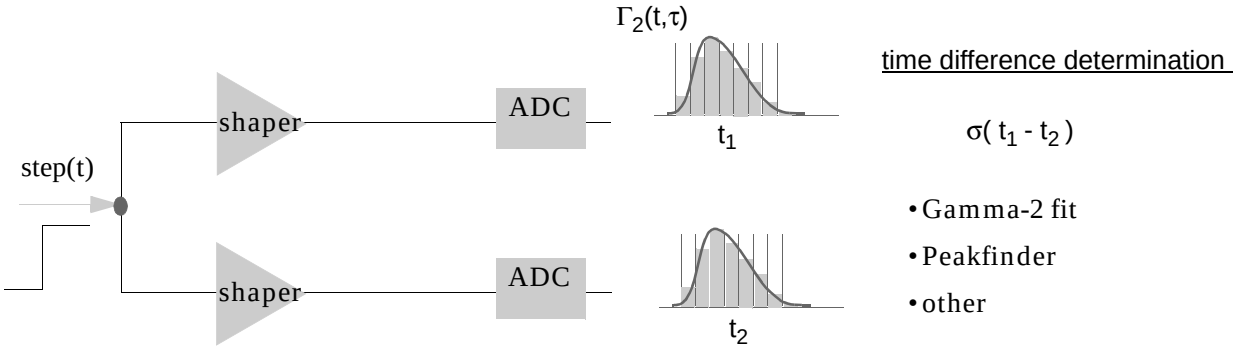


Figure 52 Principle of differential TOF resolution measurement

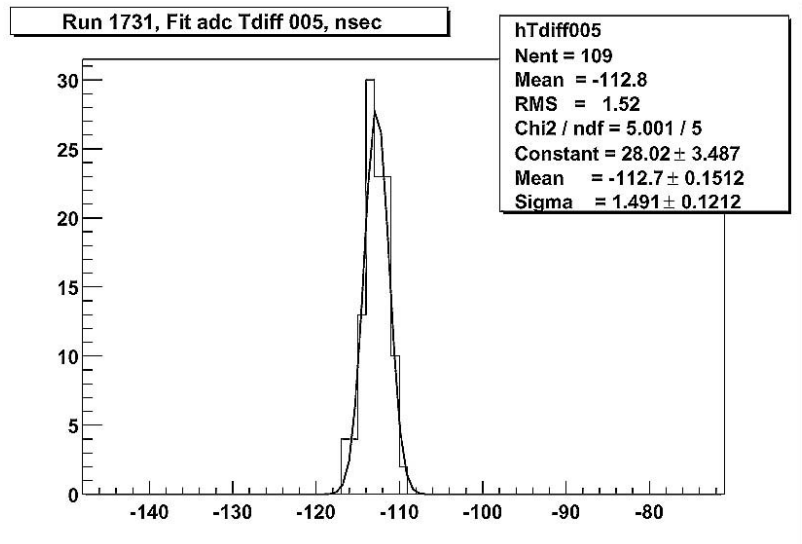


Figure 53 Differential timing resolution at 2 GeV with pulser on FEE card,

against another one. Figure 53 shows the Root plot of the difference of Gamma-2 fits between two channels. A 15 ns step function with amplitude equivalent to a 2 GeV CSP pulse was applied to the input of the FEE card, to two adjacent shaper channels. The shapers are 4 us CW-shapers @ 10 MHz ADC sampling.

$$\Delta t = 1.49 \text{ ns} / \text{SQRT}(2) = 1 \text{ ns} \quad @ \quad 2.1 \text{ GeV}$$

(Note: This measurement was taken during testbeam when the ADC noise of Figure 59 was not yet eliminated)

5.2 Measurement of differential timing resolution with blue LED

For a differential timing resolution measurement in the laboratory (December 2004) a blue LED (Kingbright L-7104PBC) with a 2 ns risetime pulser was used. The LED was mounted at 2 cm distance in front of the input windows of two adjacent crystals, and geometrically arranged such that both crystals share approximately the same amount of light. The crystals were cooled inside a deep freezer to ca -25 ^{o}C. The APD gain was set to the nominal value of M=50, and the light pulse intensitiy was adjusted to correspond approximately to 400 ADC counts, corresponding to 2 GeV (see Figure 54.left) The resulting Root fit is shown in Figure 54

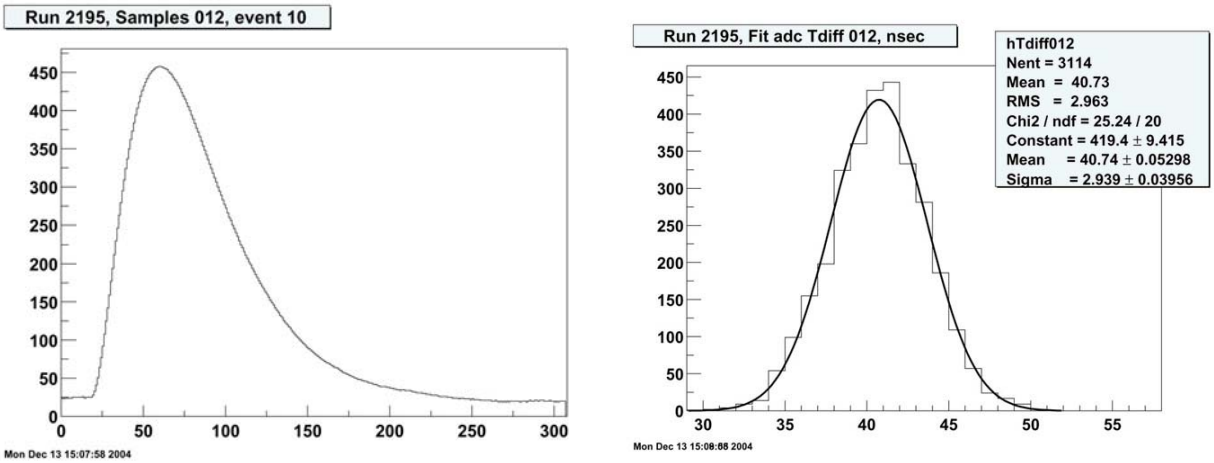


Figure 54 Differential timing resolution measurement of neighboring FEE shaper channels with a common blue light pulser. The Amplitude of the semi-gaussian CW shaper output (4 us peaking time) corresponds after pedestal subtraction to ca 2.1 GeV.

right.

With a sigma (A -B) = 2.94 ns

single channel timing resolution of the FEE cards at 2.1 GeV with a blue LED pulser

$$\Delta \mathbf{t} = 2.94 \text{ ns} \ / \ \text{SQRT}(2) = 2.07 \text{ ns} \quad @ \ 2.1 \text{ GeV}$$

This timing resolution constitutes a worst case, it could be improved by :

- different offline handling: binning, clock phase
- use of the rising edge
- increment of ADC sampling rate from 10 up 20 MHz
- use of particle-equivalent LED pulser
- improvement of sampling clock stability

6 Noise

The dynamic range as well as energy resolution is limited towards low energy by several noise sources which have been carefully minimized in the PHOS FEE electronics described in this document.

Ground noise, pickup noise and the digital noise are spurious noise sources to eliminate before the detector noise minimization via the shaper can become effective. The optimization via an elaborate grounding scheme and elimination of the digital ADC noise is discussed in the next chapter.The following chapter analyzes the noise characteristics of the second order shaper for the PHOS APD detectors.

The energy where the detector signal emerges from the noise sea (S/N=1) depends (for fixed light collection geometry and quantum efficiency) on crystal light yield and the APD gain.The crystal light yield has meanwhile reached a level of 12 photoelectrons/MeV whilst the PWO crystals which were available for all FEE tests had a 60% lower light yield[1].

The effect of noise increase with APD gain is globally shown in Figure 55 where the measured inclusive noise for 400 MeV equivalent LED pulses (RMS of ADC Maximum / Mean of ADC count) is plotted against the APD bias voltage.

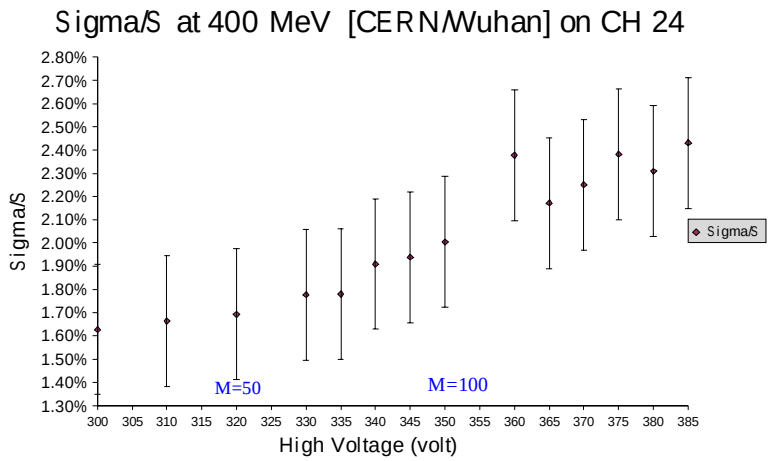


Figure 55 Measured noise dependence on Bias Voltage (APD gain)

1. Hence all measurements reported here can be considered worst case

The choice for a nominal[1]APD gain is also constrained by the CSP preamplifier gain, which produces a voltage step proportional to the input charge, proportional to the APD gain. With the maximum voltage of 1 Volt at the input of the ADC (for 1024 counts) , the only other remaining variable is the shaper gain. For the low energy range, the shaper gain needs to be number >1 in order to increase the S/N ratio.

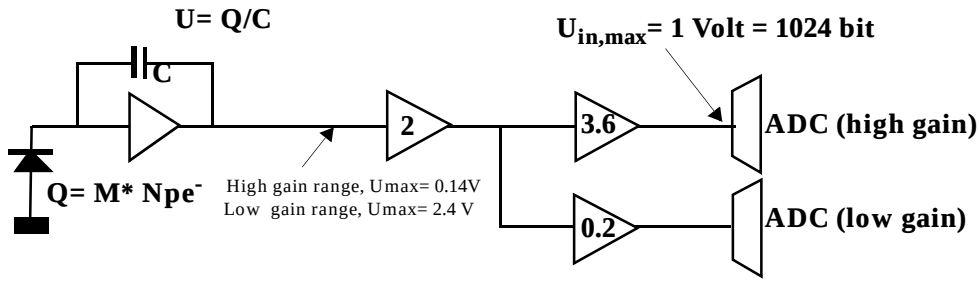


Figure 56 Relation between APD gain and CW shaper gain ranges.

As depicted in Figure 56, the maximum CSP Voltage[2] is 0.14 Volt for 5 GeV, and 2.4 Volt for the 80 GeV range. Hence the low energy shaper must apply a gain of 7.2 in order to place 5 GeV to 1024 bits of the ADC, the high energy shaper must apply a attenuation of 0.42. The cascaded signal amplification in the low energy range (high gain) improves the S/N ratio according to the well known formula below. N1 and N2 are the noise figures of the OP-Amps

$$N_{noise} = \sqrt{N1^2 + \left(\frac{N2}{K1}\right)^2}$$

Equation 10 Noise for cascaded amplifiers in CW shaper

and K1 is the gain of the first stage. For a gain less than one in the input stage, the noise increases. The positive gain K1= 2 in the input stage of Figure 56 reduces the noise N2 of the shaper amplifiers which is particularly important to minimize the noise level for the low energy range signals. Any S/N loss for the high energy range has no effect on energy resolution since S/N is by definition very high in the high energy range.

6.1 APD excess noise

The 8664-55 is a Si ADP from Hamamatsu with quite low noise characteristics. It has a excess noise factor F which can be approximated as F = kM +2 (McIntyre formula approximated for k < 0.1 and M > 20) where k, the ionization rate ratio for Si is very low k=0.0055 (see [9]):

1. nominal means that this value is used as default scaling factor for calculations. The real value may be changed, for example as function of the increasing PWO light yield
2. this results from M=50, 4 pe /MeV and C=1.2pF

The excess noise factor F is a measure of gain uncertainty in APD's, it quasi contributes to the stochastic term like Equation 11 by a variance in the electron multiplication. $F^{1/2}$ is the factor by which the statistical noise on the APD current exceeds that which would be expected from a noiseless multiplier on the basis of Poissonian statistics (shot noise) alone. F is largely temperature independent. The spontaneous gain fluctuations lead to the r.m.s. broadening of the signal given for N_{pe} photoelectrons by Equation 11

With the CMS measurement of Figure 57 the excess noise factor is F=2.27 for M=50 .

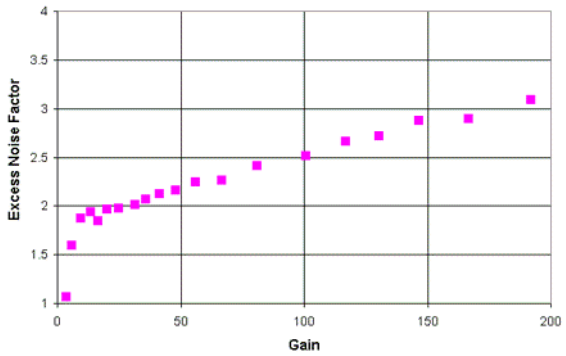


Figure 57 Excess noise measurement by CMS for 8664-55 for room temperature

There are two types of APD leakage current of which the total dark current is composed

$$I_D = I_{DS} + I_{DB}M$$

The surface current I_{DS} is ohmic , whilst the bulk current I_{DB} is subject to carrier multiplication and also radiation.

The APD contribution to the current noise (see Equation 4) is described as (see 6.4).

$$I_{DS} + I_{DB} \cdot M^2 \cdot F = I_{dark}$$

The excess noise is gaussian like noise with variance F-1 which broadens to the signal resolution. The lower limit of the stochastic term of the Energy resolution due to the Excess noise factor, can be approximated with Equation 11 by

$$\frac{b}{\sqrt{E}} = \sqrt{\frac{F}{N_{pe}}}$$

Equation 11 Single channel stochastic term approximation

where N_{pe} is the number of primary photoelectrons.

With 4 e- /MeV and F=2.27 @ (M=50), the lower limit of the single channel stochastic term b at 1 GeV can be approximated as 2.3 % GeV $^{1/2}$

6.2 Grounding scheme

For a 10 bit ADC with a single bit equivalence of 0.97 mV and a LSB quantization noise limit of 0.4 LSB which corresponds to 40 uV, any noise coupling from the digital and high voltage part to the analog part must be carefully avoided. For this purpose a ground plane layout was chosen following the scheme used in the TPC FEC card, which keeps analog and digital return currents completely separate and connects them only at a single common equipotential point close to the LV power connector.

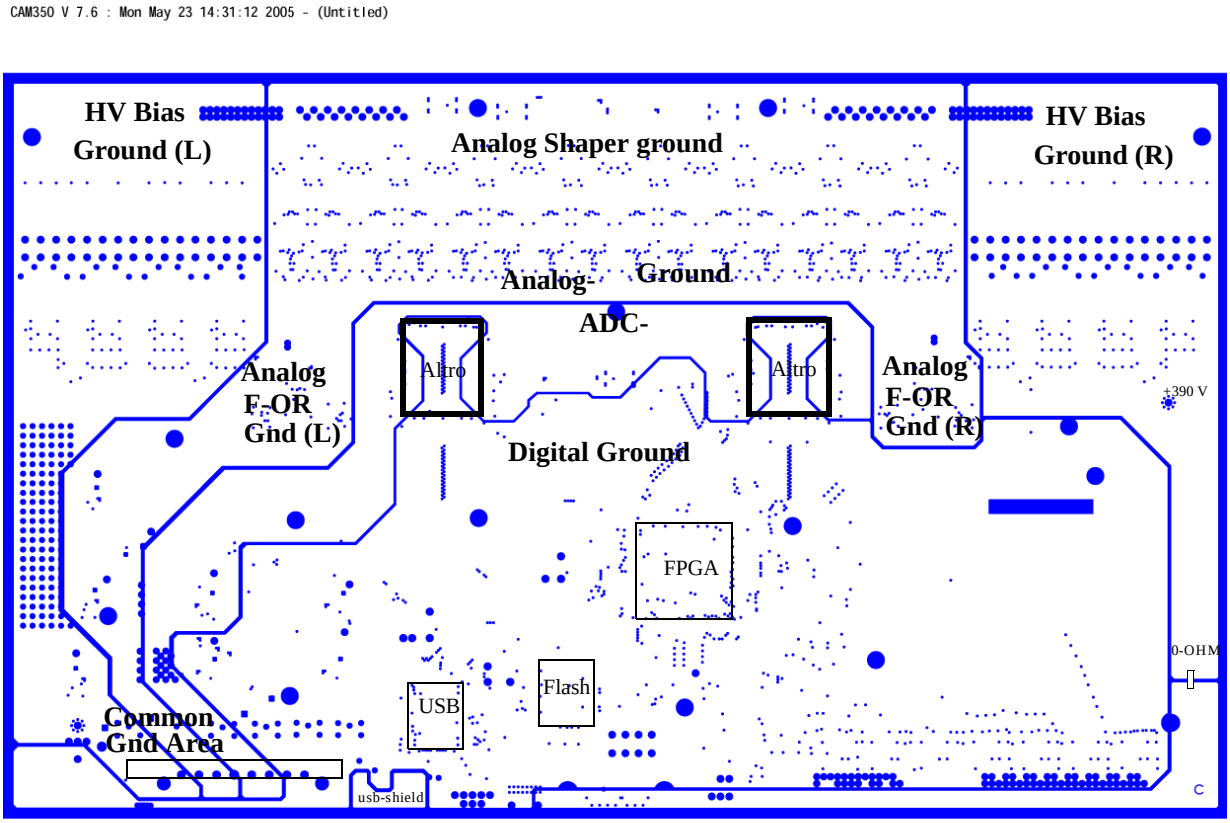


Figure 58 FEE card Rev 1.1 grounding scheme

The effect of noise coupling across hidden path's is show in the first measurements taken in the october 04 testbeam.

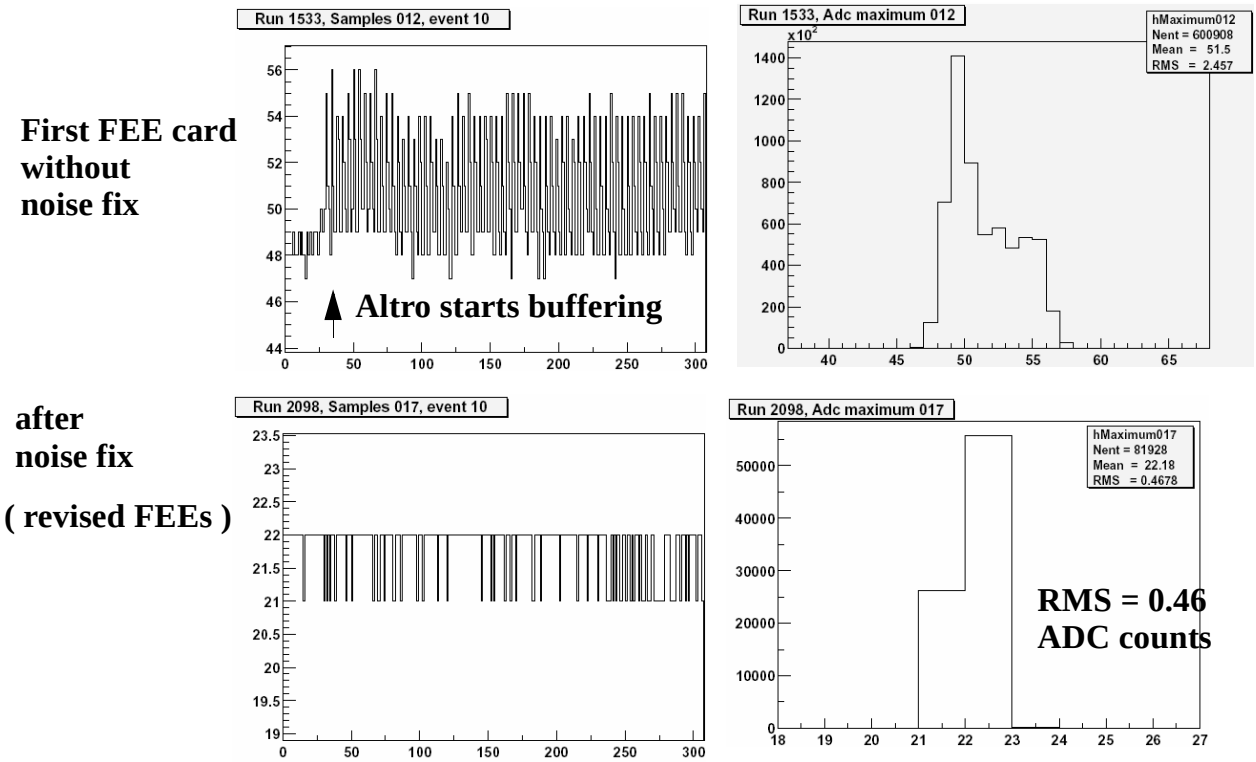


Figure 59 Digital noise coupling to analog part . **TOP:** RMS noise 2.5 ADC counts due to current coupling across reference voltage tree. **BOTTOM:** digital/analog noise couplings removed in revised FEE card prototype.

6.3 RMS noise

The RMS noise is measured offline from the variation of the pedestal noise (dark detector) over the N measurements.

$$\mathrm{Noise}_{\mathrm{rms}} = \frac{1}{N}\sqrt{\sum_i (y_i - \mathrm{Mean})^2}$$

The measurement of the RMS noise with APD detector connected includes the dark current noise and excess noise.

Figure 60 shows Root evaluations of RMS noise of FEE channels with and without detector for

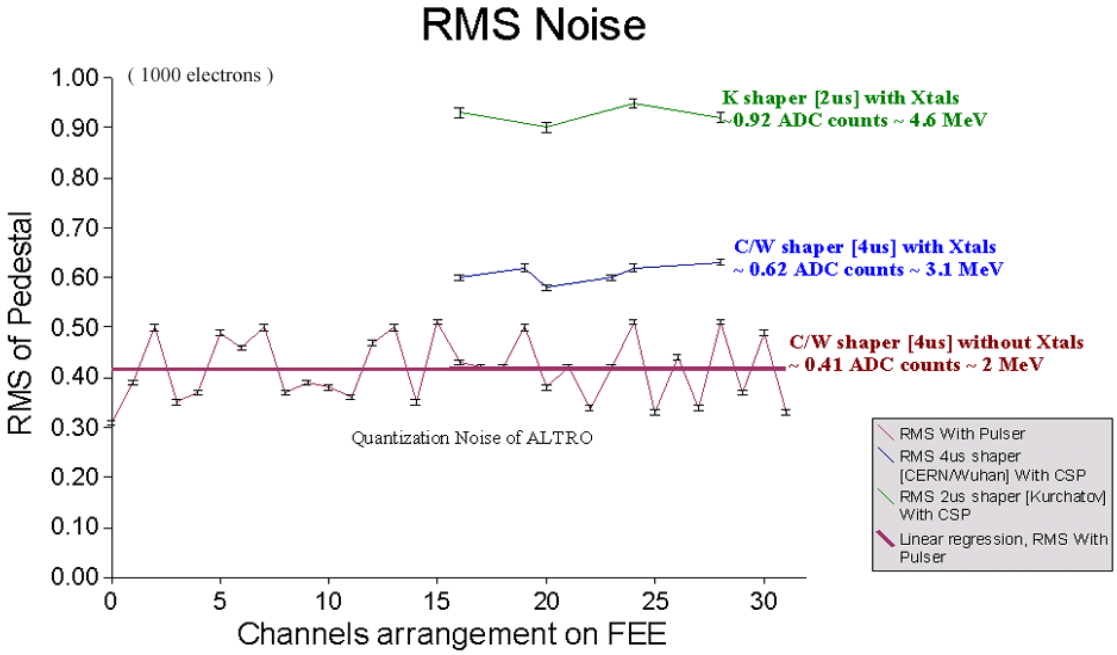


Figure 60 RMS noise (ADC counts / electrons) after shaper for 3 cases

both CW and K shaper. The RMS noise of 1 ADC count corresponds here to 1000 electrons since 1 ADC count corresponds to 5 MeV and because the APD light yield for M=50 is is 200 electrons per MeV.

a.) the RMS distribution over all 32 high gain FEE channels (no detector connected) results in 0.41 ADC counts, which is close to the Altro 10 bit ADC quantization noise.

b.) the RMS result from 6 channels with a 4 us CW shaper and APD connected at a corresponding APD gain of M=50 results in 3.1 MeV[1]

c.) the RMS result from 4 channels with 2 us K shaper and APD connected at a corresponding APD gain of M=100 results in 4.6 MeV.

The higher RMS noise for the K shaper is due to the double bandwidth bandpass and due to attenuation of the low energy signals (compare Equation 10)

1. Crosscheck for b: Since 1 ADC count corresponds to 970 uV, 0.62 ADC RMS noise counts correspond to 600 uV. The shaper gain is ~7, hence RMS noise corresponds to a CSP amplitude swing of 86 uV. From Figure 11 the CSP swing is 30 uV / MeV, hence the noise level is 86 / 30 = 2.8 MeV.

6.4 Shaper time constant

A general noise model of an amplifier reflects all noise sources to the input and representing them in an equivalent representation as Equivalent Noise Charge (ENC) which includes both the amplifier and the detector noise. There are in general 4 noise components:

1.) Current noise (parallel) : Shottky $2qI_d$ + Shunt resistor thermal R_p+ equivalent input current

2.) Voltage noise (serial) $4kTR_s$ thermal + Johnson noise at amplifier input

3.) 1/f noise (neglegible for PHOS)

4.) pileup noise (neglegible for PHOS).

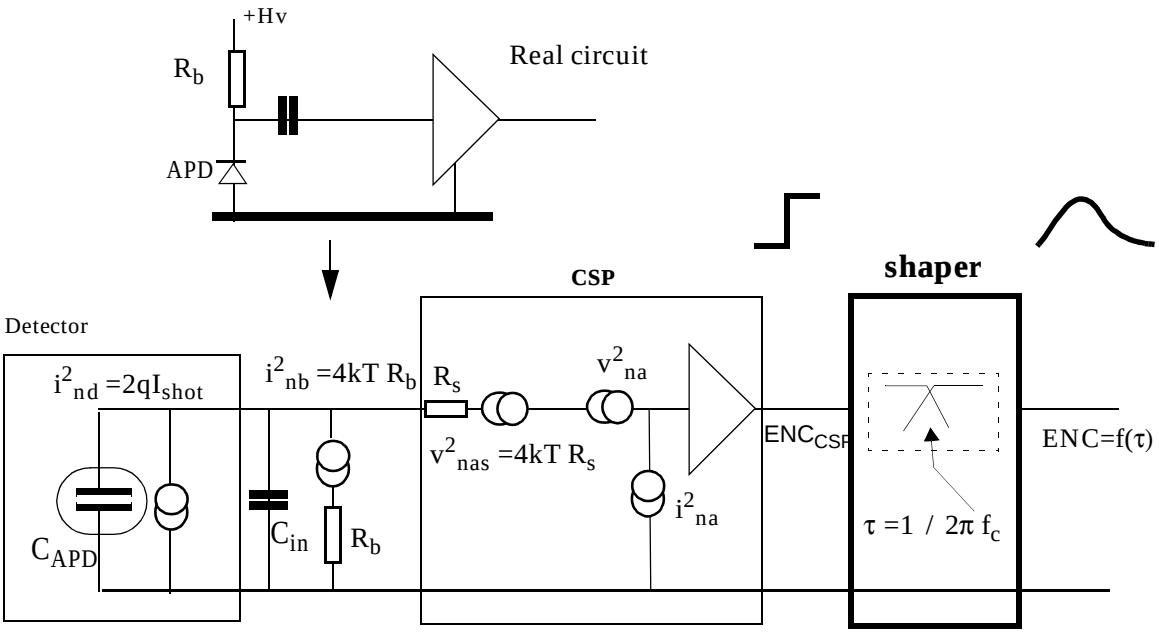


Figure 61 ENC noise analysis components

The shaper applies via its bandpass filtering a noise reduction which filters noise contributions (like pickup noise) to a minimum. The CSP noise charge represents the integral of noise over the full Fourier spectrum. The shaper further separates the charge signal information from the noise sea. The measuring of charge at the step amplitude of the CSP would be overdefined since the information contained in the plateau of the voltage step like in Figure 14 is not needed, it's fourier spectrum contains a spectum of noise components . The shaper produces from the charge signal a ballistic effect for the peak amplitude of a semi-gaussion output pulseshape. It can be proven that the peak amplitude is strictly proportional to the detector charge (see chapter

7) The pulseshape of a correctly designed shaper filter belongs to Gamma-n family of time functions where n is the order of the shaper.The bode diagram of the filter has a cutoff characteristic above the critical frequency f_c which is of negative slope n * 20dB / octave (see Figure 66). The critical frequency is related with an integrator time constant as $\tau = 1 / 2\pi f_c$

Low noise analysis for particle detectors [22] is a method to determine the minimum noise level of detector noise as function the integrator time constant τ of the shaper. The analytical equivalent noise charge ENC after the shaper and as function of the shaper time constant τ as depicted in Figure 61 is shown below Equation 20 [17]. The time constants τ for the successive differentiator and integrator stages of the shaper are equal. The minimum ENC defines the best shaper time constant.

$$ENC_{electrons} = \sqrt{\left(\frac{e^2}{8}\right)\left[\left(2q_e I_{Dark} + \frac{4kT}{R_p} + i_{na}^2\right)\cdot\tau + (4kTR_s + e_{na}^2)\cdot\frac{C_D^2}{\tau} + 4A_f\cdot C_D^2\right]}$$

Current noise ~τ independent C_D — **Voltage noise ~ $1/\tau$** and ~ C_D^2 — **1/f noise ~ C_D^2** independent τ

Equation 12 ENC after shaper as functiion of shaper time constant

T is the absolute temperature, C_D is the detector capacitance ($C_{APD} + C_{in}$), Rs an equivalent series resistor in the input stage, R_p an equivalent shunt resistor for C_D corresponding to the APD leakage current and the Bias Resistor (see Figure 61).

The parallel shunt resistor Rp can be calculated by taking i as dark current of the APD at 320

$$Rp = 4kT\frac{1}{2qi} = 43M\Omega$$

Volt and -20^{0}C as ~ 1 nA (see Figure 16 for room temperature 3.5 nA) and T= 250 Kelvin[1].

The serial noise (voltage noise) is produced by the Johnson noise in the input J-FET Transistor and can be described by a series resistor Rs whose resistance is inversely proportional to the input forward transconductance gm. For modern FET transistors the proportinal constant is a ~1.

$$Rs = \frac{a}{gm} = \frac{1}{gm} = 40\Omega$$

R_s can be calculated with the forward transmittance gm of the input transistor (see Figure 20)

1. The dark current is an exponential function of temperature I_d ~ exp(-aT)

The **input capacitance** of the CSP consist of 2 parts:

$$C_D = C_{apd} + C_{FET} = 100pF$$

The S8664-55 APD diode has ca 90 pF terminal capacitance at 320V (Figure 16), the input capacitance of the 2SK932 J-Fet is 10 pf.

For CR-n RC shapers the noise depencence on the shaper time constant τ is given by [18].

$$ENC = \sqrt{ENC_p^{\,2} + ENC_s^{\,2} + ENC_{\frac{1}{f}}^{\,2}}$$

which can be expressed is a general way by using serial and parallel noise figures Fs and Fp to separates the parallel and serial noise in three terms of which two depend in on the time

$$ENC^2 = \frac{4kT}{q^2 \cdot R_p} \cdot F_p \cdot \tau + \frac{4kT}{q^2} \cdot R_s \cdot F_s \cdot \frac{C_d^2}{\tau} + C_d^{\,2} \cdot const$$

Equation 13 Noise of CR-2RC shaper as function of integration time constant

constant τ of CR-nRC shapers. The third term represents the 1/f noise which is independent of τ. The manufacturing constants are not known to us for the J-FET transistor used in the CSP (2SK932) however since the 1/f contribution is constant, the minimum time constant τ is **independent** of this term. The noise figures Fp and Fs depend on the order n of the shaper and are listed in Table 1 .

Table 1 Noise figures Fs (serial) and Fp (parallel) [18]

n	**1**	**2**	**4**	**6**
Fs	0.92	0.84	0.99	1.16
Fp	0.92	0.63	0.45	0.36

When using CR-nRC type band-pass filters of order n, the low-pass slope is n*20 dB / octave (see Figure 66. For second order CW shaper, the low pass bode diagram Figure 66 shows correspondingly an attenuation of -40 dB/octave. The -3dB **cutoff frequency f_c** of the shaper is given by

$$f_c = \tau/(2\pi)$$

The time response function (shaped output) produced by such bandpass filters closely resembles a semi-gaussian shape of analytic form (see chapter 7) with n=2

$$\mathrm{Vout}(t)) = \left[\frac{n^n Q \cdot A^n}{Cf}\right] \cdot \left[\frac{t}{\tau_p}\right]^n \cdot e^{-n\frac{t}{\tau_p}}$$

In order to fine-tune the analytic form to almost identity with the pulseshape obtained by the electronics (see Figure 31 and Figure 32) one can finetune the relatice cutoff frequencies for the low pass and high pass.

By initially neglecting the 1/f noise as a constant, Equation 13 becomes for T= 248 K for n=2

$$\mathrm{ENC} = \sqrt{5.35 \cdot 10^{17} \cdot \frac{F_p}{R_p} \cdot \tau + 5.35 \cdot 10^{17} \cdot R_s \cdot F_s \cdot \frac{C_d^2}{\tau}}$$

(CR-2RC) shaper and the PHOS paramaters (Cd = 100 pF)

Figure 62 shows this ENC dependence on the shaper time constant for 3 values of the APD dark current Id (1 nA, 0.8 nA and 0.4 nA). The dark current is a strong function of temperature as seen in the Hamamatsu specification (see chapter 1.3) we simply extrapolate the dark current given for -20 C to values less than 1nA in order to see the dependence.

The ENC noise minimum bejond shaper time constants of 2 us is predominately a function of the current noise of the APD, shown here for 3 cases of the dark current More than 2 us is

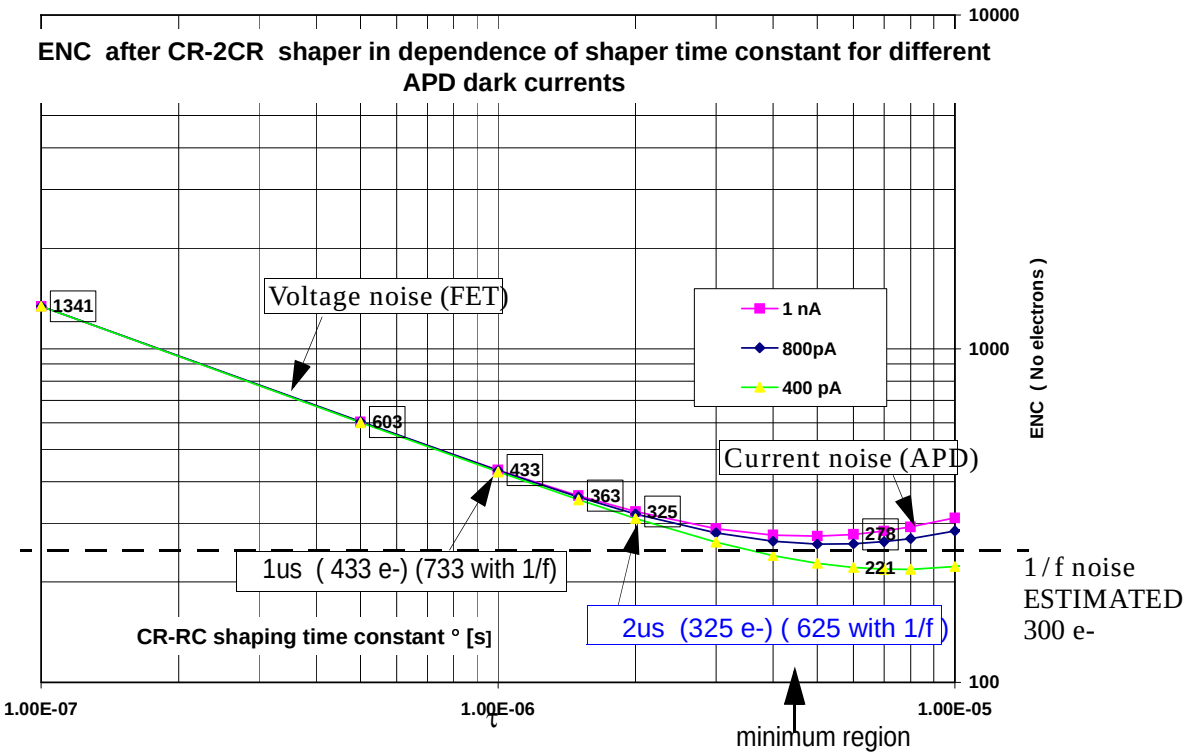


Figure 62 Calculated noise for PHOS APD/CSP frontend after CR-2RC shaper in dependence of shaping time constant τ.

however not adequate due to the increasing pileup of pulses the longer pulses.

Below 2 us, the Voltage noise increases. Figure 62 shows the calculated ENC noise level for the second order CR-2RC shaper for two choices (τ= 2, 4 us) .

By addition of an estimated 1 / f noise contribution of 300 electrons, though this is a crude guess in view on the 1 / f dependencies for shapers as described in [16], the estimated ENC noise levels after the shaper are shown in Table 2

Table 2 Two choices of 2nd order shaper time constant for CW shaper and noise with etector

shaper constant τ	electrons without 1/f noise	with **estimated** contribution from 1/f noise
τ= 2 us	325	625
τ= 1 us	433	733

The peaking time of the time response pulse is defined by

$$\tau_{peak} = n \cdot \tau = 2\tau$$

A compromise between low noise and pileup reduction is a **shaping time constant of τ= 2 us and correspondingly a peaking time of τ_{peak}= 4us** for the semi-gaussian shaper of second order. (see Figure 15 and Figure 31)

The RMS noise measured with this choice for the CW shaper has been determined as 0.62 ADC counts or 620 electrons (see Figure 60) as compared to 0.92 ADC counts (920 electrons) with the τ= 1 us , τ_{peak}= 2us setting of the K-shaper.

Note1: The fact that the τ= 1 us K shaper measures with 920 electrons more noise than expected is due to it's signal attenuation factor of K1 < 0.4 which increases the noise according to Equation 10

Note: The shaper time constant τ=1us for the CW shaper represents a compromise with the expected better timing resolution with shorter time-constants (wider bandpass). The FEE version V1.1 will initially be produced with both time constants 1 and 2 us (corresponding to peaking times 2 and 4 us) in order to determine the best compromise between low noise and best timing resolution.

7 Shaper

The CW shaper is a bandpass for the voltage step signal of the CSP pre-amplifier, suppressing noise contributions from the low and the high frequency noise sea available at the CSP level. It consists of a series of 1st order high-pass (differentiator) and n^{th} order low-pass (integrator) of the same time constant. The order of the shaper corresponds to the noise cutoff power, a first order shaper for example has the cutoff power of an RC filter with -20 dB slope per octave. An order-n shaper performs as n* -20db, i.e with better noise cutoff characteristics. For example the total ENC noise for first order shapers is generally 12.5 % higher than for second order shapers. For the PHOS FEE electronics, the best economical compromise for a discrete logic shaper implementation was n=2 (second order).

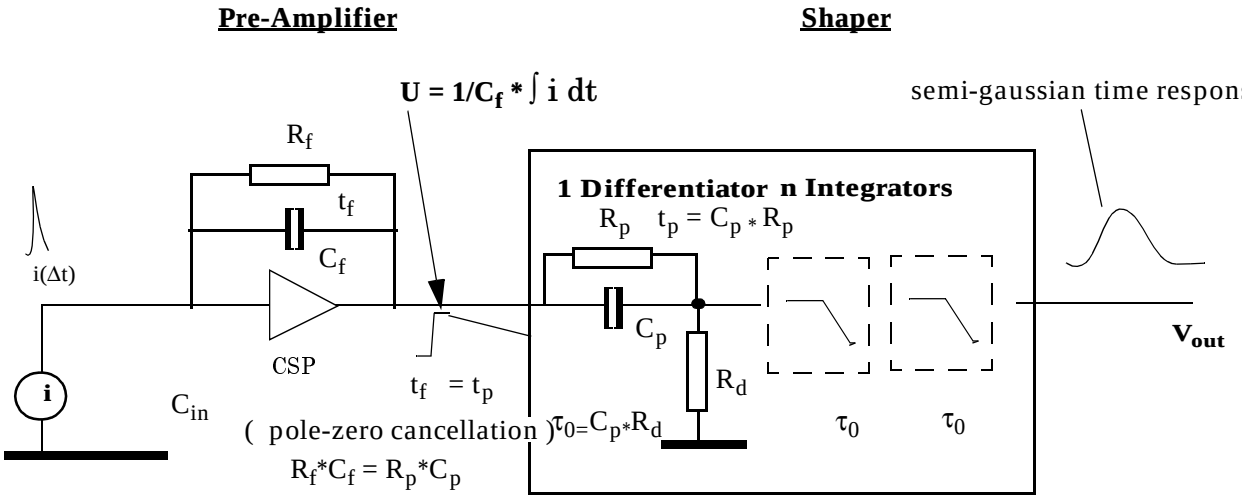


Figure 63 Semi gaussian shaper of type CR-2RC with pole-zero cancellation

With ($s = i\omega$) the Laplace analysis is the standard approach to calculate shaper transfer functions H(s). The transfer function for a step function s , followed by a semi-gaussian shaper as depicted in Figure 63 is given by [16]

$$H_{shaper}(s) = s\left[\frac{\tau_0}{1+s\tau_0}\right]\times\left[\frac{A}{1+s\tau_0}\right]^n$$

step function — CR differentiator 1-st order — RC integrator n-th order

Equation 14

where τ_0 is the time constant of both the differentiator and the integrators, and A is the gain of the integrators and n is the order of the semi-gaussian shaper. The step function is represented by the operator s

By defining the peaking time of the output pulse as

$$\tau_{peak} = n \cdot \tau_0 = 2\tau_0$$

the inverse Laplace transform results in a semi-gaussian pulse shape of form

$$V_n(t) = \left[\frac{n^n Q \cdot A^n}{C_f}\right] \cdot \left[\frac{t}{\tau_p}\right]^n \cdot e^{-n\frac{t}{\tau_p}}$$

giving a peak amplitude V_{max} at τ_{peak}

$$V_{max} = \frac{Q \cdot A^n \cdot n^n}{C_f \cdot n! \cdot e^n}$$

For PHOS, the shaper implementation with discrete logic is cost and real estate- critical, hence the optimal choice was n=2 since dual integrators can implemented with a single stage of operational amplifiers.

For a second order shaper the time response function is:

$$V_{2nd}(t) = \left[\frac{4Q \cdot A^2}{C_f}\right] \cdot \left[\frac{t}{\tau_p}\right]^2 \cdot e^{-2\frac{t}{\tau_p}}$$

Equation 15 second order Gamma function for PHOS

The **complete** transfer function has to be extended to include the CSP:

$$H_{CSP+shaper}(s) = s \times \left[\frac{1}{1 + \frac{1}{R_f \cdot C_f}}\right] \times \left[\frac{\tau_0}{1 + s\tau_0}\right] \times \left[\frac{A}{1 + s\tau_0}\right]^n$$

Equation 16 Complete transfer function for CSP and Shaper

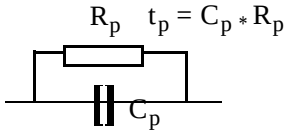
The new term effectively produces an undershoot in the semi-gaussion time response.

The pole zero-cancellation consist in adding a RC network whose Laplace term cancels with the new term, hence of a network operating as

$$1 + \frac{1}{R_f \cdot C_f}$$

Equation 17 Pole-zero term

This is simply an RC network as shown below:



between the CSP and the shaper (see Figure 63). The time constant $t_p = C_p * R_p$ should theoretically be equal to R_f*C_f (= 100 us), in practise, it has to be determined by experimenting.

For the CSP, the empirical pole zero time constant was determined as 67 us. With this, the complete CSP-pole-zero-Shaper (n=2) chain produces a semi-gaussian output with undershoot < 1 % over the full high gain range (compare Chapter 3)

7.1 Calculation of the 2nd order Bessel filter values

The second order filter requires implementation of a dual integrator stage. This is feasible with a single operational amplifier with multiple feedback architecture (MFB), shown in Figure 64

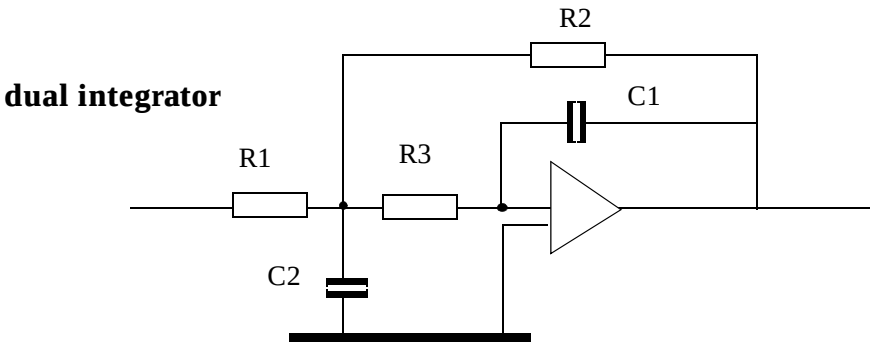


Figure 64 Second order low pass implemented with Multi-Feedback MFB.

It's transfer function can be expressed [8] as a function of frequency (Equation 18)

$$H(f) = \frac{-K}{\left(\frac{f}{fc \cdot FSF}\right)^2 + \frac{1}{Q} \times \frac{if}{FSF \cdot fc} + 1}$$

Equation 18 Transfer function of dual integrator MFB architecture

showing that for the frequencies above and below the -3dB cutoff frequency fc two cases apply

- f<<fc H(f) ~ K (constant gain K)
- f>>fc H(f) ~ -K * (FSF * fc / f)^2 (attenuation at square of frequency ratio)

The attenuation above f_c with $1/f^2$ corresponds to a second order low pass filter with an attenuation of -40 dB per octave. FSF is the frequency scaling factor for the -3dB cutoff frequency f_c. Q is a quality factor.

In general, the Laplace transform for MFB integrators have the polynomial form

$$H(s) = \frac{K}{1 + as + bs^2}$$

Equation 19 Laplace form of MFB architecture with polynomial

The **Bessel** type of transfer functions other than (Tschebycheff or Butterworth, see Figure 65) have a maximally flat response and group delay at f<<fc, hence they can replace RC-based integrators.

The Bessel filter of second order has a quality factor of Q=0.5773 and a frequency scaling factor of FSF =**1.2736**.

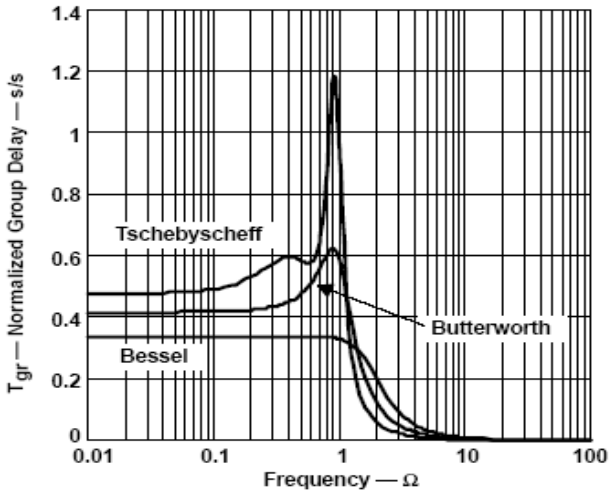


Figure 65 Comparison of Bessel filter types with other filters

For Bessel filters the coefficients[21] of the transfer function are with $\omega_c = 2\pi f_c$

- $K = R_2/R_3$ (gain for f << fc)
- $a = \omega_c C_1 (R_2 + R_3 + R_2R_3/R_1) =$ **1.3617**
- $b = \omega_c^2 C_1C_2R_2R_3 =$ **0.618**

Given values for C1 and C1 which satisfy the condition

$$C_2 \geq C_1 \cdot \frac{4b \cdot (1-K)}{a^2}$$

With this, the resistors can be calculated as The -3dB cutoff freqency f_c is

$$R_2 = \frac{aC_2 - \sqrt{a^2 \cdot C_2^2 - 4bC_1C_2 \cdot (1-K)}}{4\pi f_c \cdot C_1C_2}$$

$$R_1 = \frac{R_2}{-K}$$

$$R_3 = \frac{b}{4\pi^2 f_c^2 \cdot C_1C_2R_2}$$

Equation 20 Resistor formulas for shaper in dependence of cutoff frequency

$$fc = \frac{1}{2\pi \cdot \sqrt{R_2 \cdot R_3 \cdot C_1 \cdot C_2}} \cdot \frac{1}{FSF}$$

For the optimal PHOS shaper time constant (see 6.4) of $\tau 0 = 2us$ the components are to be calculated for the -3dB cutoff frequency of the Bessel filter:

$$f_c = \omega_c / 2\pi = 1/(2\pi * \tau_0) = 79.5 \text{ kHz}$$

7.2 Dual gain CW shaper RC values

The shaper applies a gain such that the maximum CSP voltage (for a constant APD gain) fits in the full range ADC window of 1 Volt input (= 1024 bit). Based on a nominal light yield of 10 obtained with PHOS crystals and APD gain =50 (see Chapter 1.1.4) the following two ranges and gains were implemented (compare chapter 4.1):

High gain : 5 MeV - 5.12 GeV: U_{csp} = 137 uV - 0.1407 Volt <u>shaper gain = 7.2</u>

Low gain : 80 MeV- 81.92 GeV : U_{csp} = 2.19 mV - 2.245 V <u>shaper gain = 0.45</u>

The CW shaper was developed (see PSCC-5 shaper in [15]) for optimal noise performance (chapter 6.4) as successive RC differentiator and dual Bessel integrator stages of common cutoff frequency and with gain ratio of 16 for low-energy and high energy ranges. The RC differentiator is combined with a pole-zero cancellatio, tuned for the CSP (see chapter 3). The output stage to the Altro ADC is fully symmetrical and contains a high frequency RC noise filter.

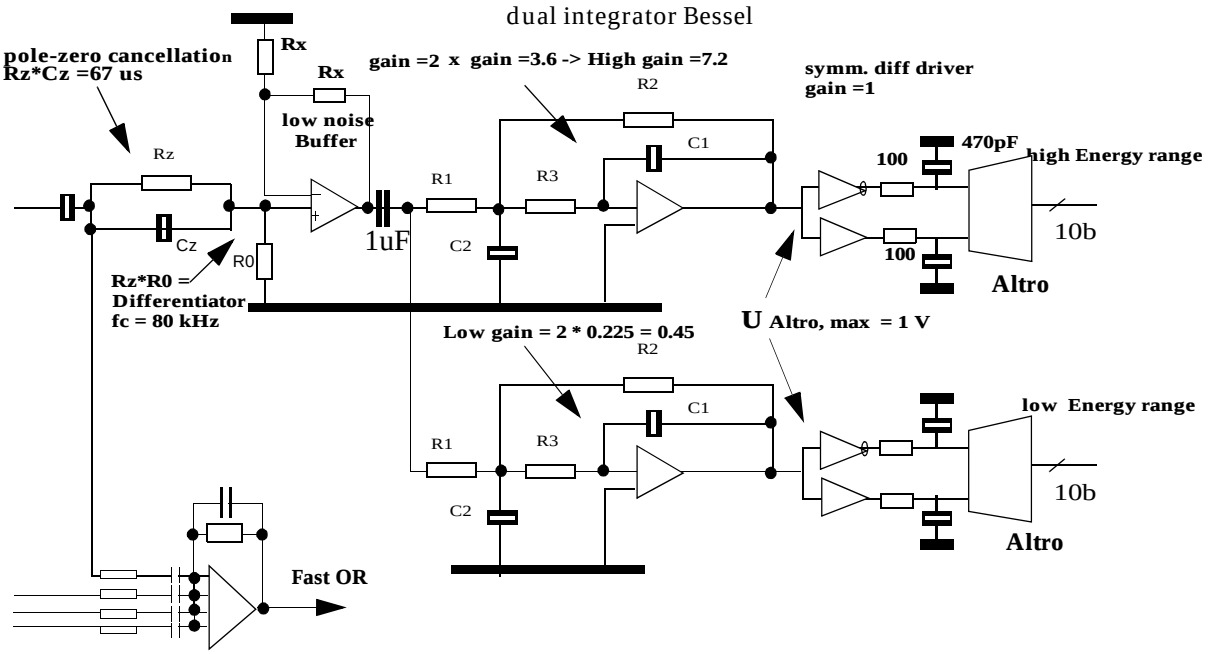


Table 3 shows the results obtained with the Bessel calculation for the CW shaper RC components for the example of 4 us peaking time and gain ratio 1 / 16. Rz has been determined empirically as the best non-overshoot value of the pole zero cancellation.Rz corresponds with Cz like shown in Equation 17. For a change in the bandpass frequency (or peaking time) of the shaper, R0 must be adjusted to correspond with Cz to the new bandpass value. All other values R1..3, C1..2 can be calculated with the method described in 7.1

Table 3 RC values for CW shaper 4 us and 2 us peaking time (buffer gain = 2, gain ratio =16)

CW Shaper	R1	R2	R3	C1	C2	Cz	Rz	R0
gain 2*3.35 τ_{peak} =4.1 us	649	4.42 k	1.78 k	150pF	2.2 nF	470 pF	143 k	9.1 k
gain 2*0.21 τ_{peak} =4.06 us	10.5 K	4.22 K	5.9 K	220 pF	470pF	470pF	143 k	9.1 k
gain 2* 3.35 τ_{peak} =2.04 us	681	4.87 k	1.96 k	68 pF	1000 pF	470 pF	143 K	4.22K
gain 2*0.21 τ_{peak} =2.04 us	4.02 K	1.69 K	5.36 K	150 pF	470 pF	470 pF	143 k	4.22 K

The BODE diagram corresponding to the CERN / Wuhan shaper with 4 us peaking time and

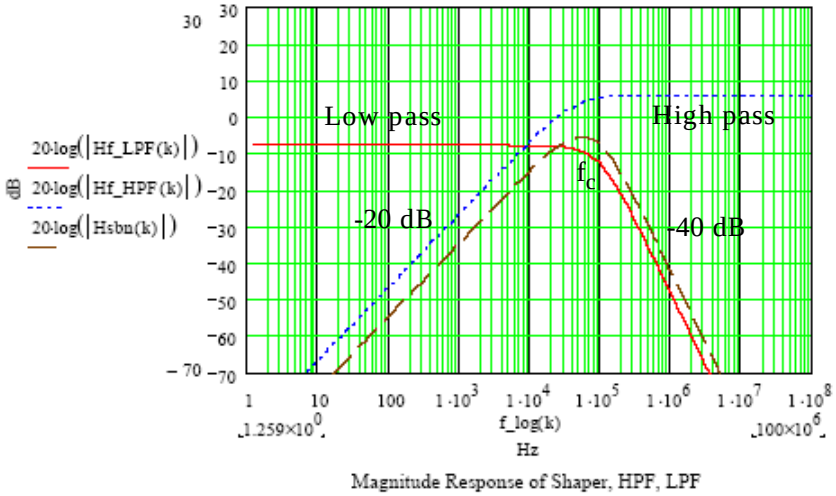


Figure 66
CERN/Wuhan shaper frequency response

with gain 2*0.21 is shown in Figure 66.

The relative oscilloscope pulseshapes for step pulse input to the second order CW shaper with 2 us and 4 us peaking time (implemented with the RC values of Table 3 are shown in Figure 67.

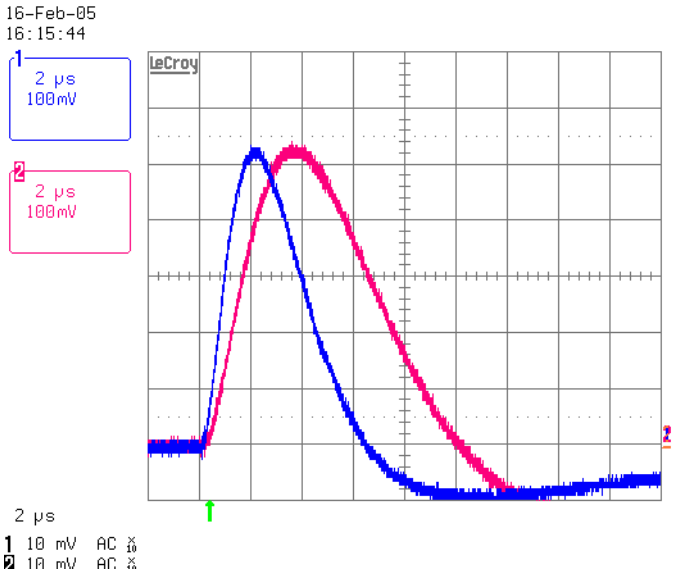


Figure 67 oscilloscope picture of CW shaper output with 2 and 4 us peaking time (semi-gaussian)

The undershoot is due to the fact that the measurement was taken without CSP connected, hence the pole zero-network creates an undershoot.

8 PHOS Control and Monitoring (PCM)

The PCM controller[1] on the FEE cards are state machines which respond as slave device to the communication protocol of the Readout Control Unit (RCU). For this purpose the PCM implements the I2C-like protocol of the 26 line GTL bus which connects all FEE cards with the control domain of the RCU (see Figure 57).

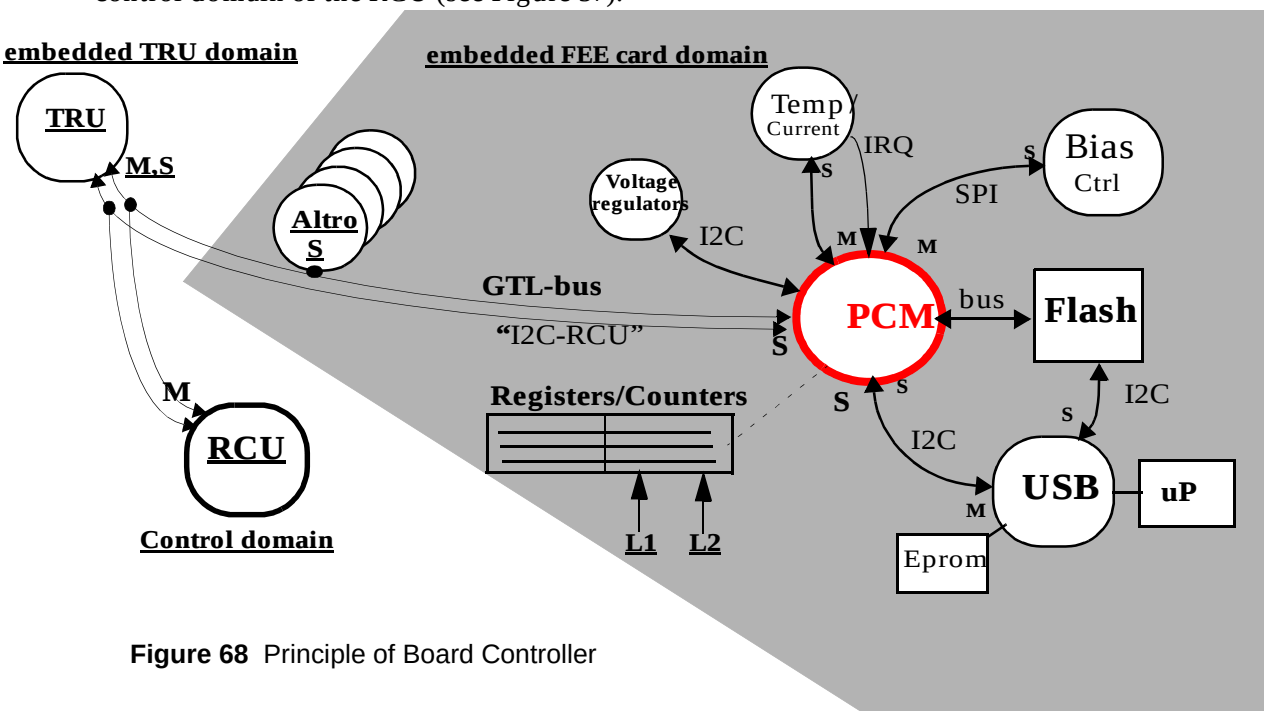


Figure 68 Principle of Board Controller

The PCM either mirrors the status of values in a set of monitoring registers or it uses a register to update a setting. It also implements specific commands like Reset.

The board control logic on the PHOS FEE card was based on the BC on the TPC FEC card. An addition for the PHOS BC are 32 registers for the APD bias setting and the Motorola SPI bus for the APD bias regulation. For local board diagnostics (without RCU), both the FEE and the TRU are equipped with a single-chip USB port, which maps into the I2C bus on the FEE card. In this way, all resources which are available to the RCU via I2C can be used also via a USB connection to a local PC. The USB controller on the FEE card is used for local servicing via a standard PC. It also serves a micro-processor which is checking the board controller alive status. In case of a misfunctioning boardcontroller FPGA, it can re-initialize it's configuration from a Flash memory.

1. previously called Board Controller, renamed PCM to avoid confusion with the TPC Board controller

The FPGA-based PCM logic structure is shown in Figure 69, containing:

- communication logic with the RCU
- information about temperatures, voltages and currents
- a set of counters and registers.
- controls individual voltages of each APD

The communication between the RCU and the PMC is made through either the RCU-I^{2}C protocol or the ALTRO bus, with priority given for the RCU-I^{2}C over the ALTRO protocol..

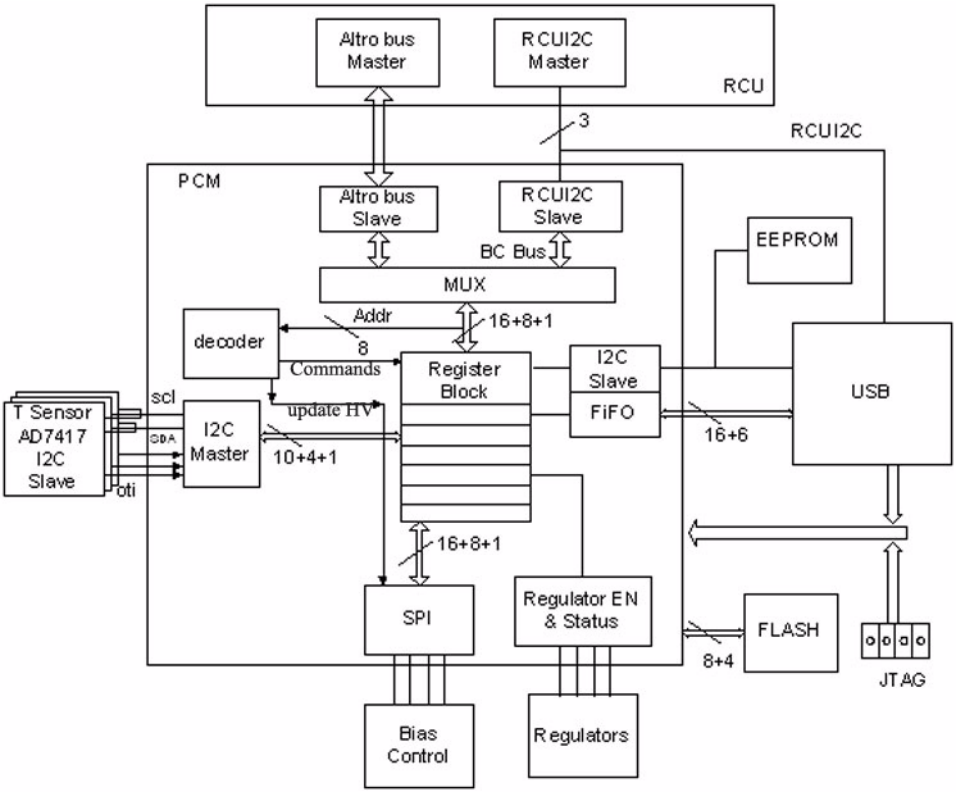


Figure 69 Details of Phos Control and Monitoring logic (PCM)

Through it's protocols the RCU can:

- Configure the registers with threshold values for setting up temperatures, voltages and currents limits.
- Send control flags in order to clear counters, reset the ALTROs, reset of the PCM, and control the AD7417 Voltage digitizer.
- Control the APD BIAS by loading the internal registers on the PMC which are then transmitted via SPI to the BIAS controller.

The PCM can inform the RCU of:

- Critical voltages, currents, or temperatures that are acquired / digitized and stored on the AD7417 device The communication between the PMC and the AD7417 is via RCU-I^2C.
- Values of counters regarding the number of level-1 and level-2 triggers, sampling clocks, and data strobe. With this feature the RCU can be certain that the time domain of the collected data is the same on all FEEs Digital Readout
- High voltage settings of each APD

8.1 USB diagnostic port

The Cypress USB2.0 chipset EZ-USB FX2 is integrated on the FEE card as programmable USB peripheral for diagoniistic use. It contains a 8051 microprocessor with RAM based architecture allowing for programmable reconfigurations. It is connected via it's peripheral lines to the

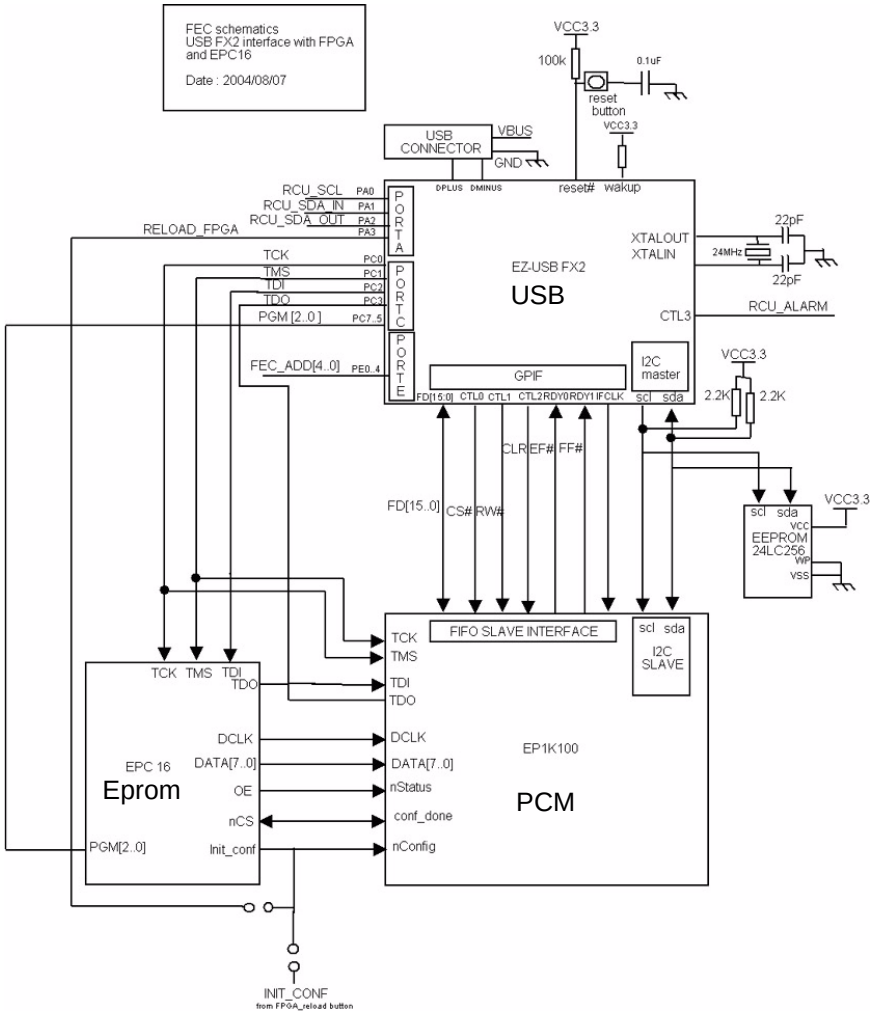


Figure 70 Schematical overview of the USP control port on the FEE card. A 480 Mbit USB 2.0 controller

PCM FPGA's FiFo port, allowing to transfer data (under 8051 control). A particular feature is that the Eprom of the PCM can be programmed via the USB port C. A detailed thesis report [25] on the USB port on the FEE card is available under http://cern.ch/hmuller/usb4fee.htm.

9 ADC and digital logic

The connection overview between the Altro digitizers and the RCU is depicted in Figure 71. The RCU's bus interface uses two protocols to address and control both the ALTRO's and the PCM logic: parallel Altro Readout bus and serial RCU-I2C bus. The RCU's can geographically address individual ALTRO chips (see Paragraph 2.4) in order to setup their internal registers or to readout event data.

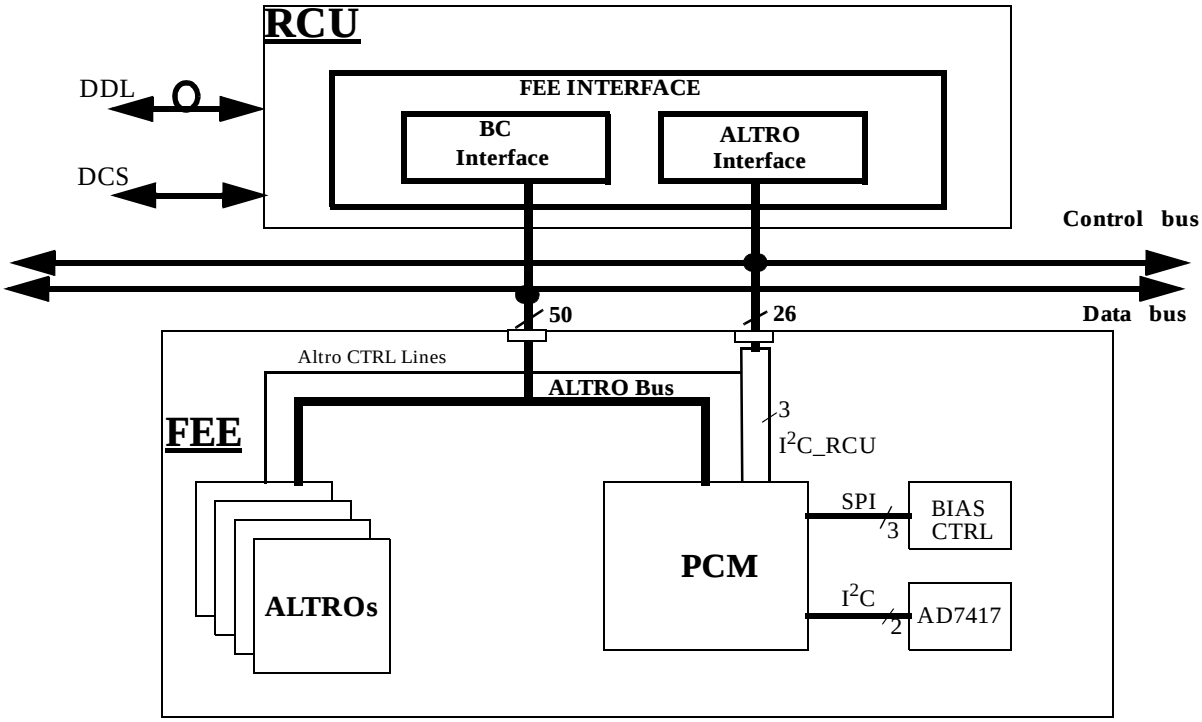


Figure 71 Readout bus hierarchy between RCU master and FEE slaves

9.1 Altro ADC

The ALTRO-16 chip[1] [3] of the ALICE TPC is also used by PHOS used for digitization and processing of the semi-gaussian pulseshapes after the FEE shaper describend in chapter 2.2 . The Altro chip contains sixteen 10 bit ADC'c, each followed by a signal processing chain and up to 8 event-buffers. The Altro chip is produced by ST Microelectronics, based on a 0.25 um HCMOS process, consisting of ca. 6 million transistors and sold in a TQFP-176 package. With

1. produced by ST Microelectronics

a supply Voltage of 2.5 Volts it's power consumption is 15 mW per ADC channel. Shown in Figure 72 is one of its sixteen 10-bit ADCs blocks, follwowed by a processing chain and the Multi-event buffers. The common control logic contains registers, the readout bus interface and the trigger manager.

The Multievent buffer (1040 * 40 bit) can be partitioned into 4 or 8 blocks.

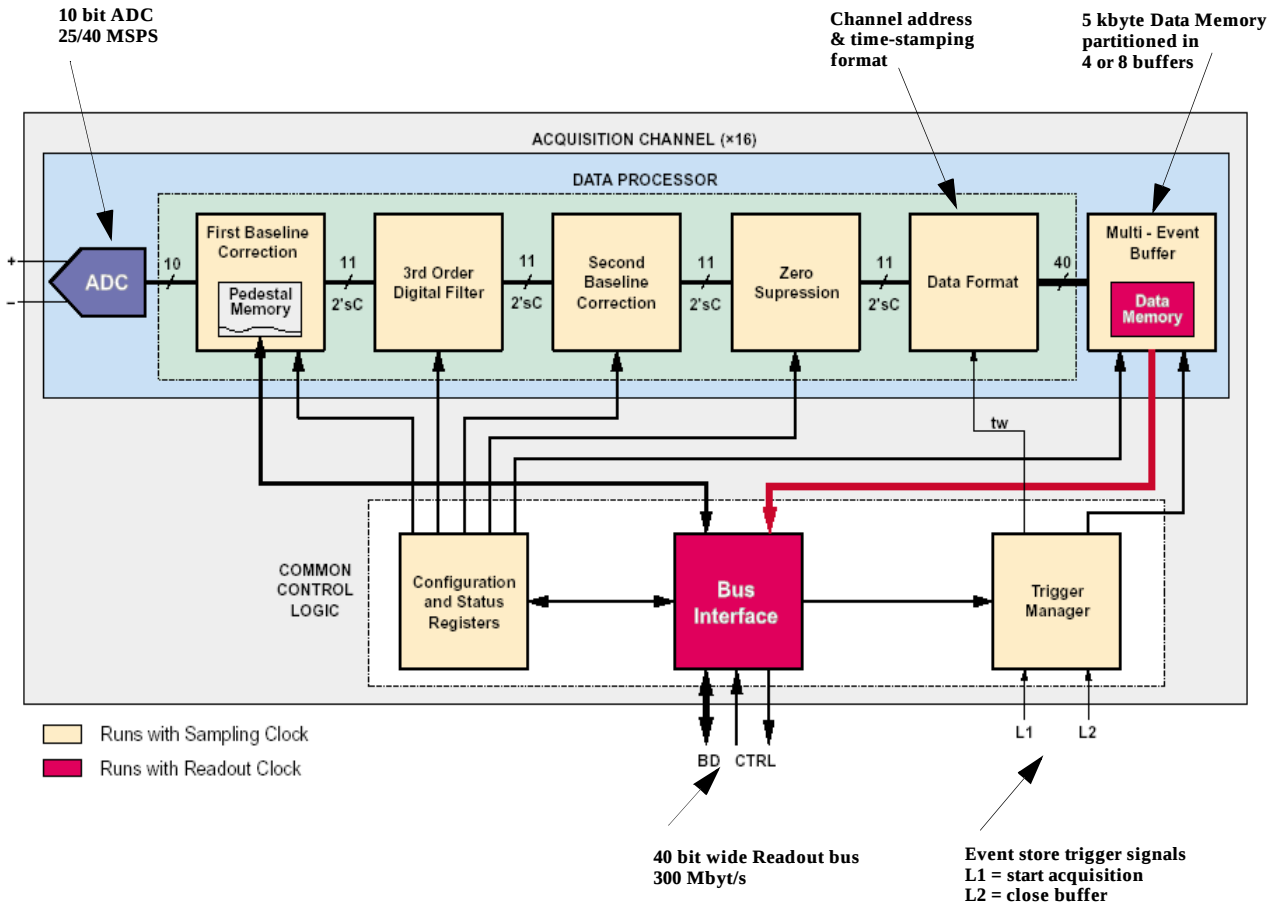


Figure 72 Block diagram of the Altro-16 chip (From Altro Manual) showing on of 16 ALTRO channels.

The data readout requires a GTL interface to the LVTTL interface of the Altro chip. This is implemented using GTL transceivers in an ALTRO compatible mode, i.e. the GTL drivers GTL16612DGG are operated at 2.5 Volt Altro supply voltage.

The A/D converters are macro blocks which are based on the TSA1001 made by STMicroelectronics which can be clocked up to a maximum of 40 MHz. At 10MHz sampling frequency we have 9.7 effective number of bits (ENOB) as shown in Figure [73]. The converted data is fed into a 6 stage pipeline of data processing which can perform a baseline subtraction, a tail cancelation filtering, adaptive baseline correction, and zero suppresion. The output of the filter inputs into an embedded multi-event buffer.

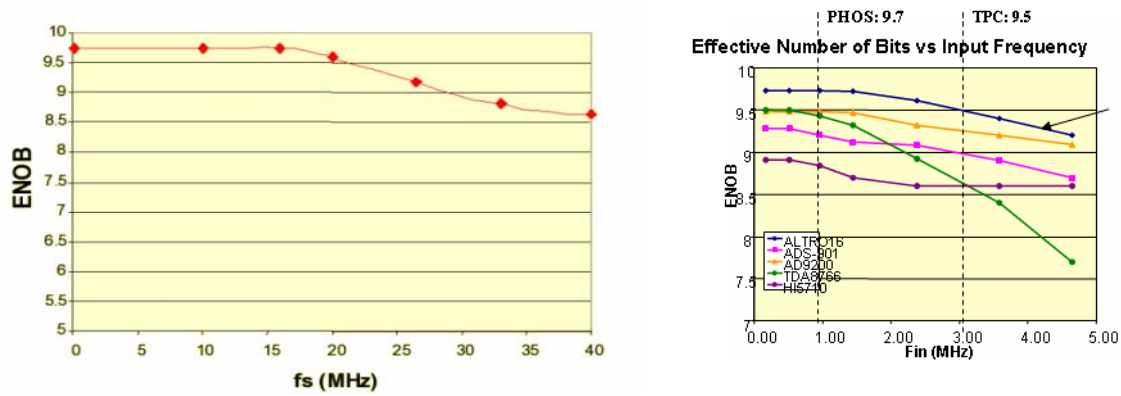


Figure 73 Left: Effective Nr of bits vs sampling frequency of the ALTRO chip [27].
Right: Effective Nr of bits vs input Bandwidth (shaper) for several ADC's and Altro [28]

The sampling rate is in principle freely selectable (at the RCU level) between the Nyquits frequency = 2* input bandwidth and a maximum sampling frequency of 20 MHz. With a shaper bandwidth < 0.5 MHz, PHOS applies overclocking[1] above the Nyquist frequency of 1 MHz. All 2004 tests with the FEE cards applied a sampling clock of 10 MHz.

9.1.1 GTL readout and control bus

Each TRU domain consists of 14 FEE cards and one TRU card all sharing a common GTL data and control bus which is mastered by an RCU branch. The data bus is a bidirectional, 40 bit data bus, clocked at 40 MHz[2] for a nominal bandwidth of 160 Mbyte/s. The control bus is a mostly uni-directional bus for 16 control signals, also including the differential sampling clock in LV-PECL standard. The signal names and pinouts of the two GTL buses are shown in Appendix 3 The connection plan between the RCU master and the 15 modules of one TRU domain is depicted in Figure 74.

1. Overclocking combined with averaged binning may increase the effective number of bits, provided that the noise power spectrum at the ADC input is gaussian like. So far this has not been applied to our measurements.

2. potentially on the new RCU, the data clock can be increased to 50 MHz for a bandwidth of 200 MByte/s matching the DDL bandwidth.

The GTL+ bus consists of 40 cm flat cable and 60 cm PCB strips, and is terminated on both the RCU and the GTL strip extremes. A detailed interconnection plan of one TRU domain is shown in Figure 97 and the connectors and cables are specified in 14.1 .

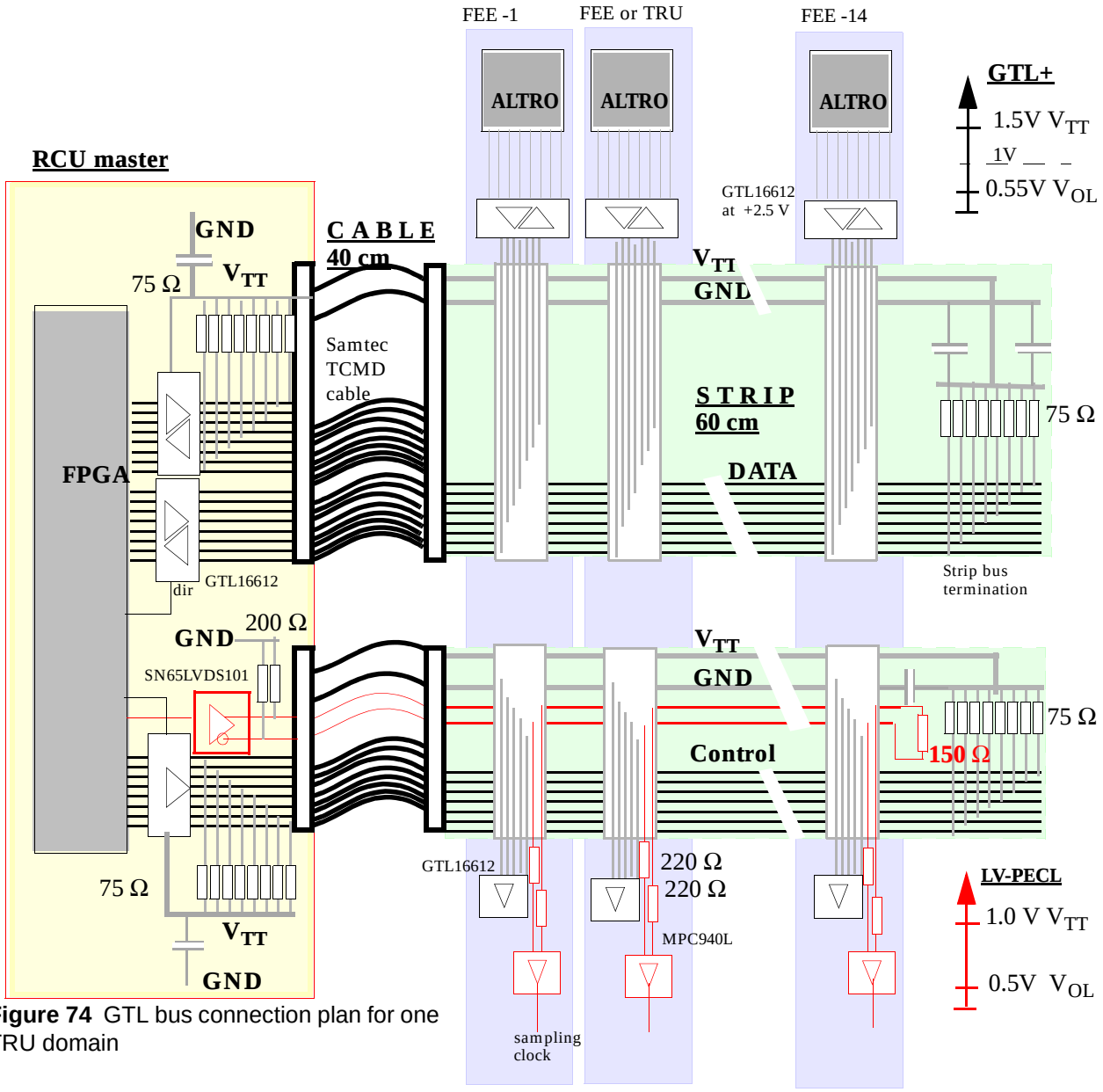


Figure 74 GTL bus connection plan for one TRU domain

The detailed bus dimensions are shown in Figure 75. The pinout, connectors and termination are equivalent with the GTL bus strips of the TPC. The PHOS GTL bus strips are re-engineered for a regular and parallel FEE connector spacing of 45.4 mm with one central TRU module connector at half space. The geographical address coding is shown in Figure 37. A 4-layer PCB thickness of 700 um is used. A photo of the GTL connectivity with FEE cards in a test crate is shown in Appendix 14

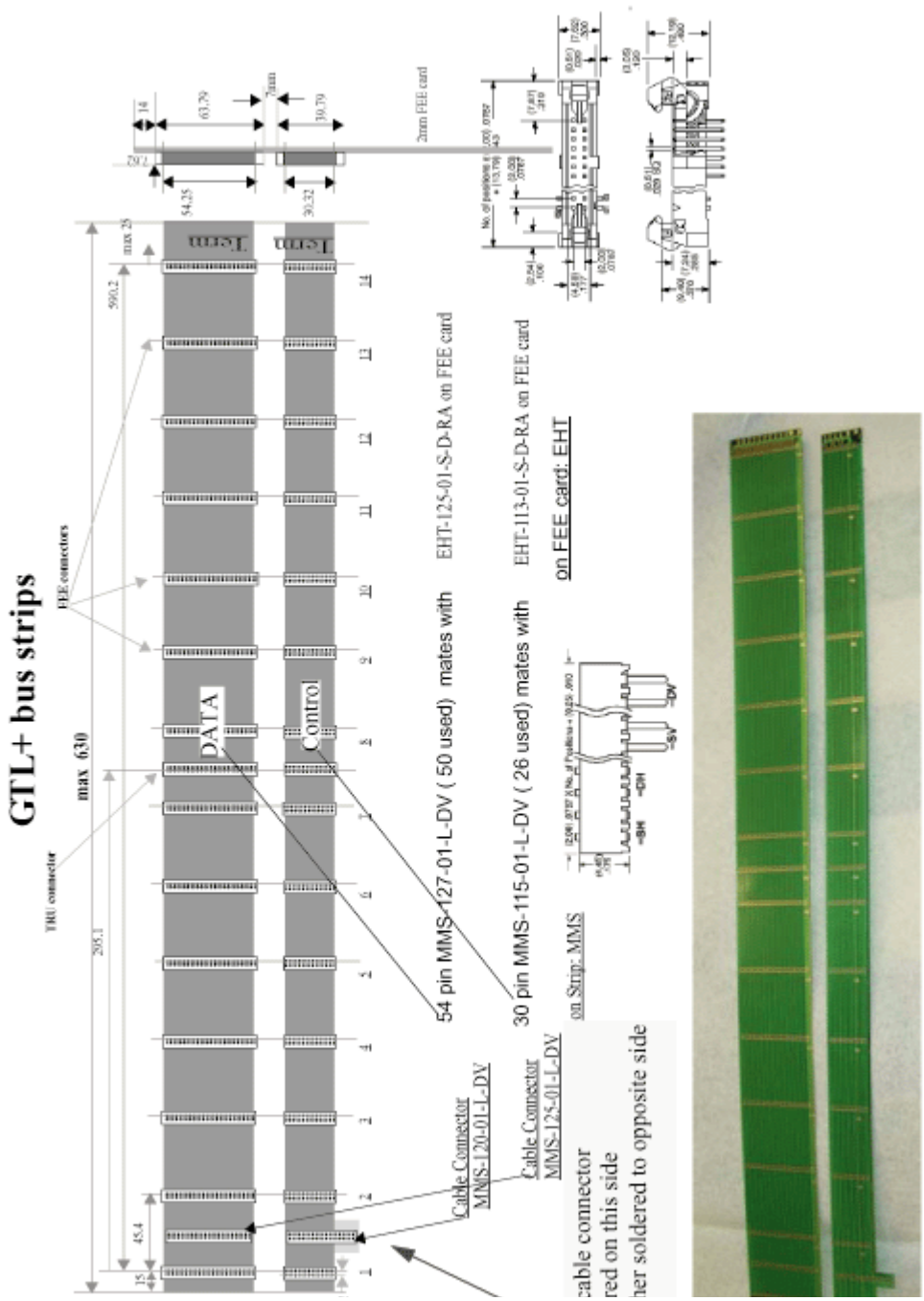


Figure 75 Design files of the GTL Control and data bus strips for PHOS.

CERN production

Data Bus : **EDA-00711-V1 Data**

Control bus

EDA-00712-V1 Ctrl

9.1.2 Run and Test mode schemes

Through a onboard switch (SW1 which is located near the LEDs) one can change between two modes. Run mode and Test mode. The main mode is the Run mode and must be always selected whenever the RCU and other FEE cards are pluged into the backplane. Test mode should be used whenever there is no backplane present.

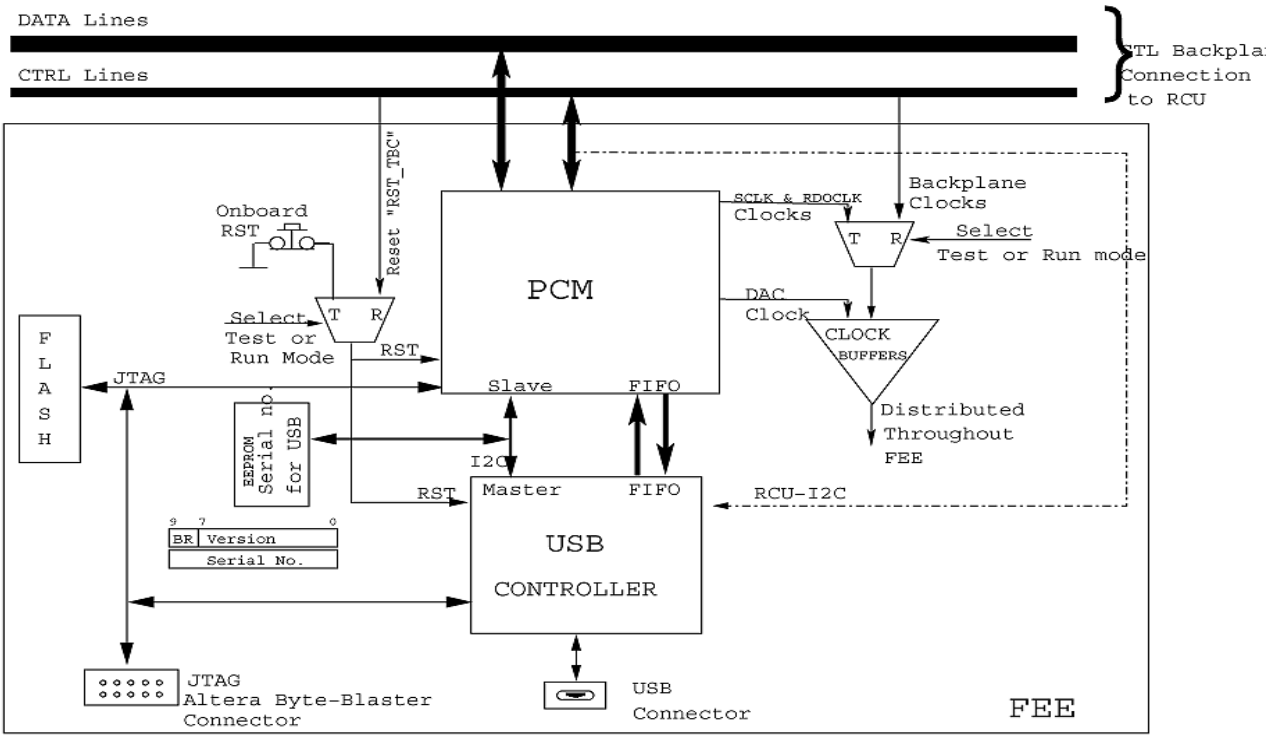


Figure 76 RUN and TEST mode selection on the FFEE cards

9.1.3 Voltage, temperature and current monitoring scheme

The Voltages, Currents on the FEE card are measured for each LV input and temperatures on 3 different places. The principle of measurement is based on quad ADC chips with integrated Temperature sensors as depicted in Figure 77 . The values read out by the individual 10 bit ADC's of 2.5V maximum input are given by

$$U_{adc\ (+)voltage} = U_{in}\ (R_2 / R_1+R_2)$$

$$U_{adc\ (+)current} = (U_{in} - I*R_5)(R_2 / R_1+R_2)$$

$$U_{adc\ (-)voltage} = (U_{in}+8.2)\ (R_2 / R_1+R_2)$$

$$U_{adc\ (-)current} = (U_{in} - I*R_5+8.2)(R_2 / R_1+R_2)$$

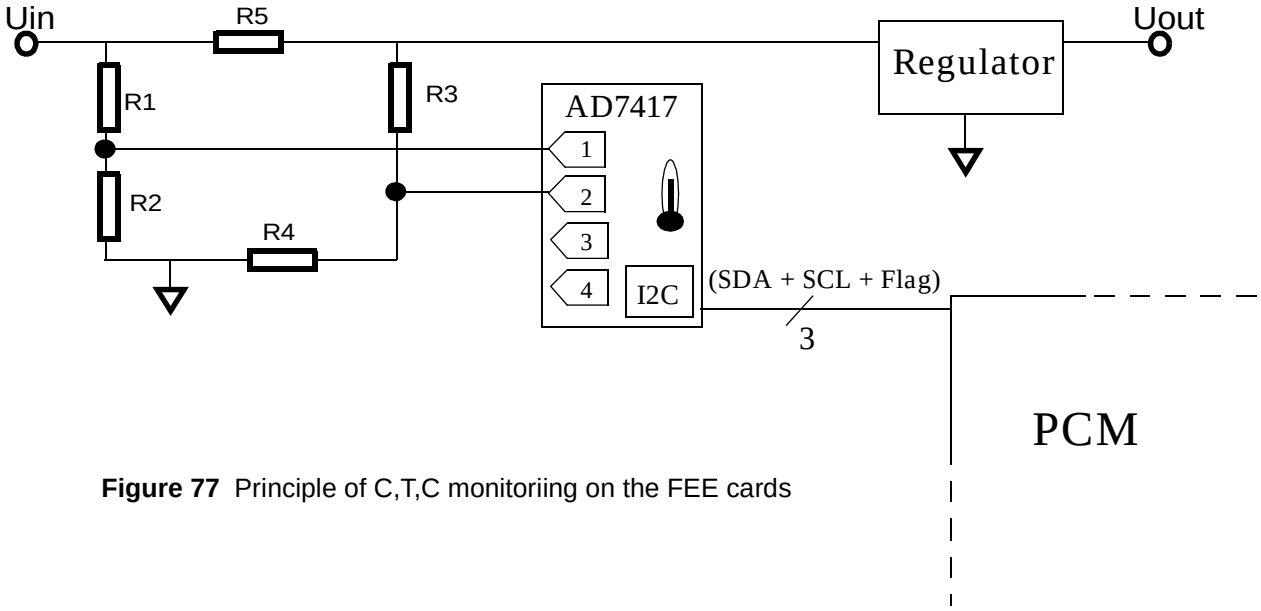


Figure 77 Principle of C,T,C monitoriing on the FEE cards

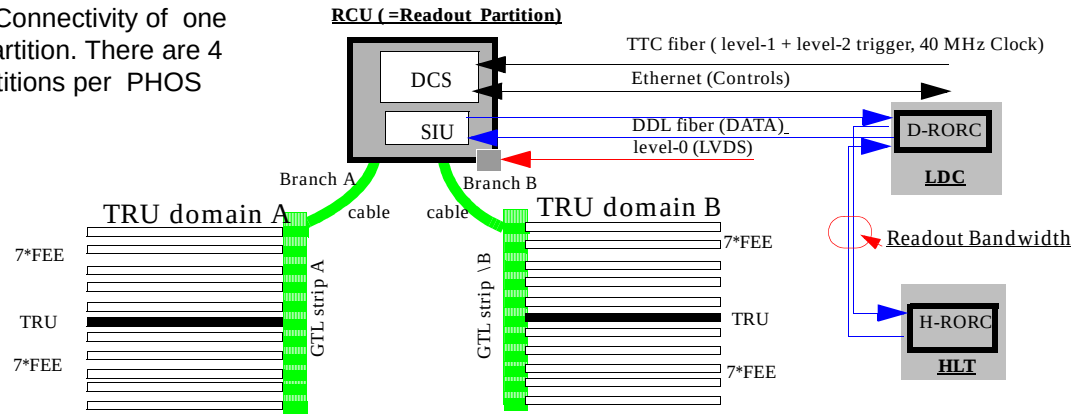
Table 4 Hardwired monitoring setting for the FEE card low voltages

Uin	+4.2V_D	+3.3V_D	+3.3V_A	+6.0V_A	-6.0V_A	+13.3V_A
R1	6.19k	4.42k	4.42k	10k	1k	27k
R2	2.7k	2.7k	2.7k	2.7k	1k	2.7k
R3	6.19k	4.42k	4.42k	10k	1k	27k
R4	2.7	2.7k	2.7k	2.7k	1k	2.7k
R5	0.27	0.15	0.15	0.15	0.33	0.27
Uout	+3.3V	+2.5V	+2.5V	+5.0V	-5.0V	+12.5V
I	0.14 Amps	0.31 Amps	0.34 Amps	0.32 Amps	1.12 Amps	0.14 Amps

10 FEE readout partition

Four RCU modules per PHOS module master the triggered readout of the Multi-event buffers on the FEE cards via two GTL bus branches(see Figure 96). Each GTL bus branch connects 14 FEE and one TRU card. (see 9.1.1

Figure 78 Connectivity of one Readout partition. There are 4 readout partitions per PHOS module.



The RCU is equipped with a DCS card (dimensions see Appendix 10), consisting of a networked processor subsystem which also receives via the TTL optical link the level-1 and level-2 trigger decisions, as well as the 40 MHz LHC clock. The RCU of PHOS also contains a simple mezzanine card connector for inputting local level-0 trigger decisions generated by the TRU's.

The RCU distributes both the level-0 and level-1 trigger decisions as well as the sampling clock via its two GTL bus segments A and B to the FEE cards, 28 in total.

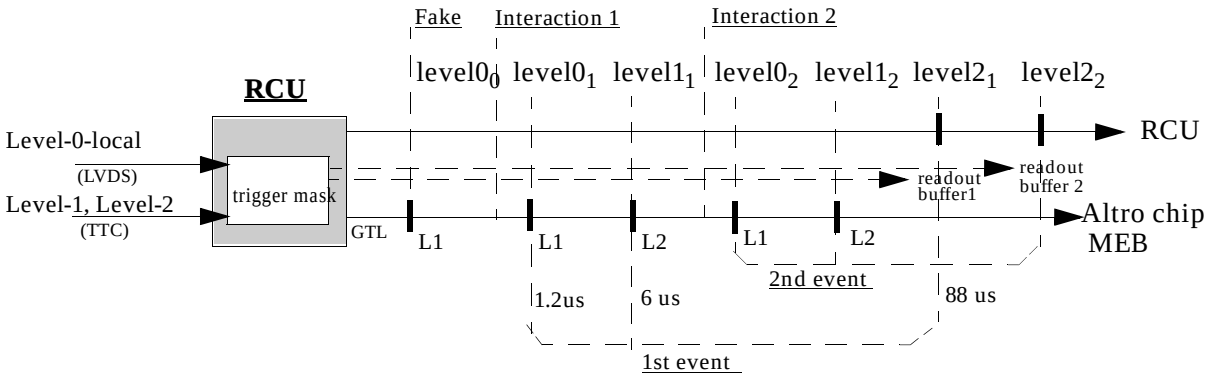


Figure 79 Trigger timing relation with Altro strobe/readout timing

The ALTRO digitizers on the FEE cards contain Multi-Event-Buffers (MEB) which are opened / closed by two timing strobe sequences (named L1 and L2) generated by the RCU as function of the level-0 and level-1 trigger. The ALTRO strobe relation with the level-x triggers is depicted in Figure 79. Other than for the TPC, the PHOS L1 corresponds to the level-0 trigger and L2 corresponds to the level-1 trigger. L1 opens an MEB data buffer and L2 closes it. Successive L1 signals with missing L2 strobe re-open the same buffer. L2 closes a buffer.

Whenever the RCU receives a level-2 signal, it initiates the readout of the Altro buffers via it's two GTL bus branches. The synchronization between level-2 triggers and their event buffers is managed by a triger mask inside the RCU . Defacto, on each level-2 trigger, the RCU addresses all Altro chips on all 14 FEE card and read's the MEB buffers which belong to the level-2 trigger.

The Altro chip has a digitization pipeline of up to 14 clocks, therefore for PHOS, the L1 strobe has a maximum latency of 1.4 us for a typical 10 MHz sampling rate. The locally generated L1 strobe (ore'd level -0 signal from all TRU's) is available earliest after 650 ns. The L2 strobe (level-1 trigger) which closes an event in a MEB buffer is received after a maximum latency of 6.2 us.

The readout decision is taken by the RCU after a L2 trigger. Up to eight ALTRO buffers are available to be filled by L1+L2 strobe pairs withing a level-2 readout boundary. Each buffer has a maximum depth of 512 words of 10 bit.The zero-suppression feature of the Altro reduces the readout block to a minimum. The RCU reads and forwards the assembled event data through the Digital Data Link (DDL).

10.1 Readout bandwidth

The maximum readout bandwidth per PHOS readout partition (1 RCU) can be approximated as 50% of the raw DDL bandwidth of 200 Mbyte / s. With two readout branches per RCU, the balanced maximum bandwith per TRU domain is 50 Mbyte / s with dynamical fluctuations up to 100 Mbyte / s.

With a peaking time t_{peak} of the shaper output pulse shape, the signal is digitized by a sampling frequency f_s. A semi-gaussian shaper pulse is measured[1] over an envelope time of $3.2 * t_{peak}$ (compare Figure 53). The number of samples N ist then

$$N = 3.2 \cdot f_s \cdot t_{peak}$$

Equation 21 Number of samples per shaper channel of 1 triggered event

With fs =10 MHz and tpeak =4us, N =128 samples per semi-gaussian pulse.

The number of samples S per channel and per second per trigger is:

$$S_{channel} = N \cdot channelHit(E)$$

Equation 22 Number of samples per second and channel

1. including some presamples for pedestal measurement

where channelHits(E) is the average number of hits / second above a chosen energy cut E (see Figure 80). Given an hit occupancy H, the readout bandwidth for one partition (2*448 channels of 20 bit) in **bit/s** is:

$$S_{partition} = 1.79 \cdot 10^4 \cdot (H \cdot S_{channel}) + (1 - H) \cdot 8.96 \cdot 10^3$$

where 8960 bits[1] represent the number of bits read out by 1 RCU partition for 100% empty channels, this is however only 1.1 kbyte and therefore neglegible. Finally the partition bandwidth in **Mbyte/s** can be approximated with 30% overhead due to byte boundary rounding etc. as:

$$S_{BW\left[\frac{Mbyte}{s}\right]} = 10^{-2} \cdot H \cdot f_s \cdot t_{peak} \cdot channelHit(E)$$

Equation 23 Partition Bandwidth approximated

where fs is in [MHz], tpeak in [us] and channelHit in [Hz]. The above approximation does not include zero-suppresssion.

The channelHit rates are taken from channel rate simulations of 2004 [5] for p-p and Pb-Pb interactions, reproduced in Figure 80 below

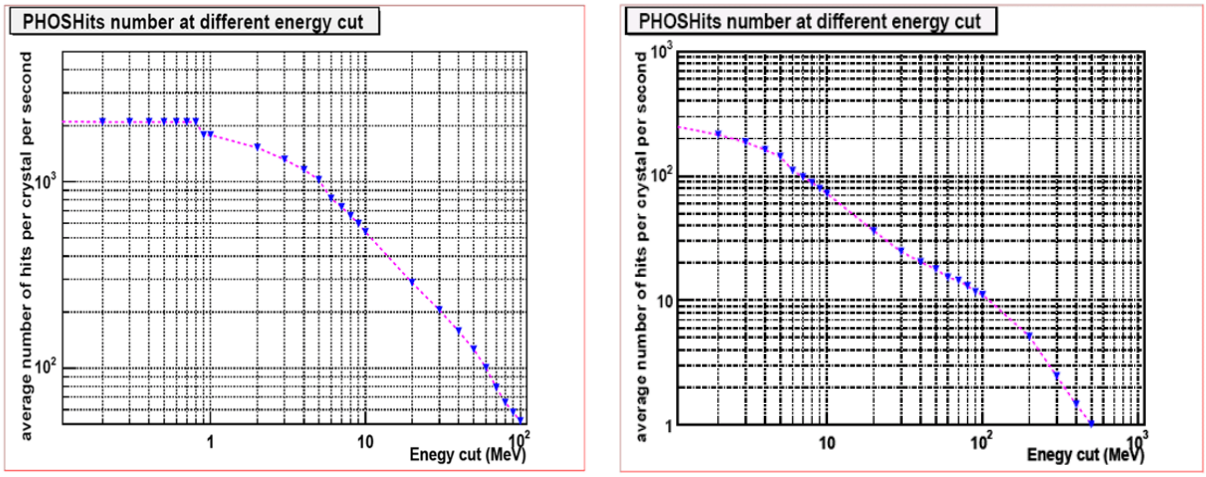


Figure 80 (D. Rohricht et al. 2004) TOP: average number of hits per channel for 5 TeV, 8kHz Pb-Pb interactions in dependence of the energy cut (Hijing , min. bias) BOTTOM: average number of hits per channel for 14 TeV p-p interaction rate of 8 kHz in dependence of the energy cut (Pythia min. bias)

1. one empty channels consists of one 10 bit word.

10.1.1 Bandwidth of Pb-Pb interactions

With an interaction rate of 8 kHz for a high p_T trigger Pb+Pb, a PHOS occupancy of 20% is expected for energy cuts at 40-50 MeV. With a 4us CW shaper and 10 MHz sampling rate there are N=128 samples per trigger. With an single channel rates for different energy cuts as depicted in Figure 80 TOP, and Equation 23 Figure 81 shows the partition bandwidth for three different occupancies as function of the energy cut. These numbers scale with sampling frequency and

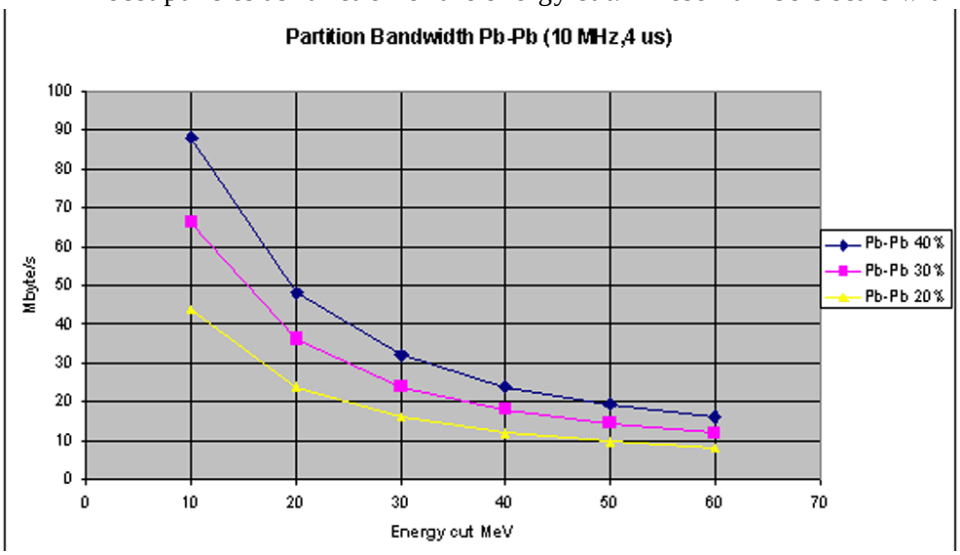


Figure 81 Partition bandwidth for Pb-Pb as function of Energy cut for different occupancies (40, 30 and 20 %)

with peaking time of the shaper.

10.1.2 Bandwidth of p-p interactions

With an interaction rate of 200 kHz for a trigger p+p, a PHOS occupancy of < 1% is expected for energy cuts at 40-50 MeV. With a 4us CW shaper and 10 MHz sampling rate there are N=128 samples per trigger. With an single channel rates for different energy cuts as depicted in Figure 80 bottom, Figure 82 below shows the partition bandwidth as function of the energy cut. These numbers scale with sampling frequency and with peaking time of the shaper.

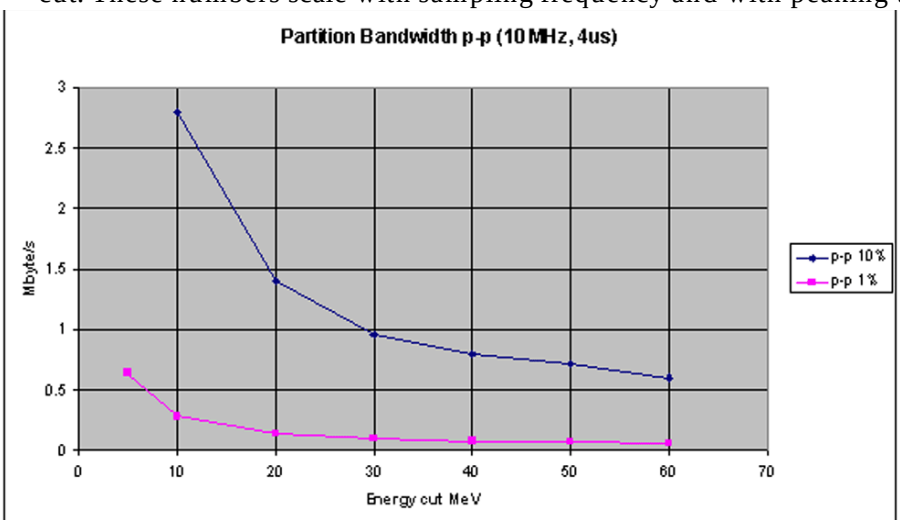


Figure 82 Partition bandwidth for p-p as function of Energy cut for 1% and 10% occupancy

11 Trigger Region Unit (TRU)

The FEE and TRU consitute a co-design of embedded electronics inside the PHOS modules. The TRU generates Level-0 and Level-1 trigger decisision over a TRU domain of 28*16 crystal areas[2], it will be described in more detail in a separate document. The level-1 trigger has 1 LVDS outputs for level-0 and 3 LVDS outputs for low, mid, high threshold triggers A TRU receives 112 fast analog sums from it's left and right FEE cards (see 14.1) and digitizes these on the fly for fast trigger processing in a large FPGA. The FPGA-based algorithm sums the charge of crystal patches of 4*4 in all combinations, compares the integrated charge against programmable thresholds and defines the peaking time relative to the 40 MHz LHC clock. The 12-bit TRU trigger ranges from 8 MeV(LSB) to 32 GeV. .

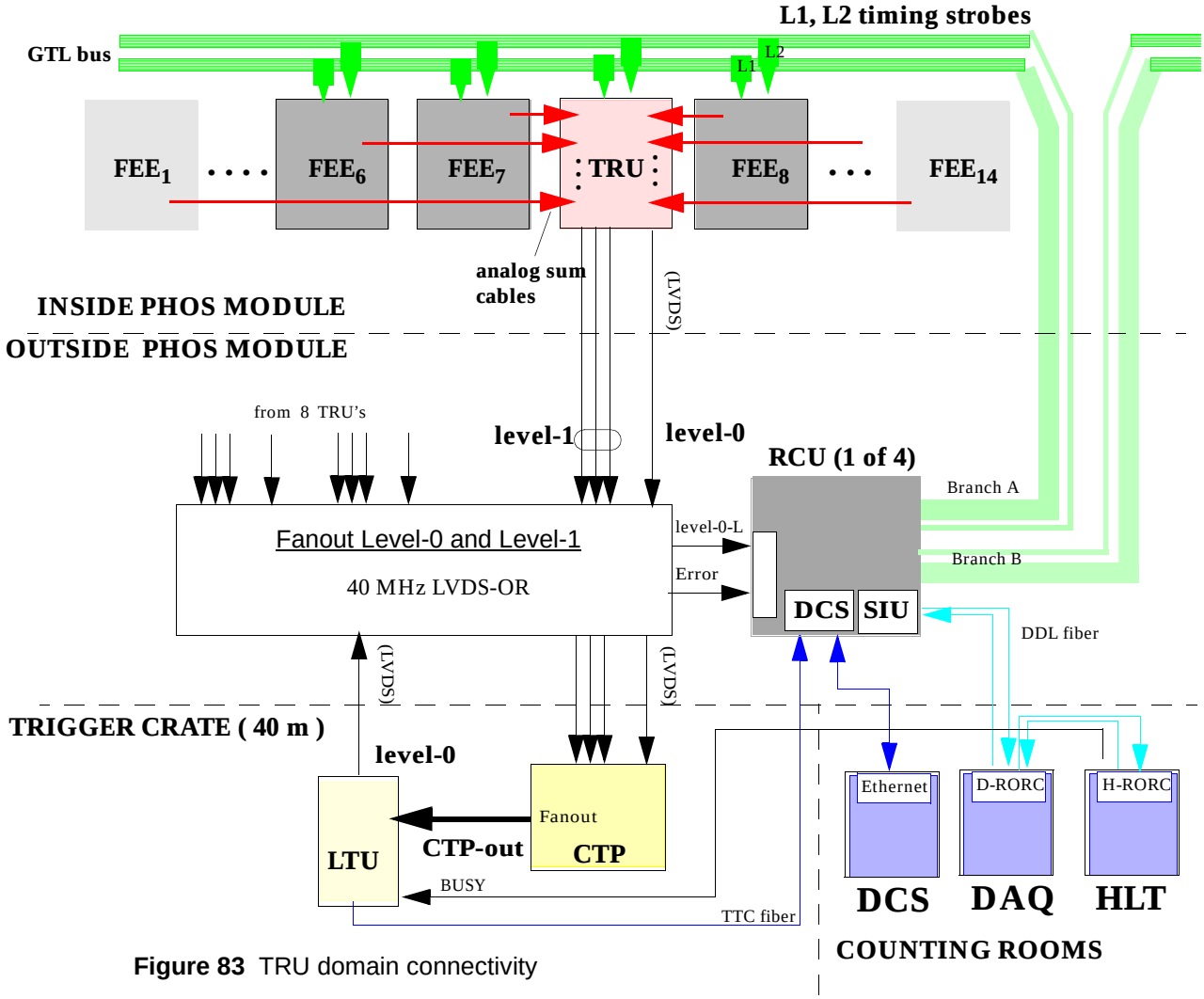


Figure 83 TRU domain connectivity

The FPGA-based algorithms take trigger decisions in ca 200 ns processing time, using a fully parallel sliding window algorithm, combined with a fast peak-finding method over 3..4 ADC samples [2]. These local level-o decisions are also combined into a locally available low latency level-0 timing signal required as buffer-strobe L1 for the Altro digitizers of the local FEE

domains. Therefore the local level-0 decisions are input the RCU. Figure 83 is an overview of the TRU connectivity within the ALICE readout and trigger context.The TRU trigger decisions are NRZ encoded 40 MHz LVDS yes / no signals, connected to an external FAN out which “OR’s” the Level-0 and Level-1 decisions from 8 TRU’s per PHOS module for the Central Trigger Processor. A local level-0 output level-0-L is connected to the RCU, whcih converts it into the L1 strobe for the GLT bus, which enables the Altrodata buffering ca. 650 ns after particle interaction. The Level-1 trigger decisions on the TRU are generated as a continuation of the level-0 processing with more samples and with graded thresholds for low, mid and high $p_{T.}$ These are OR-ed and transmitted to the ALICE Central Trigger Processor (CTP) via LVDS cables of ca 40 m length, hence arrive after ca 200 ns delay at the CTP. With a given Level-0 latency at the input of the CTP of 800 ns, the TRU’s have to output their level-0 decisions latest at 600 ns after interaction.

The TRU implements a permanentely connected USB2.0 port, allowing the TRU to take mastership over its FEE domain, in replacement of a RCU. This feature allows for diagnostic servicing of all FEE cards and for updating of all FPGA configurations via an external PC. The totality of all embedded electronics can be serviced by one PC if all 8 USB cables are externally concentrated via a USB hub.

12 Cold Zone Connectivity

The PHOS detector is constructed from arrays of scintillating PWO crystals, organized in **double Strip Units** (Figure 3). Each crystal is equipped at it's end with one APD, glued on the crystal bottom side. The charge sensitive premplifiers (CSP) are situated below the APDs. The crystals and APD's are placed in the cold zone (-25^0 C). Both the detector signals and the supply voltages for CSP and APD are passed via T-cards to a temperature isolation (Figure 84) which separates the cold and warm zone. Flat cables interconnect the connectors in the warm and the cold zone on both sides. In the cold zone, pairs of two T-cards (1 double strip unit) are mapped to a single FEE card connector in the warm zone. This mapping of double stip units to single FEE card

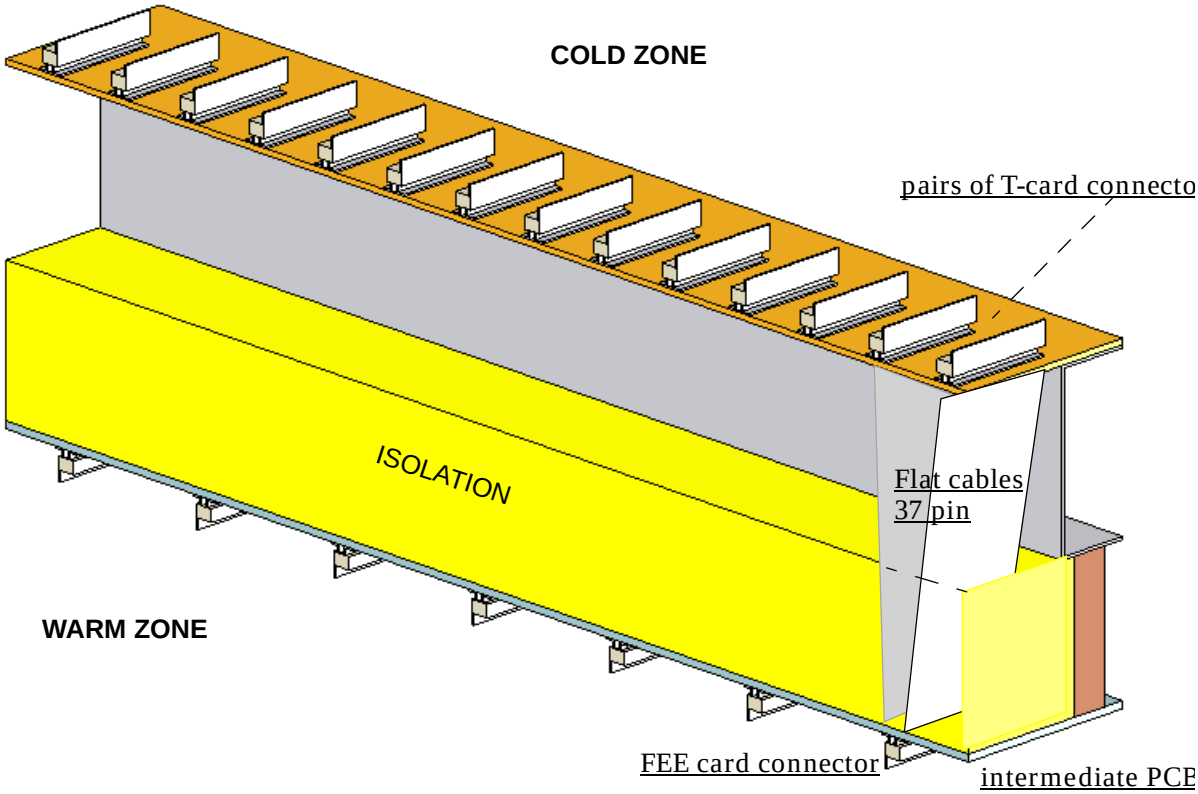


Figure 84 T-card-to FEE card connections through temperature isolation

connectors is depicted in Figure 84. Flat cables provide the interconnection of CSP signals and LV / HV supplies between the cold to the warm zone. The flat cables are passed through temperature isolation. On the warm zone FEE side, the flat cables are soldered to an intermediate PCB with FEE card connectors. Two T-card connectors are mapped to one FEE card connector.

12.1 T-card connectivity

The T-cards serve for connectivity grouping of octal crystal strip units, receiving the short Molex cables from the 8 CSP preamplifiers of an octal Strip Unit. The T-card makes three groups of signals (HV-Bias, LV and CSP output) of one strip unit available on one common, robust AMP base connector (Figure 85). The T-card also contains RC filtering of HV lines towards a common,

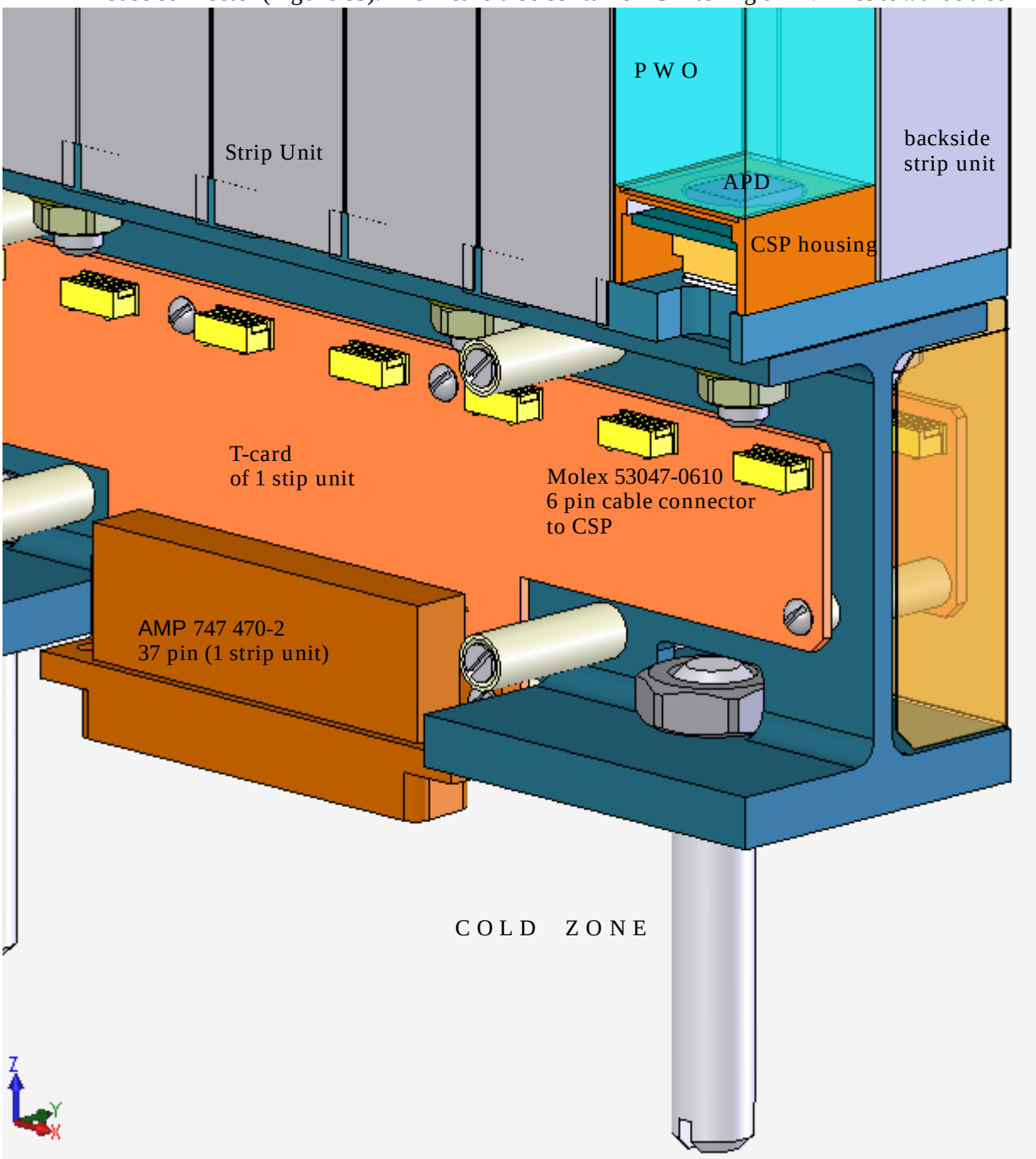


Figure 85 Closeup of T-card relative to strip unit and carrier frames

analog ground. Pinout and connectivity details are shown in Figure 86 below.

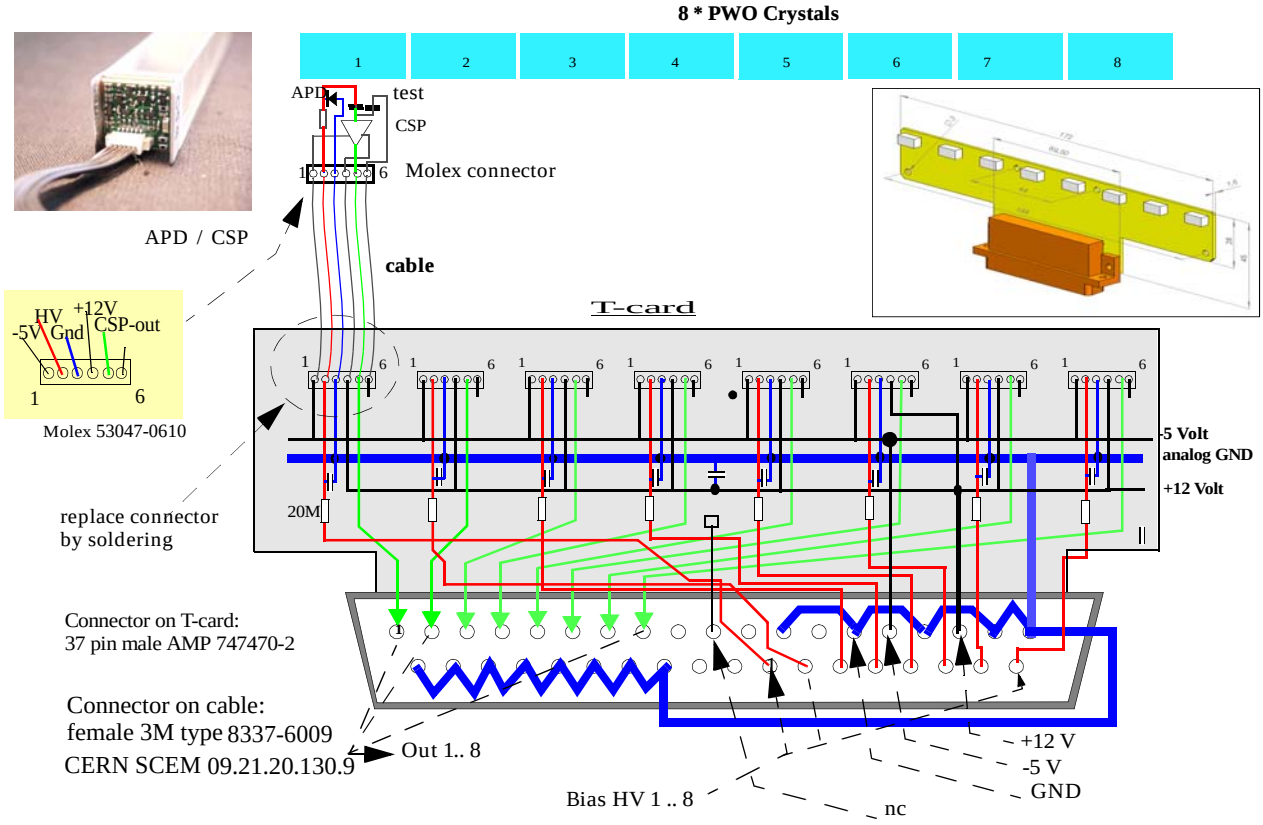


Figure 86 Overview of connectivity of a T-card

12.2 Signal feedthrough block

The output signals from the CSP's which are attached to the crystals are connected with the FEE cards in the warm zone via intermediate connector blocks (Figure 87) . The connector block

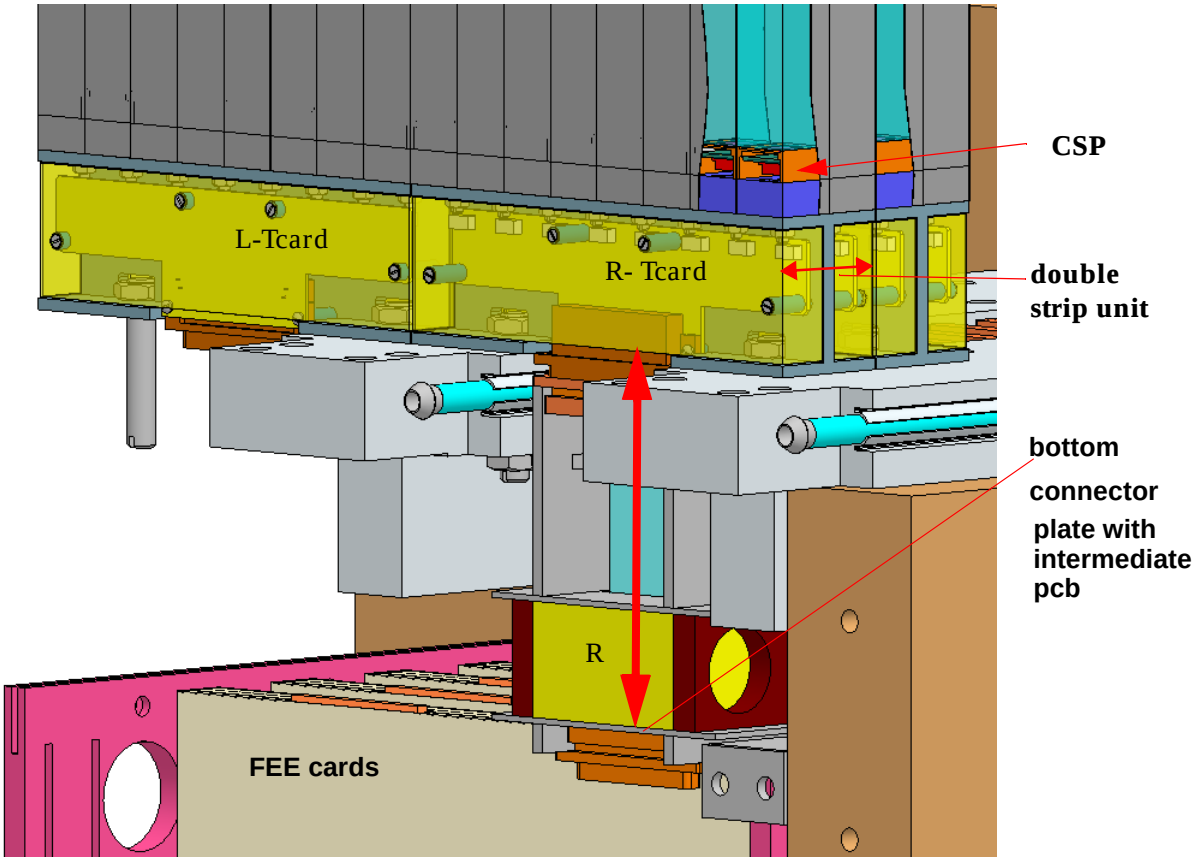


Figure 87 Position of the intermediate connector block between T-cards and FEE cards

serves both for thermic isolation and passes signals between the T-cards and the FEE cards. The signals of two parallel T-cards (of one double strip unit) are routed through the connector block to one FEE connector on the bottom side. FEE connectors are 60 pin SAMTEC LS2 connectors, soldered on the bottom side of a 2 mm thick PCB plate. They mate with the LS2 connector of the FEE cards. Due to the 180 degree rotation of the L and R double strips, the bottom connector plate requires some routing to adapt a.) the different pinouts of the T-cards and b.) the orientation. As shown in Figure 91, the flat cables from the T-Cards are soldered in their natural orientation (without turn). The PCB with LS2 connectors on the bottom side has soldering pads for the flat cables on it's upper side.

13 Warm zone connectivity

Within the warm zone (ambient temperature ~ 25 C) of a PHOS module, two double strip units in a line are read out by a single, 32-channel FEE card. The lateral dimension of a FEE card spans over two FEE connectors as can be seen in Figure 88.The orientation of the two strip units is “Left” mounted and a “Right” mounted, resulting in a left-right mirroring of the two FEE connectors. This choice allows to have the high and low Voltages routed from the left and right extremes of the FEE cards, and leaving the signal traces and analog ground in a quiet central zone ,

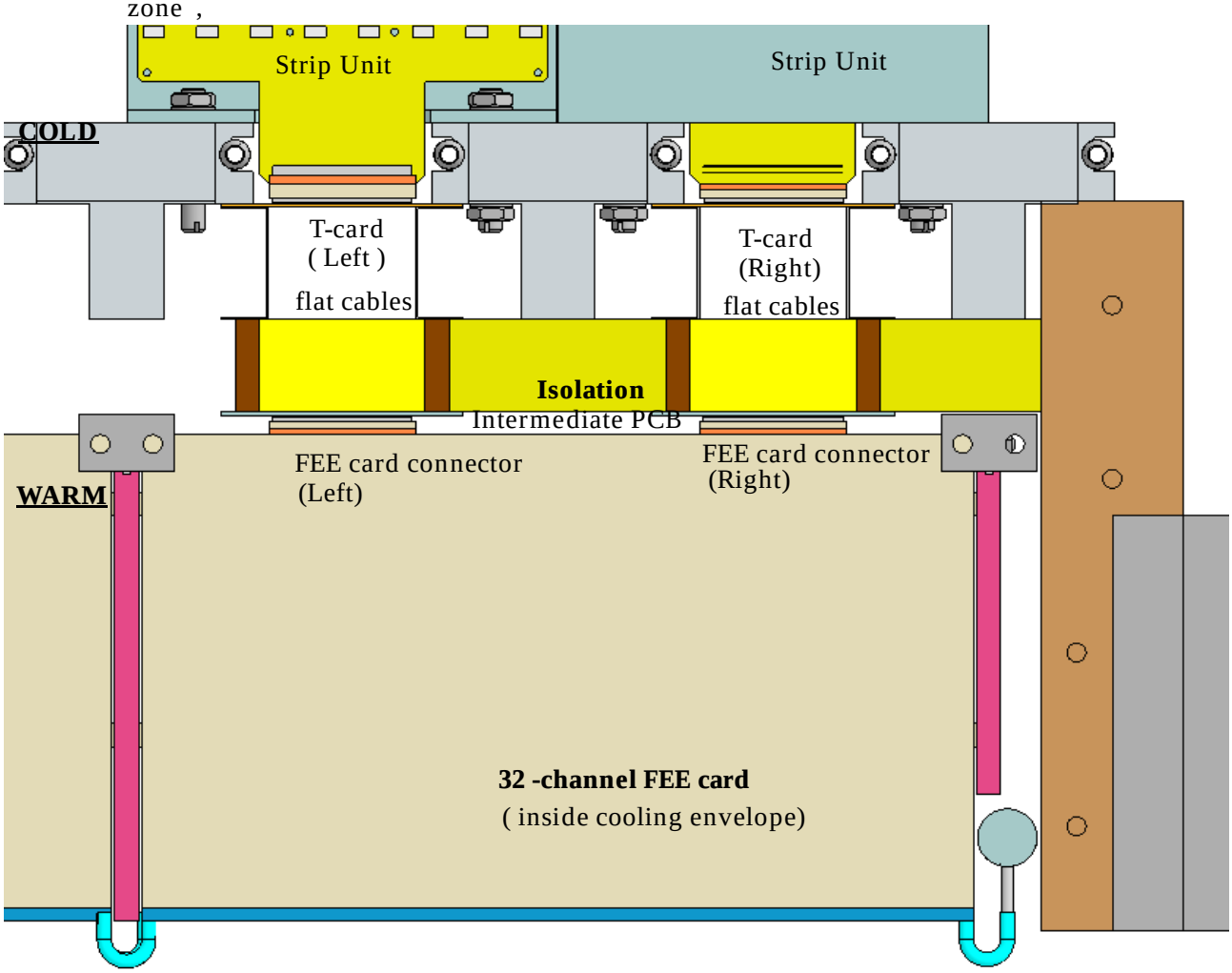


Figure 88 Situation of FEE cards in warm zone below strip units

The PHOS module dimension of 64 *56 crystals corresponds to 4*14 FEE cards. The mounting of the FEE cards (within cooling envelopes) below their double strip untits is shown in Figure 89

The overview principle of the embedded / cooled PHOS Front End Electronics (FEE) is depicted

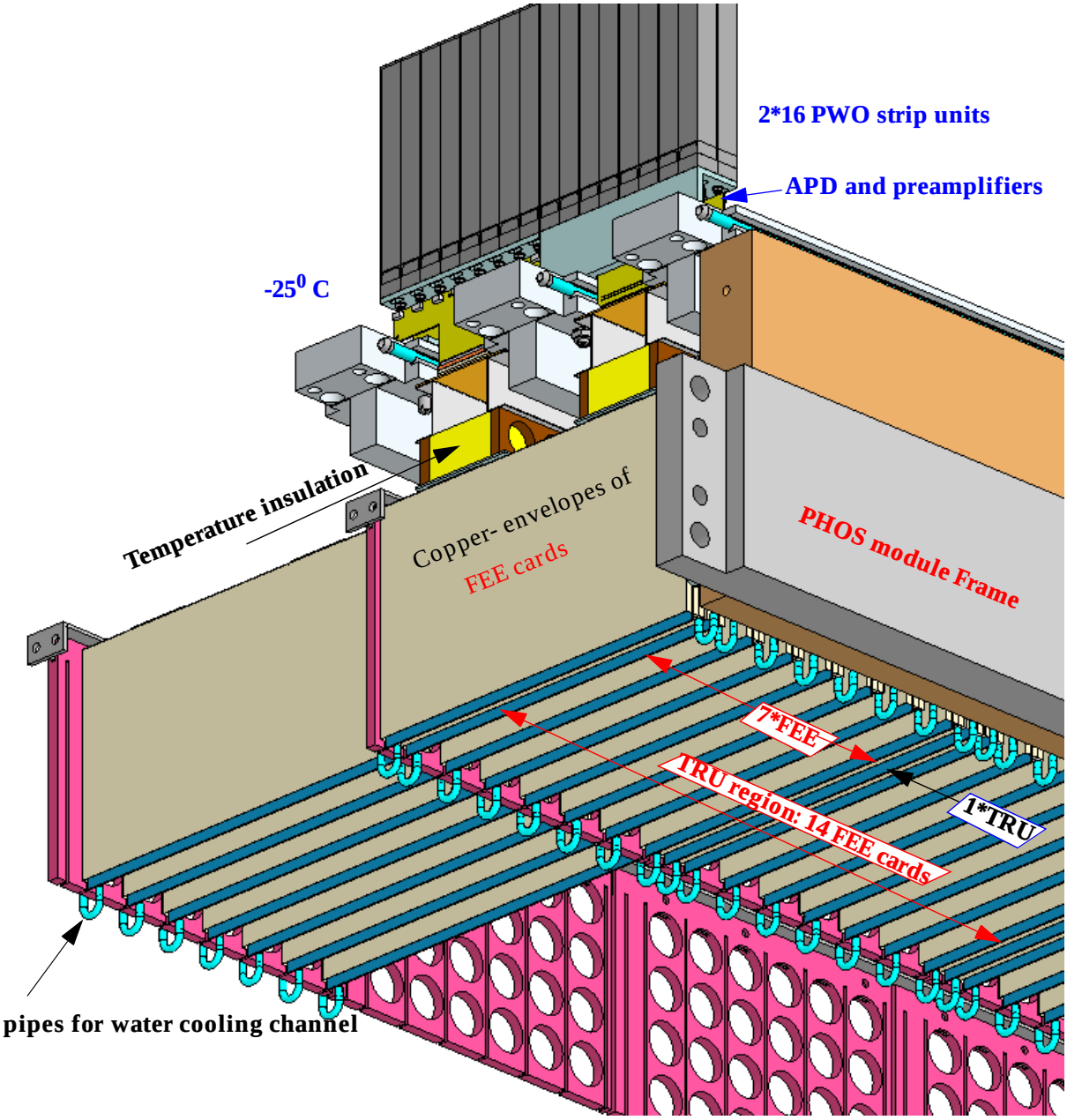


Figure 89 bottom view on FEE cards embedded in copper envelopes and with cooling pipes

in Figure 89.

13.1 FEE card connectivity

The outer dimensions of an FEE card is 210 * 348.8 mm^2 with a PCB thickness of 2 mm. More precise outline details are shown in Appendix 1

Figure 90 shows the FEE card with it's surrounding connectors on the signal input and on the

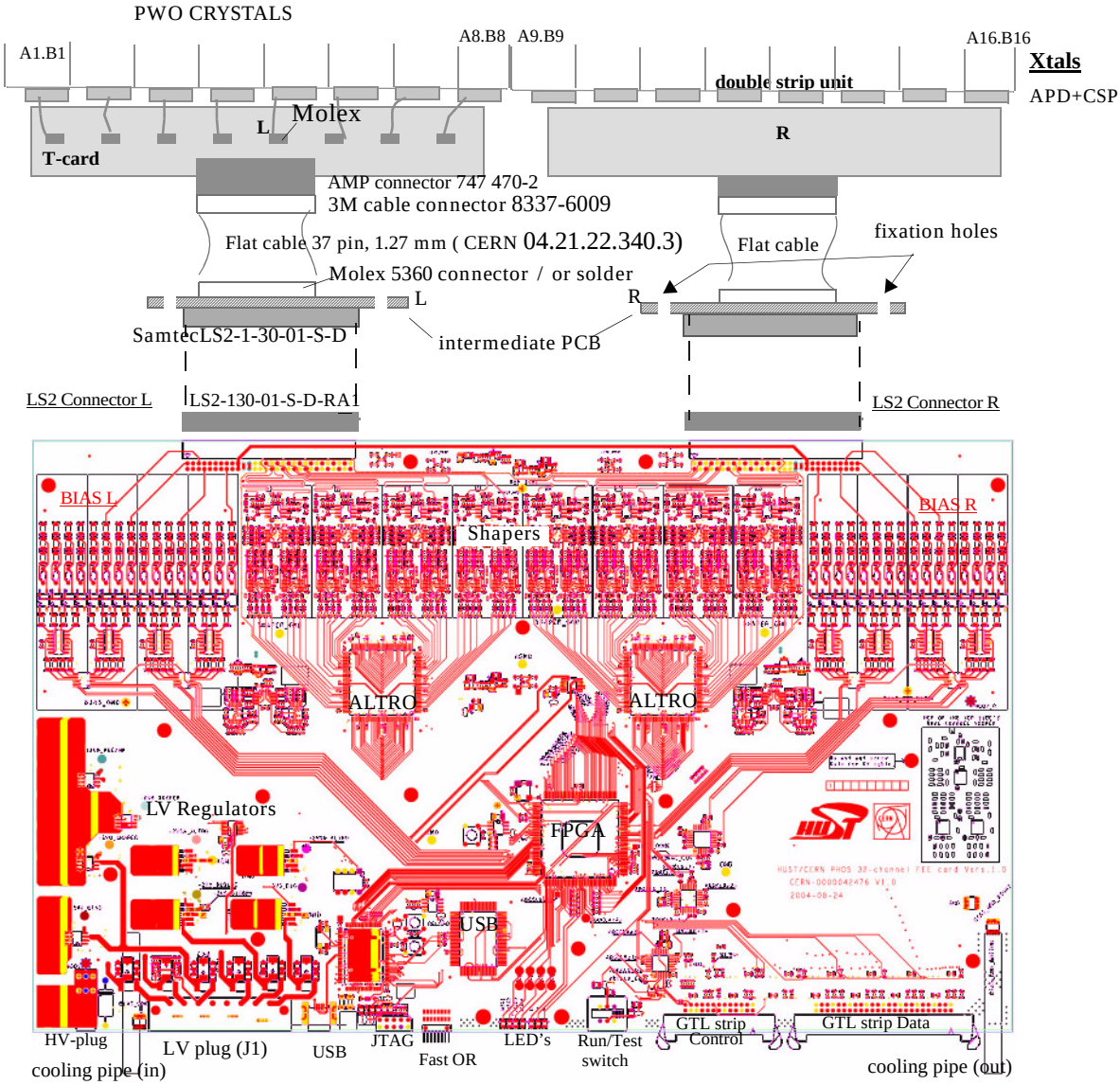


Figure 90 Layout of FEE card and Crystal mapping with FEE shapers

readout and Power side. These are detailed in the following chapters.

13.2 FEE signal input connectors

Each analog feedthrough passes 16 channels of bias high voltage, and 16 signal-gnd pairs of preamplifier signals. There are 2 low voltages, one test signal and analog grounds. The 2 mm pitch LS2 series SAMTEC connector with align and latch mechanics is used with right angle through-hole version is used on the FEE card, and straight-pin, through-hole version on the connector block.

The dielectric constant of the connector material is E= 3.7 (1 kHz) and the dielectric strength is 47 KV/ mm at 23 ^{0}C and 50% humidity. With a nominal 1.5mm isolation thickness, the high Voltage feedthrough up to 0.4 kVolt has been tested by SAMTEC for pin-to-pin and row-to row and unproblematic. The pad distances on the PCB for soldering flat cables should have an isolation distance of 1.5 mm.The flat cables are 2mm pitch cables.

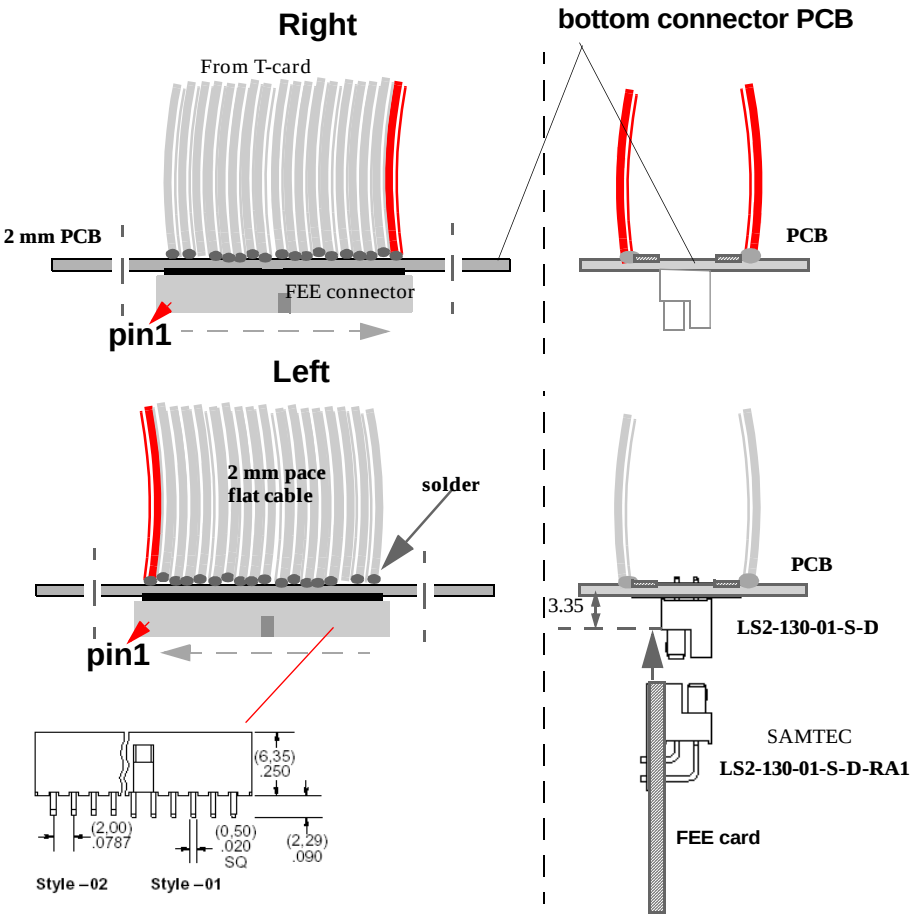


Figure 91 Orientation of flat cables from L and R with FEE input connector

As shown in Figure 91, the FEE cards are equipped with 60 pin LS2 connectors which mate with LS2 connectors in the bottom PCB plate of the connector block. When inserted, there is a 3.35 mm air gap between the FEE card and the bottom of the connector block, allowing for air ventilation.

Figure 92 shows a view from the FEE card up to the L-R oriented T-cards. The FEE card connectors are on one side relative of the FEE card. The T-cards left and right are rotated by 180 Degrees such that the T-card position relative to the FEE card plane changes.

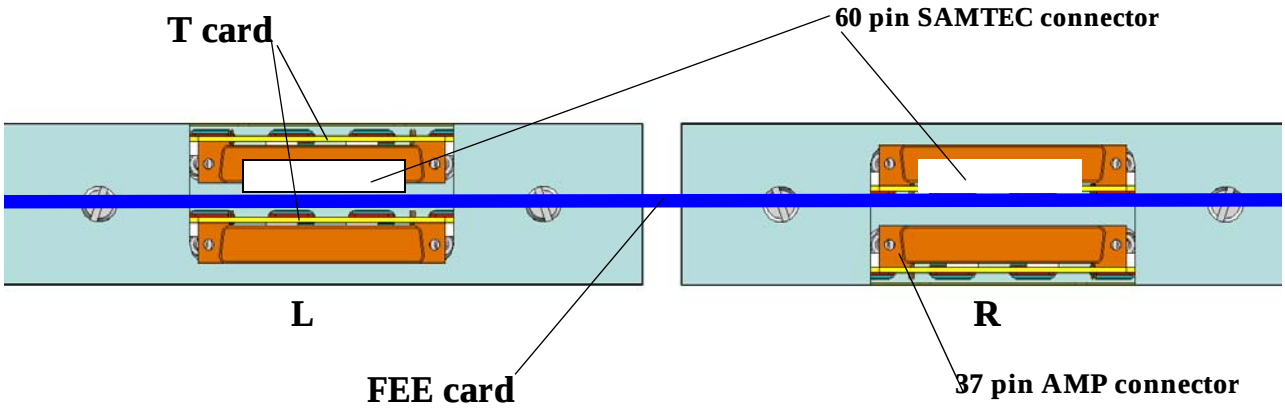


Figure 92 Orientation of Strip Units / T-cards relative to FEE card

13.2.1 Flat cable feedthrough

The Flat cable feedthrough connections per 32 channel FEE card are shown in Figure 93.

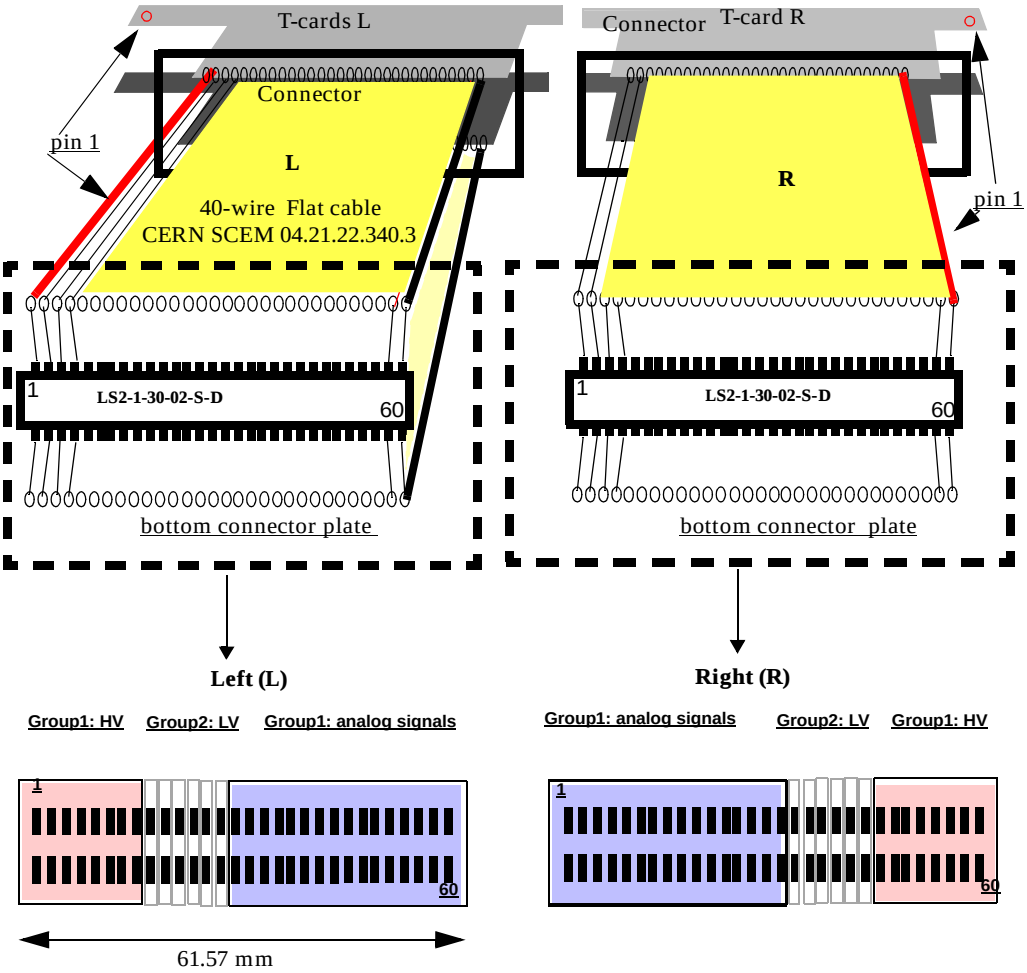


Figure 93 Implementation of signal pinout mirroring L and R connectors.

The flat cable connections between the T-cards and the bottom PCB of the connector block are first soldered on the PCB and then connected on the T-card side. The Right connector is mounted in the same orientation on the FEE card however has a mirrored left-right signal allocation. This situation is depicted in Figure 93.

13.3 FEE connector pinouts

The pinout of one 60-pin FEE connector is shown in Figure 94. There are 3 signal groups: HV, LV and analog signal.The pinout is mirrored into A and B (belonging to one double strip unit) and Left and right. Each row is connected via a single flat cables to a single T-card / strip unit.

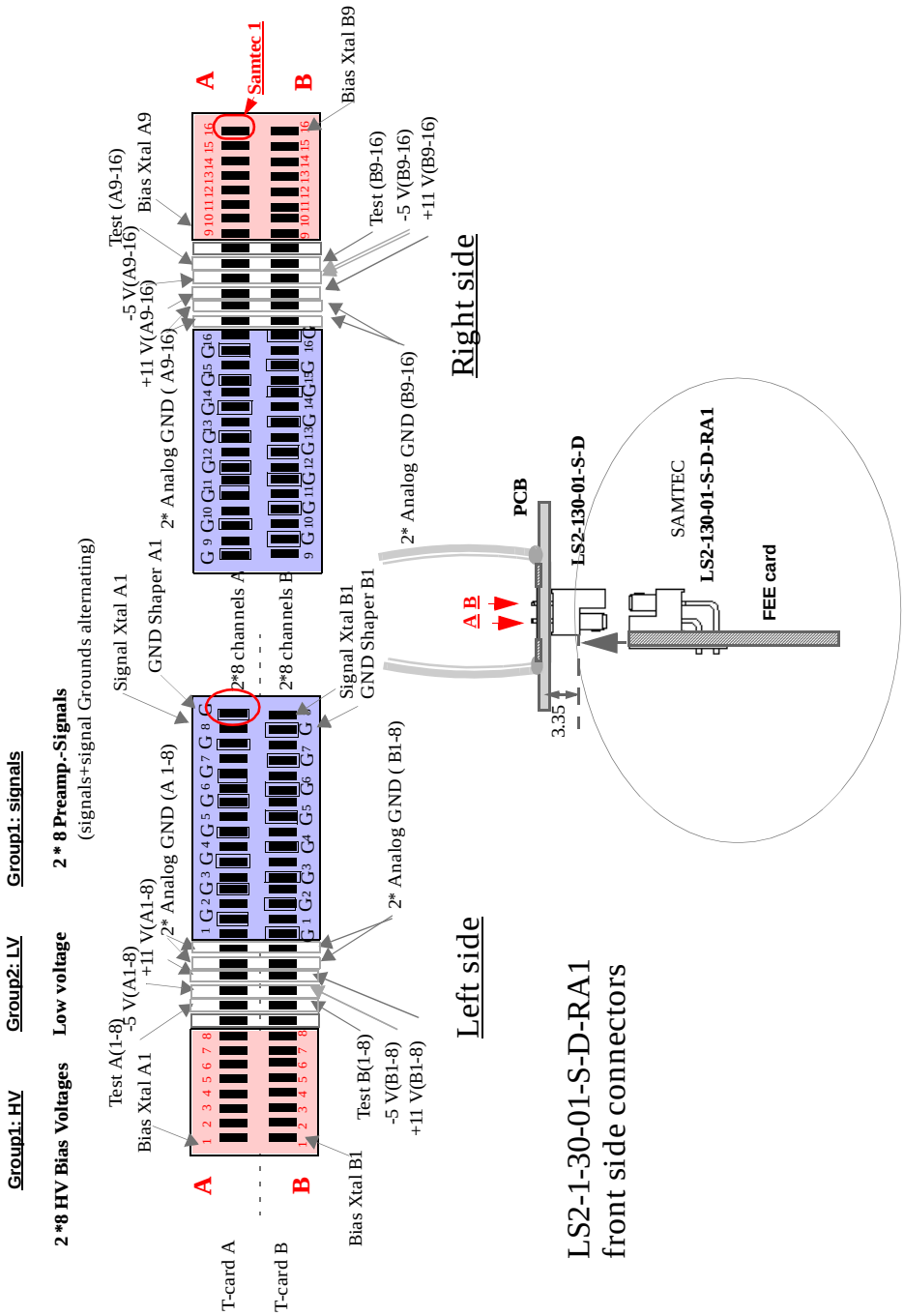


Figure 94 Signal groups in feedthrough connector (Left side view from FEE card to T-card)

13.4 Intermediate signal adapter PCB

The signal adapter on the bottom connector plate (Figure 93, Figure 87) the FEE connector is depicted in Figure 95. It shows the signal correspondence of the four T-cards and Crystals with the pin allocation on the LS-2 connectors of the FEE card.

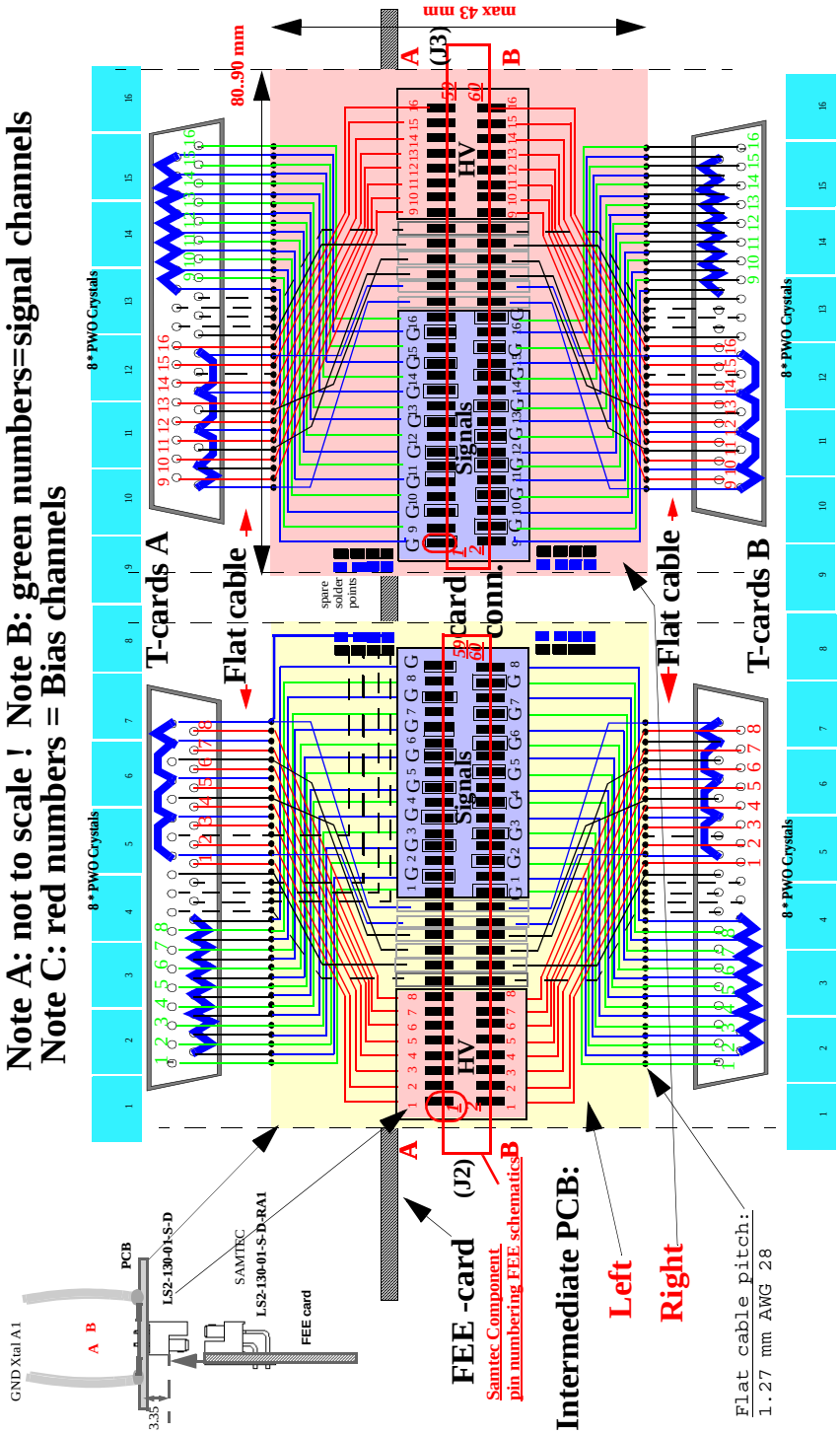


Figure 95 Routing of signals on bottom connector plate PCB

14 Module Connectivity

The global connectivity within a PHOS module and with the external logic is shown in Figure 96.

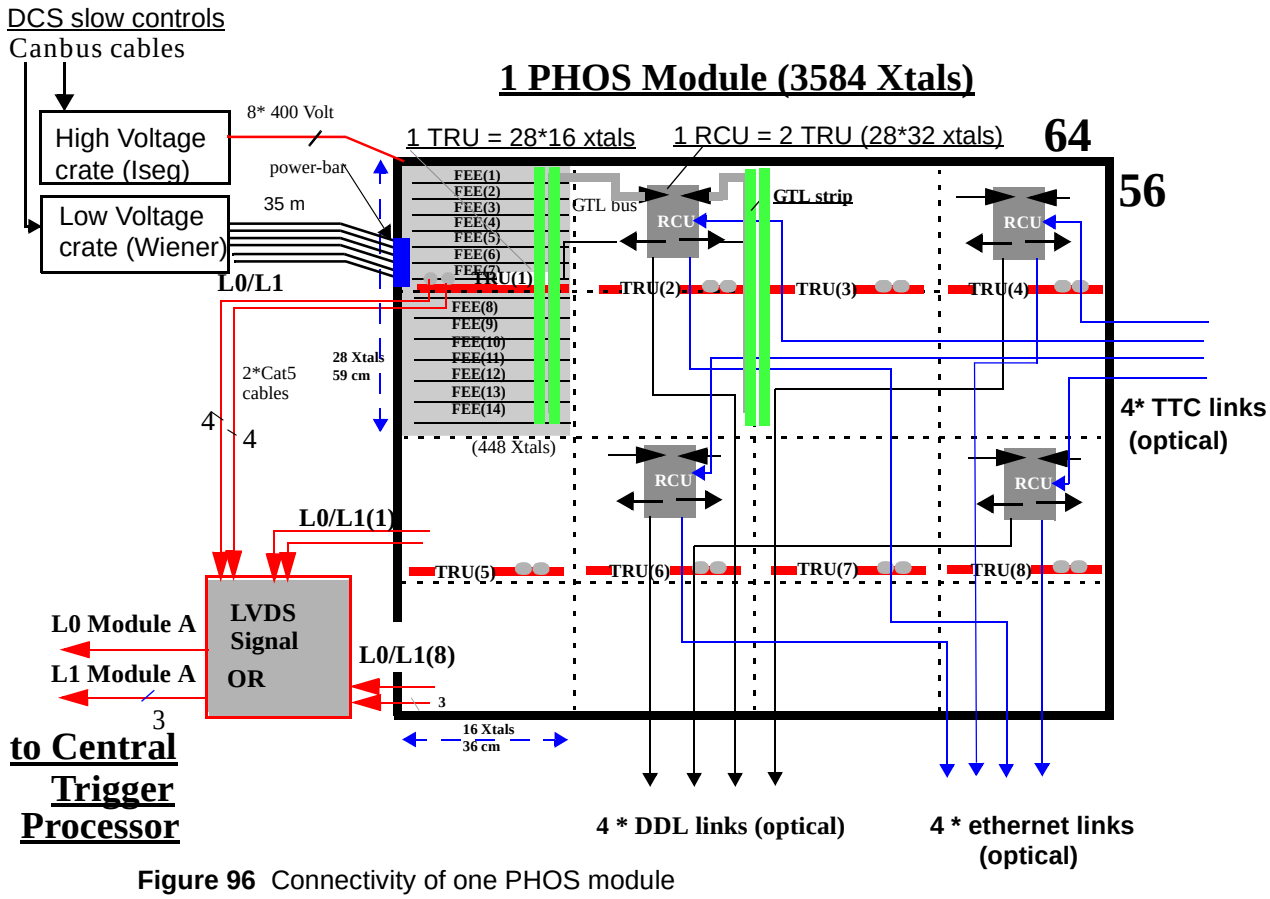


Figure 96 Connectivity of one PHOS module

Stacks of 14 FEE cards (corresponding to 448 crystals) are interconnected each with one central TRU, such that in total, 8 TRUs domains are situated within one PHOS module of 3584 crystals. Each TRU outputs one Level-0 and one Level-1 output cable (twisted pair) to a central (external) trigger OR. The TRU's are all aligned in two of the 28 horizontal air-channels formed by the horizontally aligned FEE cards. A simple, external OR unity receives 8 Level-0 cables and 8 Level-1 cables from the 8 embedded TRUs of a PHOS module.

There are 4 external Readout Control Units (RCU's), for reading out energy and trigger data from two TRU domains. Each GTL branch consists of a data and a control bus. A branch consists of

- two GTL+ cable branch cables of 40 cm length that are passed from the external RCU via openings in the bottom plate of the PHOS module
- two GTL+ backplane strips of 606 mm length as shown in 9.1.1 .

Each RCU is connected to the DAQ system through the optical ALICE DDL links. The SIU (Source Interface Unit) for the DDL is attached as a mezzanine on the RCU. A second mezzanine contains the DCS node, which is connected to the ALICE DCS via a magnetics-free Ethernet link.

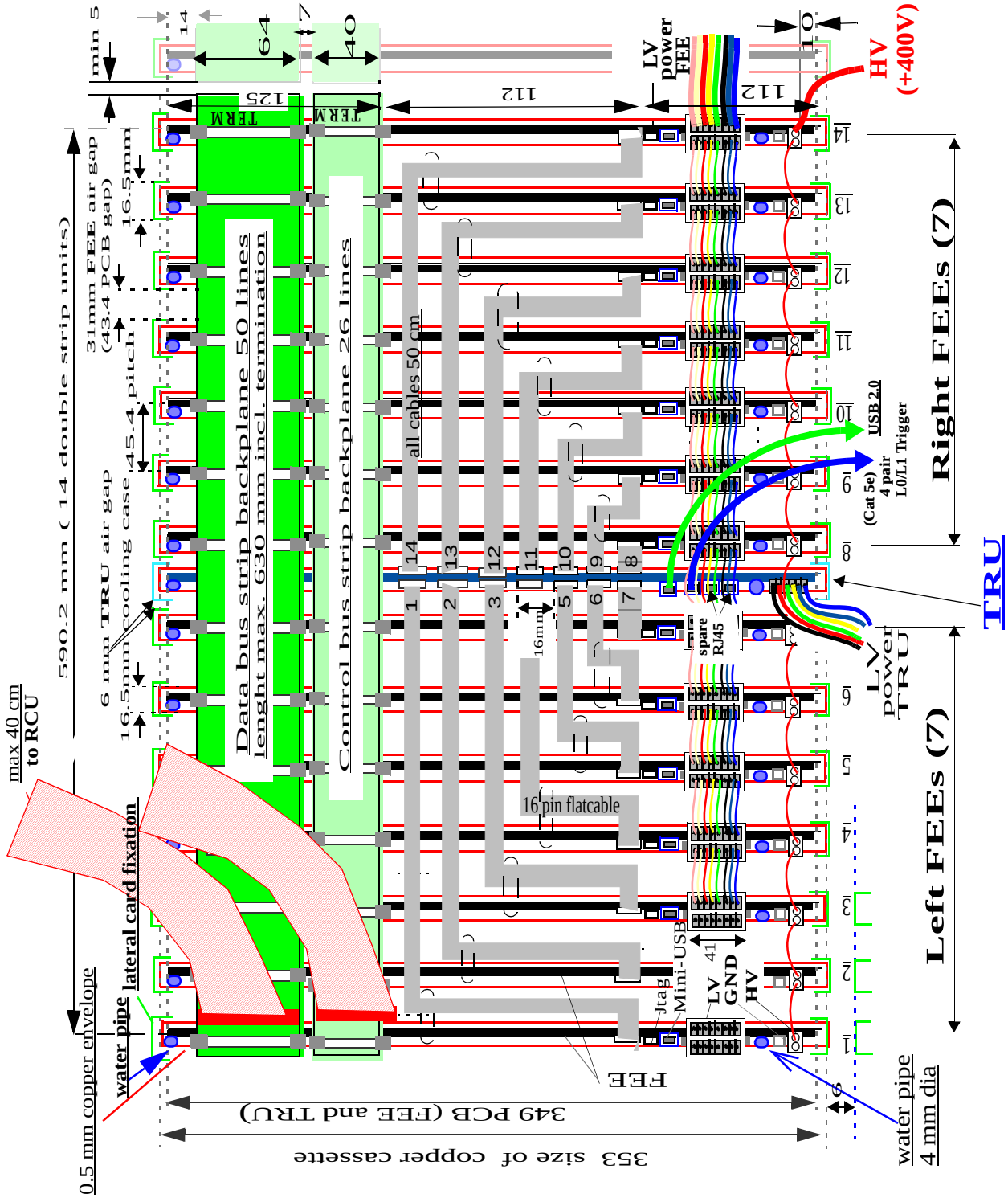


Figure 97 Embedded connectivity of a TRU readout domains.

14.1 Readout Domain connectors (GTL)

The 50 pin data bus and the 26 pin control buses (see Figure 75) are implemented as terminated pcb striplines, derived from the strip bus of the TPC Each stripline connects 2 * 7 FEE cards spaced at 45.32 mm center line, and a central TRU inserted between the middle FEE cards at half pitch.

Table 5 SAMTEC FEE card backend connectors

Data bus (50 pin)	**Connector on FEE**	**on Strip backplane or Cable**
	50 pin EHT-125-01-S-D-RA	54 pin MMS-127-01-L-DV note: only 50 pins used
		Cable connector for RCU: 2mm cable connector: 50 pin MMS-125-01-L-DV Cable: 2 mm IDC, 50 wires, 15 inch cable Samtec TCMD-25-D-15.00-01 **modified: each pair is to be inverted**!
Control bus (26 pin)	**on FEE**	**on Strip backplane**
	26 pin EHT-113-01-S-D-RA	30 pin MMS-115-01-L-DV note: only 26 pins used
		Cable connector for RCU 2 mm cable connector: 40 pin MMS-120-01-L-DV Cable: 2 mm IDC, 50 wires, 15 inch cable Samtec TCMD-20-D-15.00-01 **modified: each pair is to be inverted**!
Analog Sum (2*8 pin)	**on FEE or TRU**	**0.645mm-cable 50 cm**
	SAMTEC connector FTSH-108-01-L-DH-A	Cable 20 inch FFSD-08D-20.00-01-N

15 High Voltage distribution

The ISEG HV modules[7] are available in 6U Eurocard standard, with a single multi-wire REDEL connector for 8 channels. The EHQ 8405p_156F module has 8 *(500 Volt / 15 mA) floating Ground HV connections. The Iseg HV connector provides 8 floating HV supply voltages to a multi-conductor HV cable ending up on a HV patch panel with Redel connectors (Figure 98) which serves as HV fan-in for a single, 56 wire HV cable of ca 100 m lenght and ending at the PHOS HV distribution board in UX25 close to the PHOS detector. Each of the Redel connectors feeds eight octal HV cables for the eight readout domains of the PHOS module. Each of these is daisy-chained inside the PHOS module. .

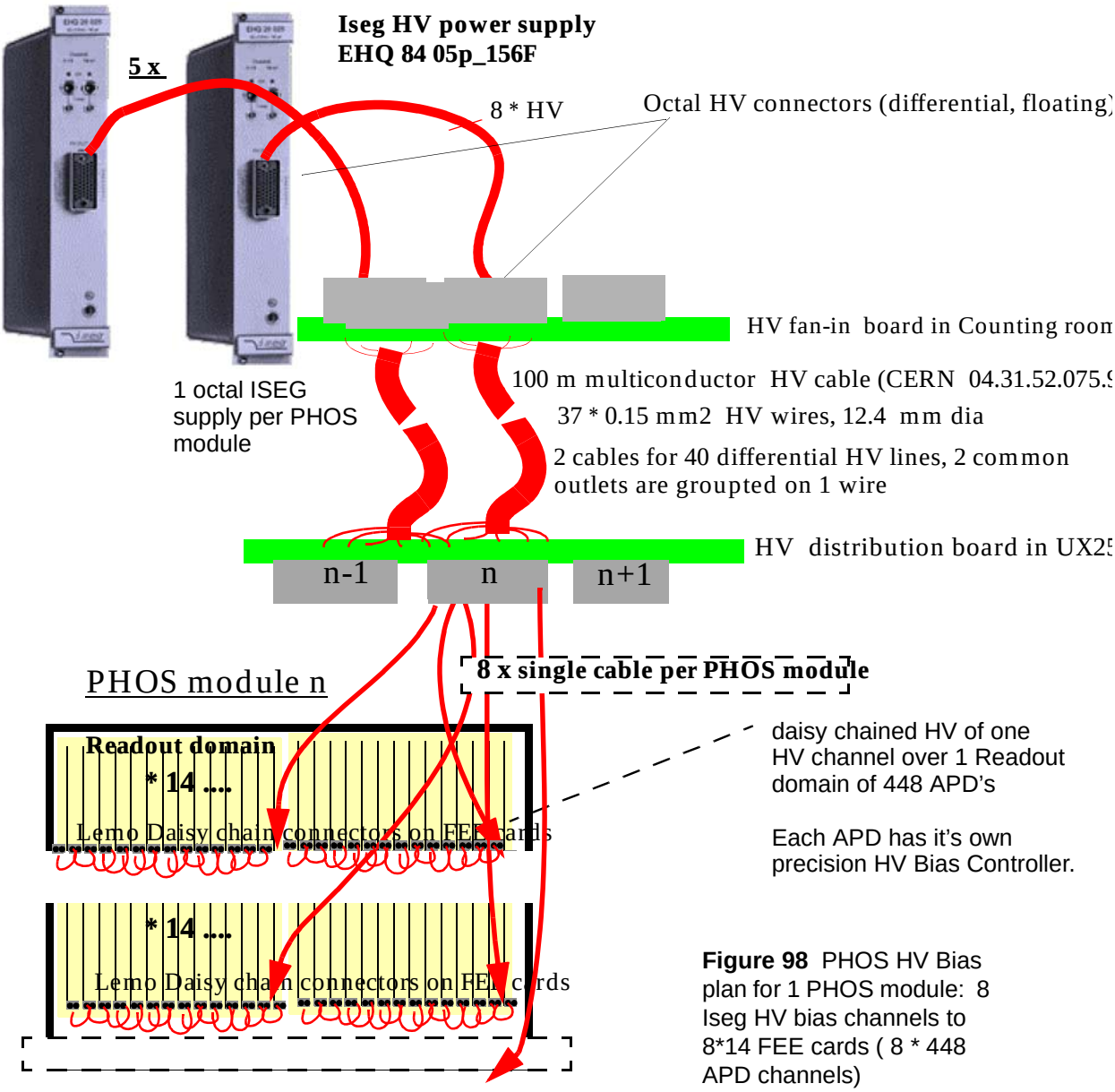


Figure 98 PHOS HV Bias plan for 1 PHOS module: 8 Iseg HV bias channels to 8*14 FEE cards (8 * 448 APD channels)

16 Low Voltage power distribution

The FEE card requires 6 low voltage power connections via differential power cables between the PHOS module power block and the LV power supplies. At the power block, the analog and digital grounds are separately connected and continued as analog and as digital ground. Each FEE card is alimented from the PHOS power block via 8- wire strands to 8-pin power connectors on the FEE cards. as shown in Figure 99.

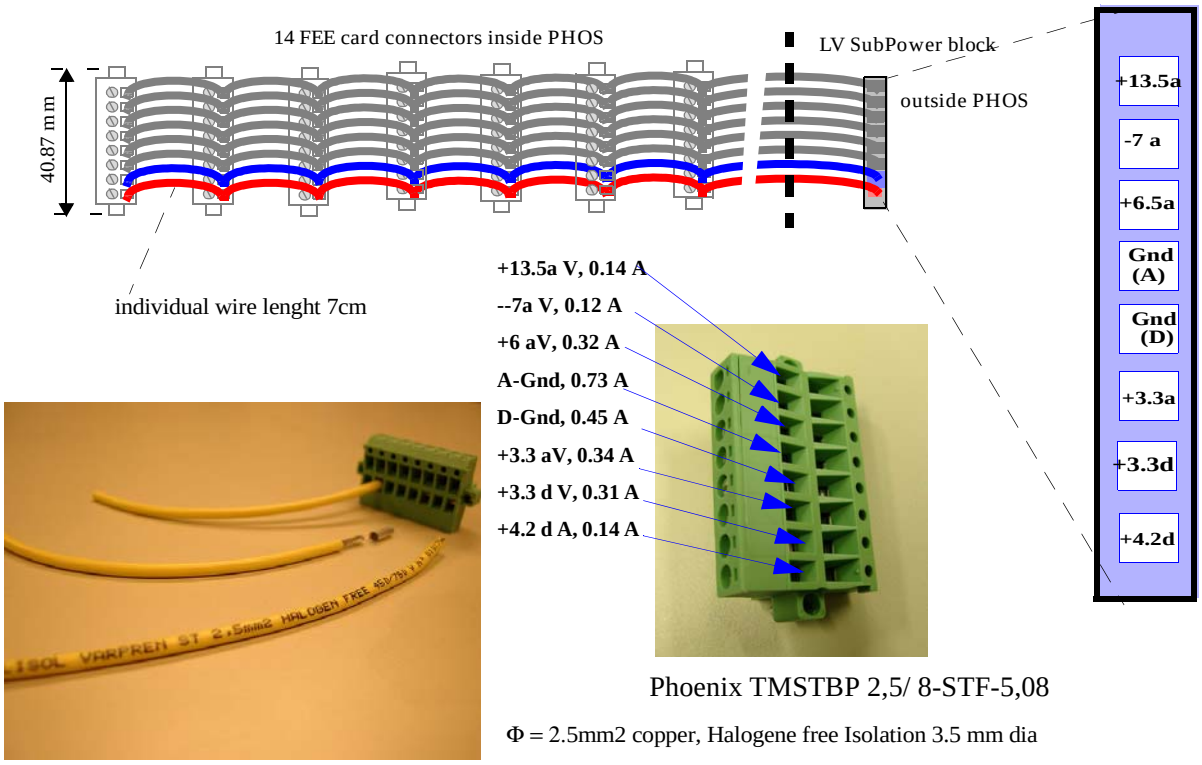


Figure 99 one of 16 power strands for powering FEE cards

The strands consist of eight 2.5 mm^2 isolated copper wires and 12 A daisy chained cable connectors of type Phoenix TMSTBP 2,5/8-STF-5.08. The 6 LV connections are:

1. +13.5 a Volt ..... 0.14 A
2. -6.5 a Volt ..... 0.12 A
3. +6 a Volt ..... 0.32 A
4. +4.2 d Volt ..... 0.14 A
5. +3.3 a Volt ..... 0.34 A
6. +3.3 d Volt ..... 0.31 A

The total power consumption per FEE card adds up to5.4 Watt

The logical LV connectivity and power plan for the FEE cards combined with the TRU and

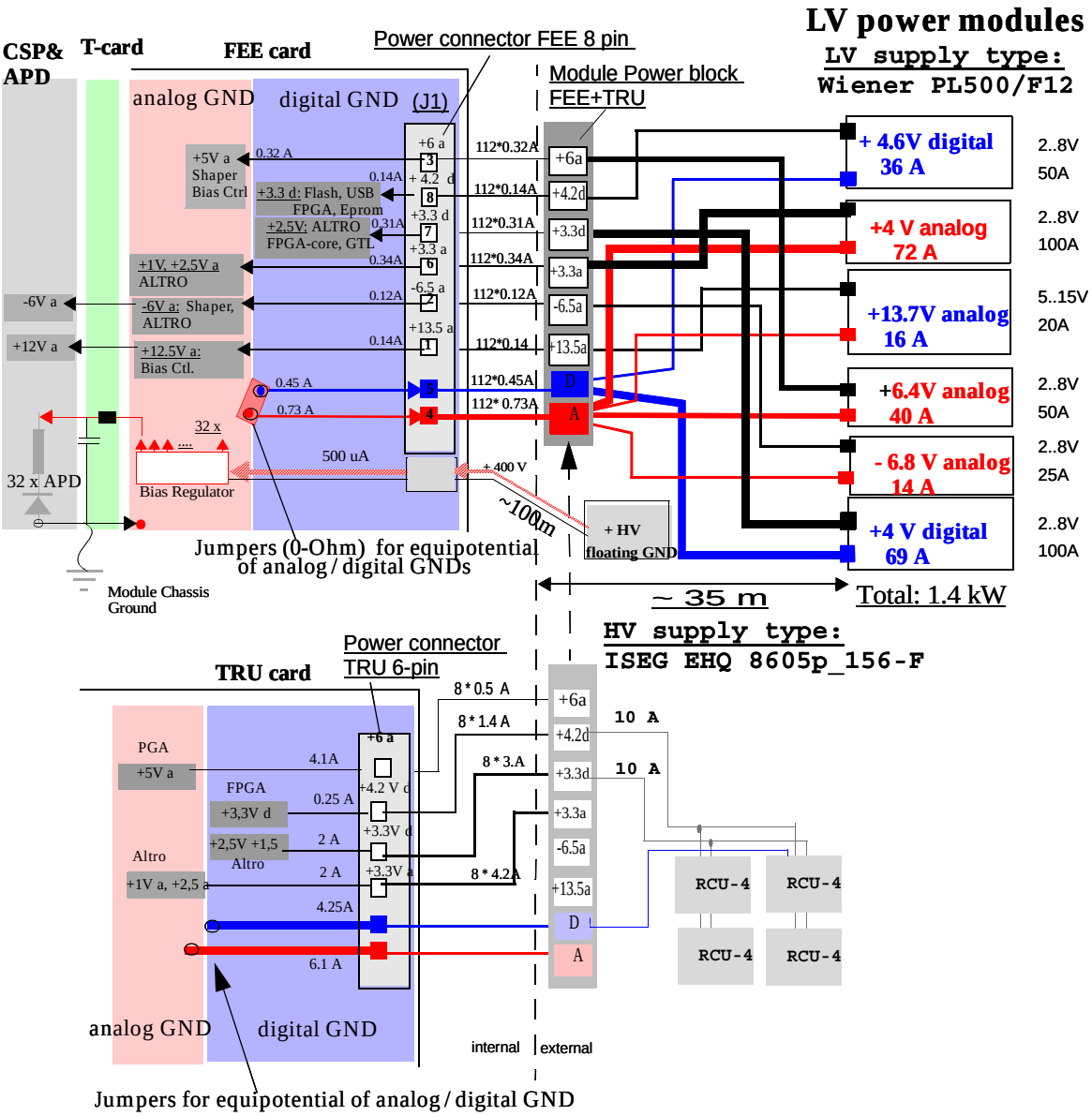


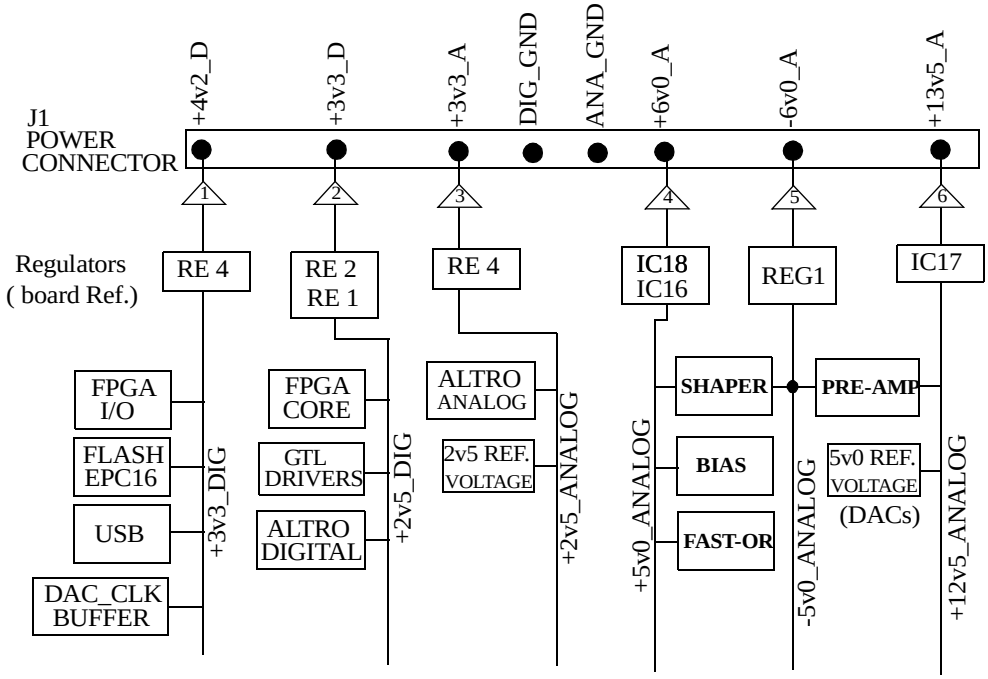
Figure 100 Power schematics for 1 PHOS module

RCU's is detailed in Figure 100.

The LV power supplies for 6 different Voltages are of type Wiener PL500 / F12 [6] providing a total power of 1.3 kWatt per PHOS module. There 2 * 6 LV power cables of 35-40 m length and cross sections between 95 and 120 mm2 required (see 16.2).

16.1 LV supply hierarchy on FEE cards

The LV supply hierchies for the FEE card electronic sections is depicted in Figure 101. The



Voltage/ Current Sensors	Power Line	Values Stored on Registers of Board Controller			
		Voltage Registers		Current Registers	
		Mnemonic	Reg. Address	Mnemonic	Reg. Address
1	+4v2D	D4V	09	D4VC	0A
2	+3v3D	D3V3	0B	D3V3C	0C
3	+3v3A	A3V3	39	A3V3C	3A
4	+6v0A	A6V	3B	A6VC	3C
5	-6v0A	AM6V	29	AM6VC	2A
6	+13v5A	A13V	2B	A13VC	2C

Figure 101 LV Power hierarchies and Board Controller LV test registers on the FEE cards

designations of the regulators corresponds to the ones on the FEE cards. The Current / Voltage sense testpoints are depicted as triangles, their correspondence with the U / I test registers of the PMC controller [26] are shown in the table below.

16.2 LV Power supplies and cables for 1 PHOS module

There are 6 high current LV power supplies of different voltage and max 300 Watt each per PHOS module. The output voltages at the LV power supplies have to be higher than at the input of the FEE electronics due to ohmic voltage drop over 35 m of differential LV power cables. Two different cable cross sections are used per PHOS module, all have a length of ca 35 meter.

- 6 LV power cables of 95 mm2 copper (CERN SCEM 04.08.61.975.0) with outer diameter > 23mm and of CERN Type UCH1s
- 6 LV powre cables of 120 mm2 copper (CERN SCEM 04.08.61.980.3) with outer diameter > 25 mm CERN Type UCK1s

The ohmic resistance of these cables for 35 meter length is calculated as follows:

Annealed Copper: 1.724 x 10-6 Ohm.cm @ 40^0 C
Resistance of 35 m length 95 mm2: 1.724 x 10-6 * 3500 * 100/95 = 6.35 mOHM
Resistance of 35 m lenght 120 mm2: = 5.02 mOHM

With the required FEE Voltages at the FEE input power block and the total supply currents, the Voltage drop and power dissipation per cable is shown below:

P.S. output	differential Voltrage drop	LV current	Cable pair heat	LV power	Voltage on power block
13.7 aVolt	0.2V on 95 mm2	16A	3.2 Watt	max 0.22 kW	(+13.5 a Volt)
6.8 aVolt	0.18V on 95 mm2	14 A	2.5 Watt	max 0.095 kW	-6.5 a Volt)
6.4 aVolt	**0.4V on 120mm2**	**40 A**	**16 Watt**	**max 0.26 kW**	**(+6 a Volt)**
4.7 d Volt	0.46 V om 95 mm2	36 A	16.6 Watt	max 0.17 kW	(+4.2 d Volt)
4 aVolt	**0.72 on 120 mm2**	**72A**	**52 Watt**	**max 0.29 kW**	**(+3.3 a Volt)**
4 dVolt	**0.69 on 120 mm2**	**69A**	**47.6**	**max.0.28 kW**	**(+3.3 d Volt)**

This requirement corresponds to 6 LV power modules of 300 Watt

1 * 2...8 Volt .....25 A, 300 W
1 * 3...15V.....20 A, 300 W
2 * 2..8 V.....50 A, 300 W
2 * 2..8 V.....100A, 300 W

LV Power Totals per PHOS module

Power consumption per FEE card + CSP : .... 7.2 Watt (FEE alone 5.2 Watt)
Power consumption per TRU card: .... 35 Watt (estimated)
Power consumption 1 PHOS module (112 FEE /CSP+ 8 TRU+4 RCU):..... 1.16 kWatt[1]
Power dissipation of LV cables (12):..... 137 Watt
Power delivered by LV supplies FEE/TRU/RCU: ..... 1.3 kWatt
Real power (~20% loss in PS) ..... 1.62 kWatt
Max. PS. supply rating (5 power modules ..... 1.8 kWatt

1. Power consumption for 1 Module in cold zone by CSP 215 Watt

LV Power Total for 5 PHOS modules:

Delivered power by rack with LV supplies for 5 modules ..... 6.5 kWatt
Real power (including ~ 20% conversion loss) ..... 8.1 kWatt
Max. power rating for Rack(s) with 5 module LV supplies ..... 9 kWatt
Power dissipation 60 LV cables for 5 modules..... 0.68 kWatt
(50 % inside magnet, hence ~ 340 Watt inside magnet)

17 Cooling of 1 PHOS module

Each FEE card is enclosed inside copper cassettes like shown in Figure 89 (for geometrical details see Appendix 4 and Appendix 11) which are open on top and bottom for connectors and cables. Copper pipes of 4 mm dia and 65 cm length are soldered to one side the copper cassettes (see Appendix Appendix 5 and Appendix 11) The pipes interconnection between FEE cards consists of plastic pipes. The TRU requires cooling pipes of 6 mm flow diameter.

The copper boxes are needed to cool the dissipation of electronic components on the FEE cards and, using a controlled (underpressurized) water-flow through copper pipes which are soldered to the copper boxes. According to Chapter 16.2 , the power dissipation of one FEE card is 5.2 Watt (without CSP) and of one TRU is 15 Watt. Four FEE / TRU cassettes in a line consitute one water cooling channel between In and Out Manifolds. The cooling pipes are connected as shown in Figure 89

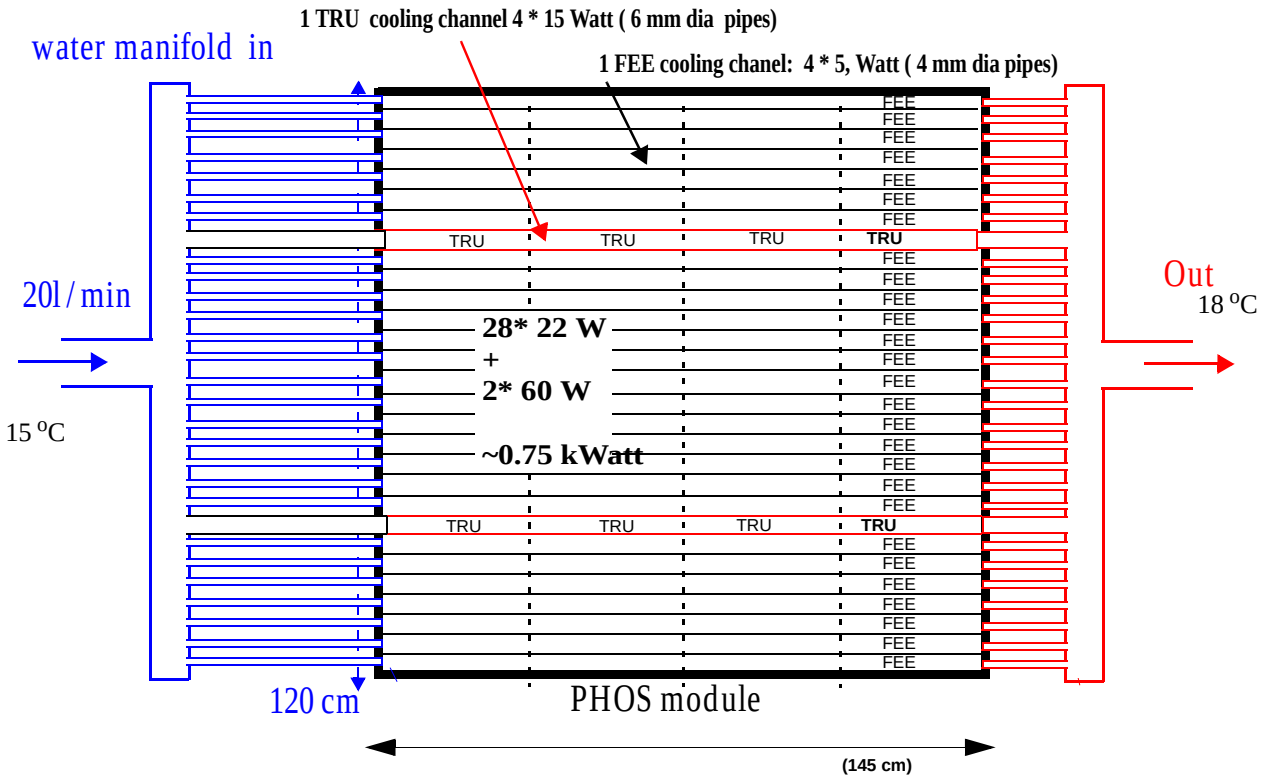


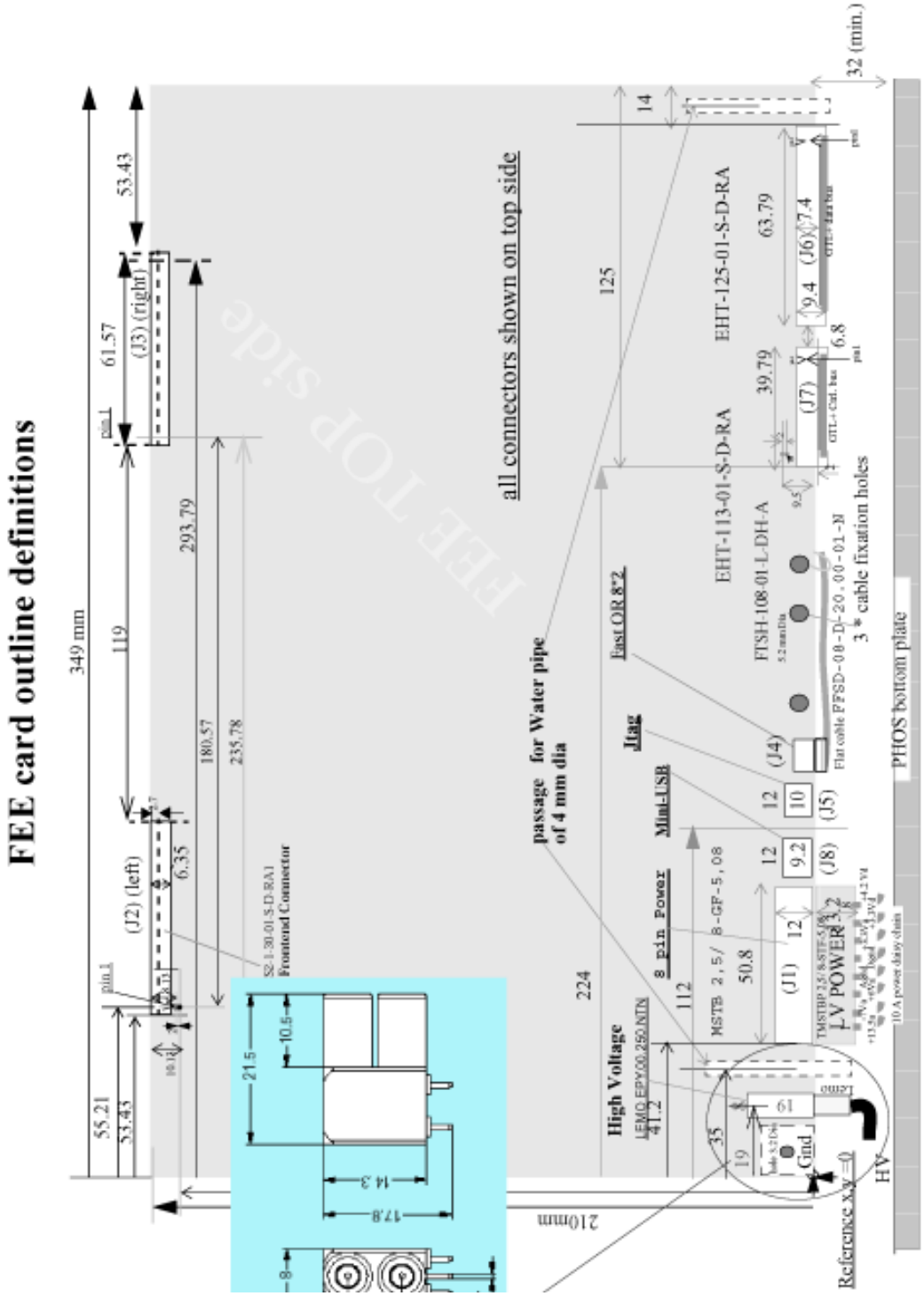
Figure 102 Cooling channels and Water manifold plan for 1 PHOS module

Figure 102 depicts the total cooling situation. A total of 28 FEE cooling channels of 22 Watt and two cooling channels of 60 Watt amount to a cooling power requirement of 0.75 kWatt per warm[1] volume of the PHOS module. The water cooling requires 20 l water per minute per PHOS module. With an In/out pressure drop of 300 mbar and an input water temperature of 15° C in , the output water temperature is ~18 C^{o}

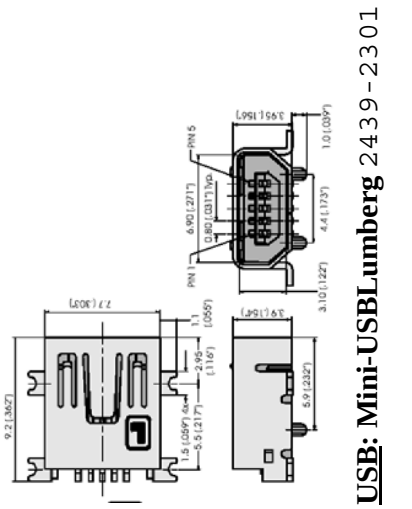
1. note that this counts only for FEE and RCU cards, the CSP and RCU are in different volumes

18 APPENDIX

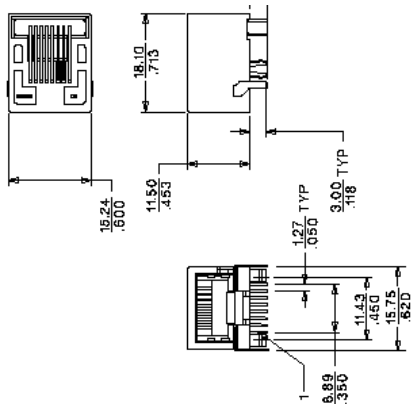
Appendix 1 FEE card embedded dimension



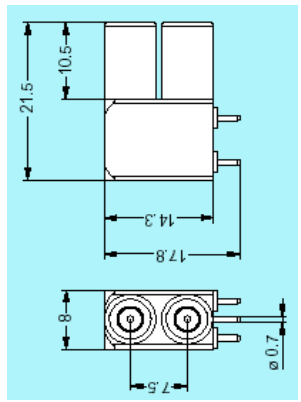
Appendix 2 FEE /CSP connectors



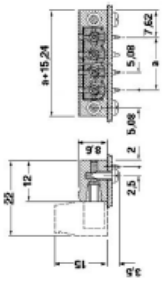
USB: Mini-USBLumberg 2439-2301



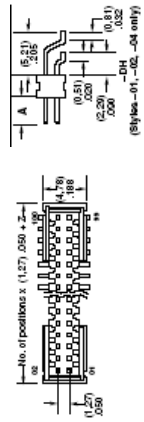
Trigger OUT: RJ45 4* Twisted pair
(Molex PS_95040)



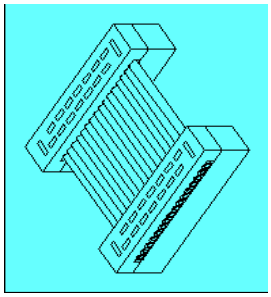
Bias Voltage: Lemo EPY.00.250. NTN



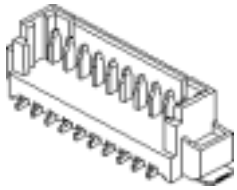
POWER:Phoenix Contact
8 pins max 12 A per pin.
MSTB 2,5/ 8-GF-5,08/ 8-GF-5,08



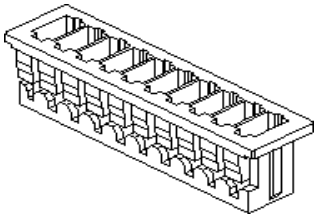
Fast Or: FTSH-108-01-L-DH-A
SAMTEC



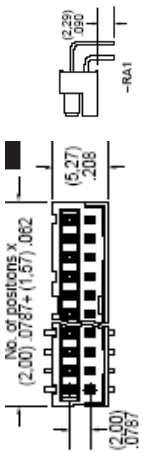
Fast OR cable 16 pin, 1.27 mm
Samtec FFSD-08-D-20
30 AWG / 1A



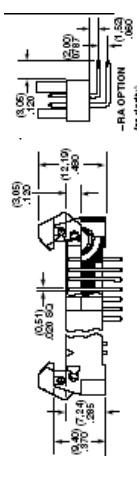
Molex 6 pin header on CSP and T-card
53047-0610



CSP cable: Molex fem.housing 6pin
51021-0600



Front End: LS2-130-01-S-D-RA1
SAMTEC



GTL bus (Data + Control)
EHT-125-01-S-D-RA / EHT-113-01-S-D-RA
SAMTEC

Appendix 3 GTL strip pinout (from TPC)

GTL+ Control bus

SAMTEC MMS-120-01-L-DV - on backplane		
PIN	FNCT	Termination required-technology
1	GND	
2	ERROR_GT	GTL
3	DSTB_GT	GTL
4	ACKN_GT	GTL
5	TRSF_GT	GTL
6	GND	
7	L2_GT	GTL
8	L1_GT	GTL
9	WRITE_GT	GTL
10	CSTB_GT	GTL
11	RST_GT	GTL
12	GND	
13	RDO_CLK	GTL
14	INTERRUPT	GTL
15	SC_DIN	GTL
16	SC_DOUT	GTL
17	SC_CLK	GTL
18	GND	
19	VTT	(to the termination on backplane)
20	VTT	(to the termination on backplane)
21	VTT	(to the termination on backplane)
22	GND	
23	SCLK_DN	On backplane only - LVPECL
24	GND	
25	SCLK_DP	On backplane only - LVPECL
26	GND	
27	PWR SW-1	
28	PWR SW-2	
29	PWR SW-3	
30	PWR SW-4	
31	PWR SW-5	
32	PWR SW-6	
33	PWR SW-7	
34	PWR SW-8	
35	PWR SW-9	
36	PWR SW-10	
37	PWR SW-11	
38	PWR SW-12	
39	PWR SW-13	
40	GND	

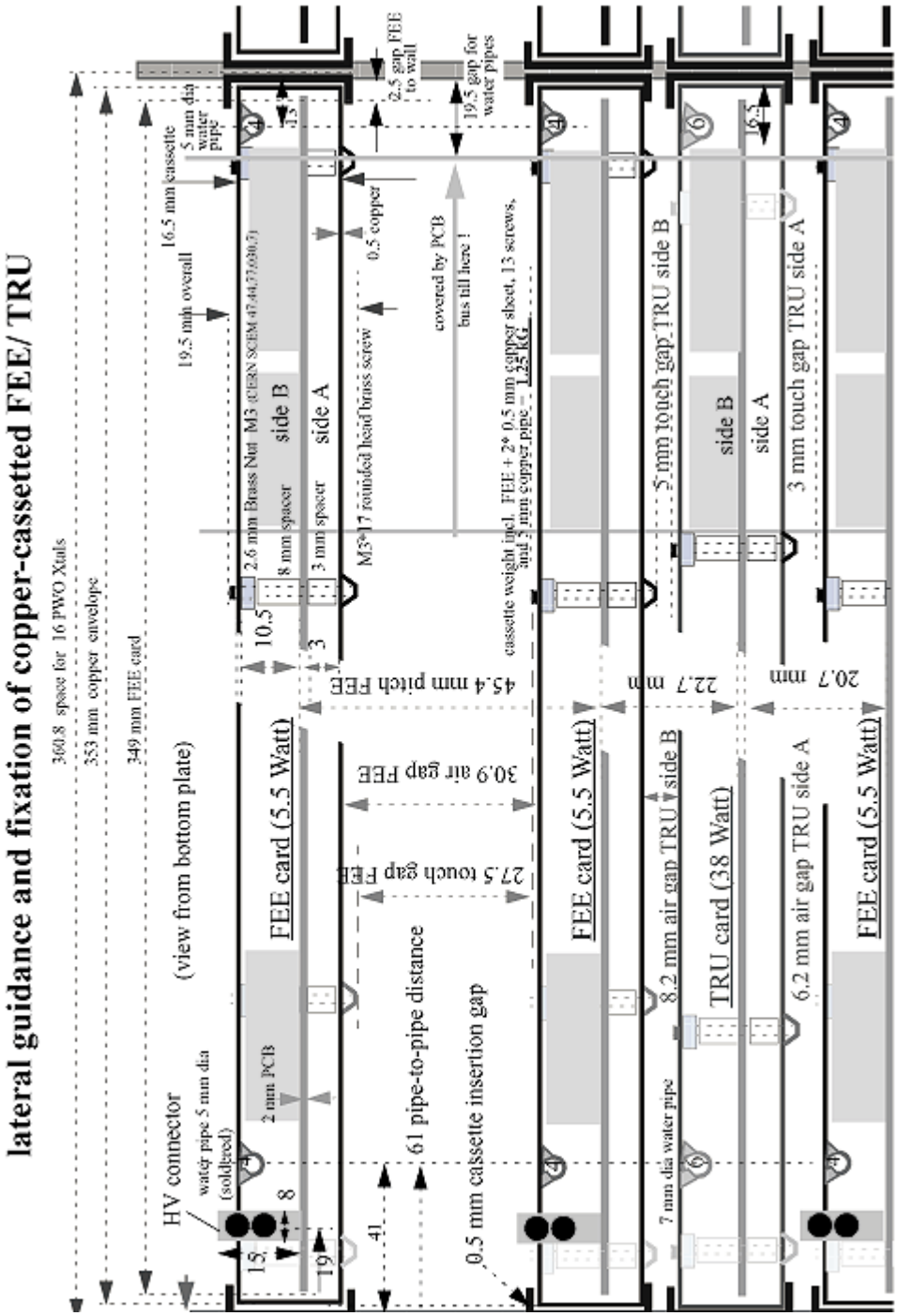
Not on connector

GTL+ Data bus

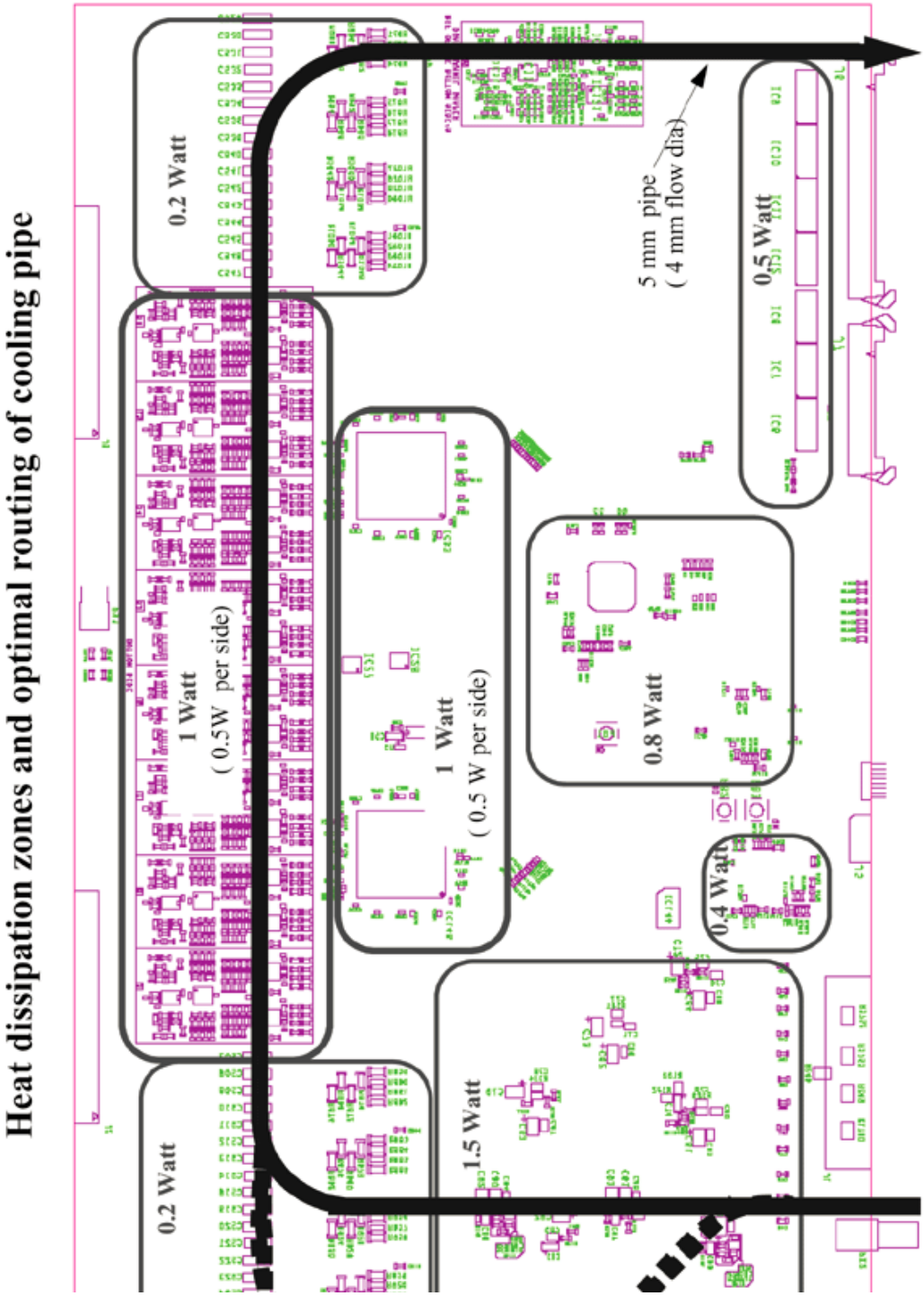
SAMTEC MMS-125-01-L-DV - on backplane		
PIN	FNCT	Termination required-technology
1	GND	
2	D39	GTL
3	D38	GTL
4	D37	GTL
5	D36	GTL
6	D35	GTL
7	GND	
8	D34	GTL
9	D33	GTL
10	D32	GTL
11	D31	GTL
12	D30	GTL
13	GND	
14	D29	GTL
15	D28	GTL
16	D27	GTL
17	D26	GTL
18	D25	GTL
19	GND	
20	D24	GTL
21	D23	GTL
22	D22	GTL
23	D21	GTL
24	D20	GTL
25	GND	
26	D19	GTL
27	D18	GTL
28	D17	GTL
29	D16	GTL
30	D15	GTL
31	GND	
32	D14	GTL
33	D13	GTL
34	D12	GTL
35	D11	GTL
36	D10	GTL
37	GND	
38	D9	GTL
39	D8	GTL
40	D7	GTL
41	D6	GTL
42	D5	GTL
43	GND	
44	D4	GTL
45	D3	GTL
46	D2	GTL
47	D1	GTL
48	D0	GTL
49	VTT	(to the termination on backplane)
50	VTT	(to the termination on backplane)

Figure 103 pinout of GTL bus (adopted from Alice TPC)

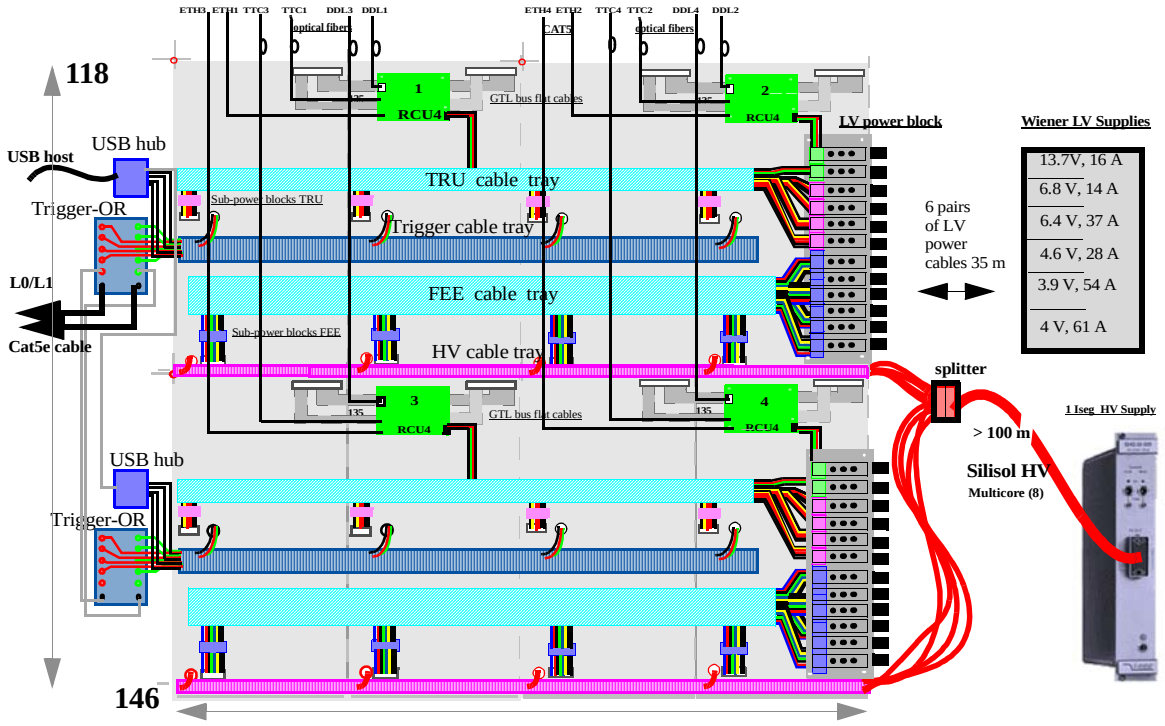
Appendix 4 Air gaps for mounted FEE and TRU cards



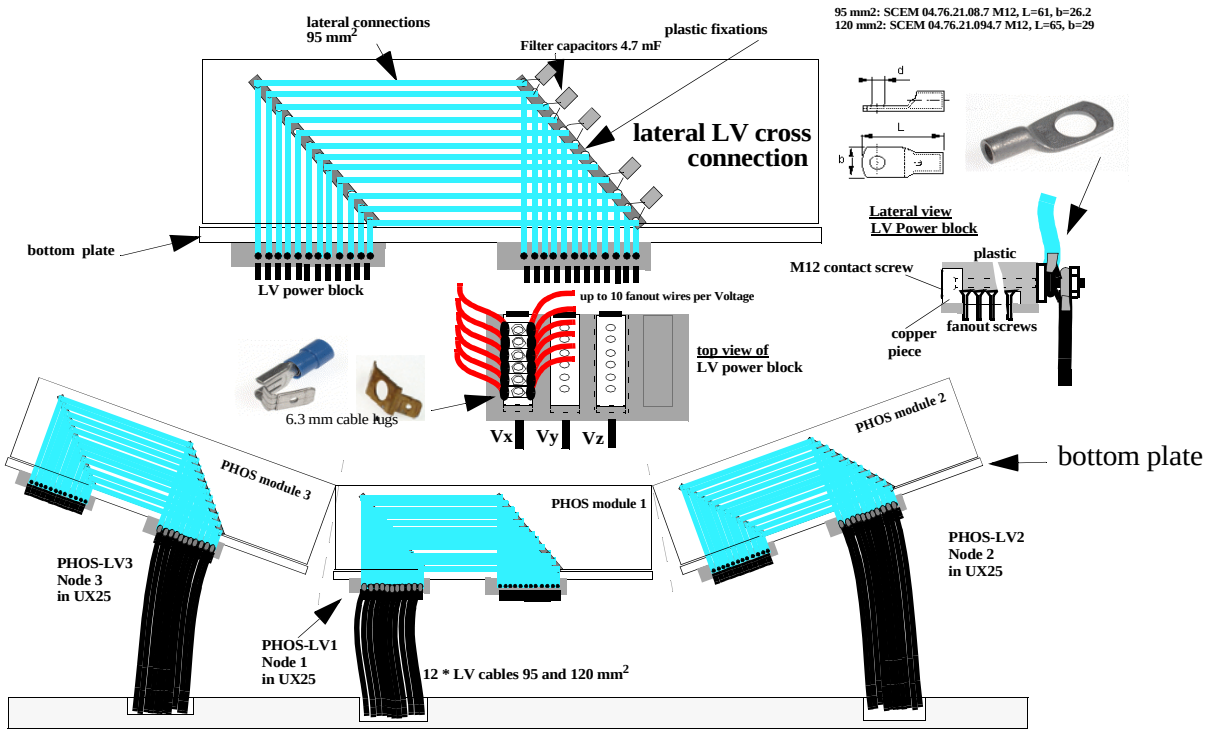
Appendix 5 Cooling pipe and heat areas



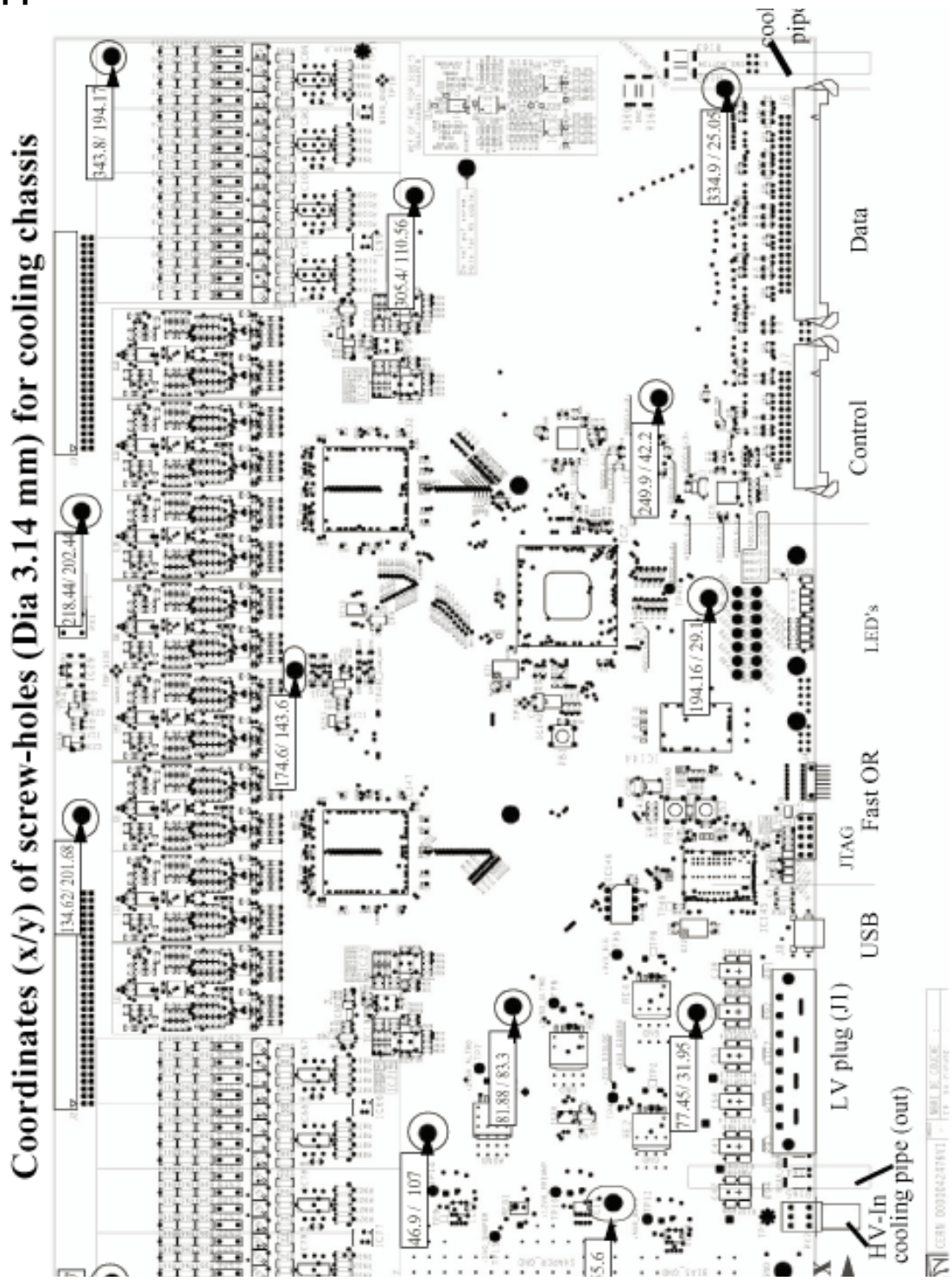
Appendix 6 Cabletrays on PHOS bottom plate



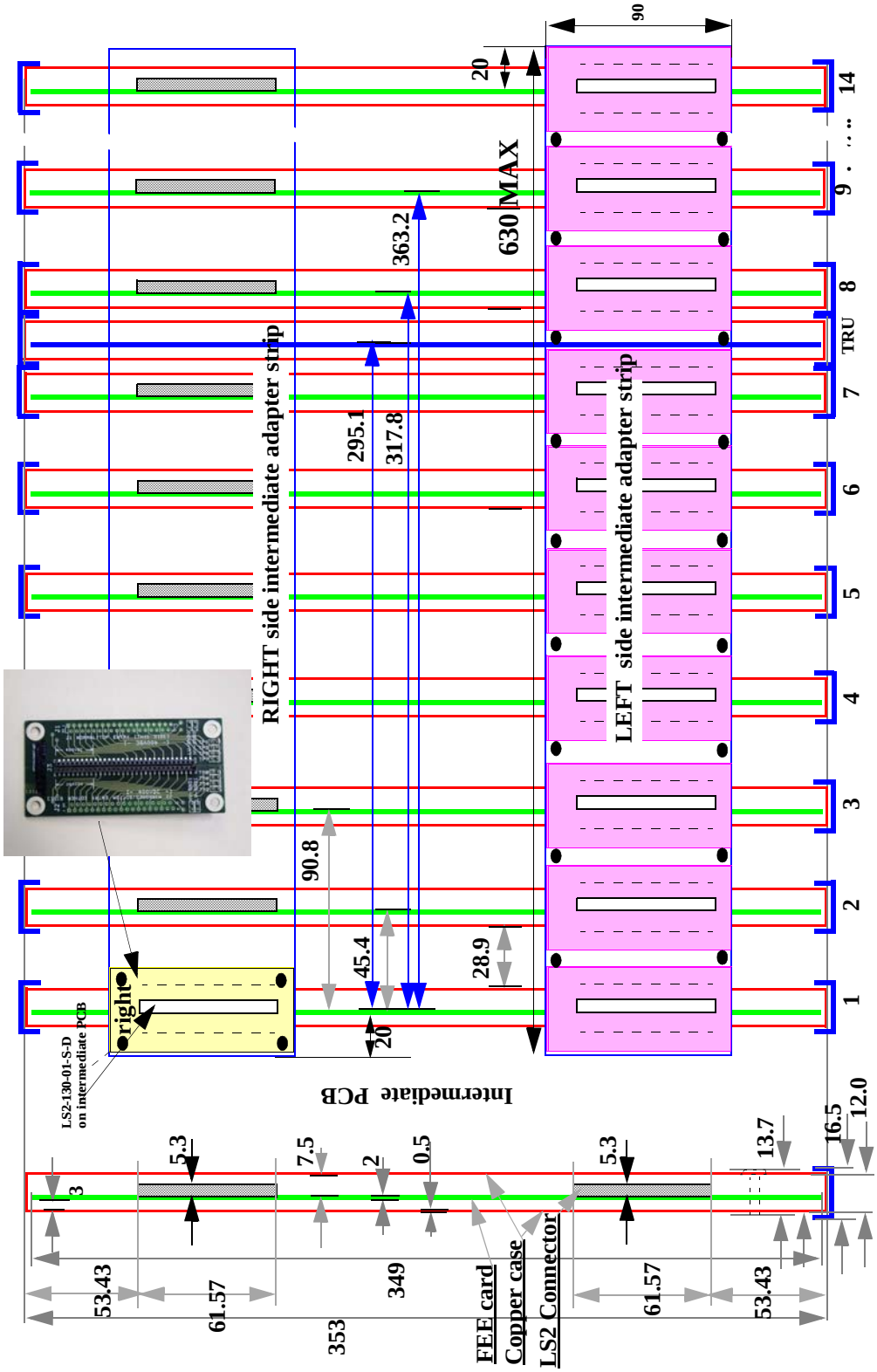
LV power distribution in UX25



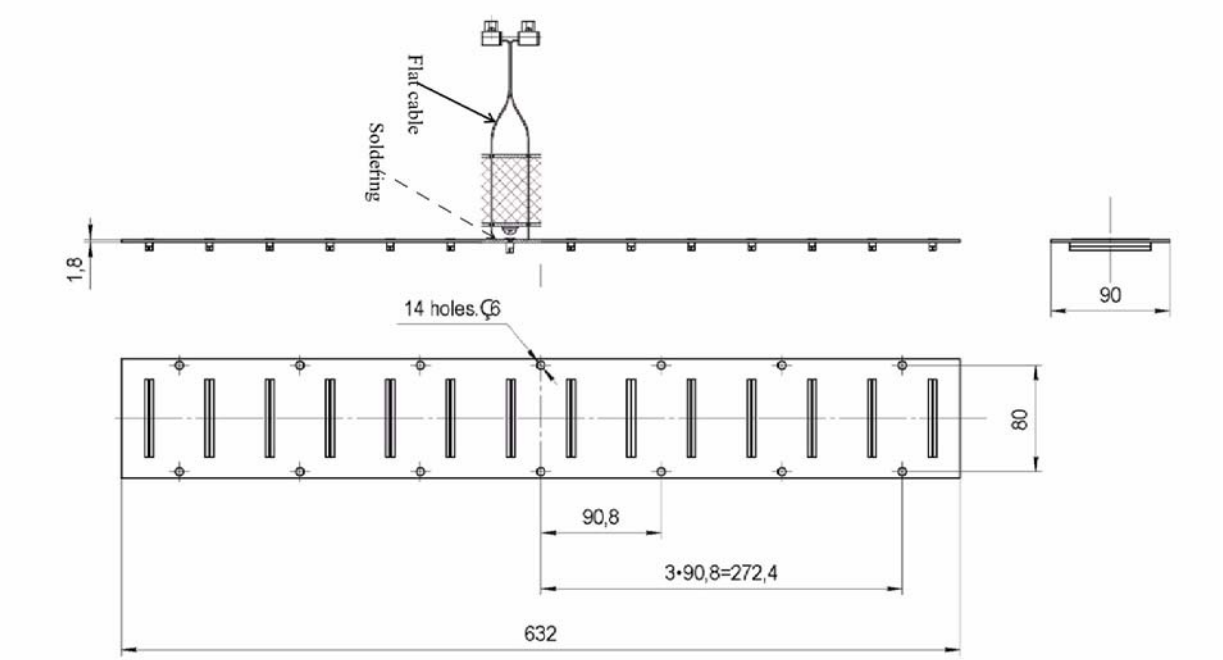
Appendix 7 Fixation Holes on FEE card

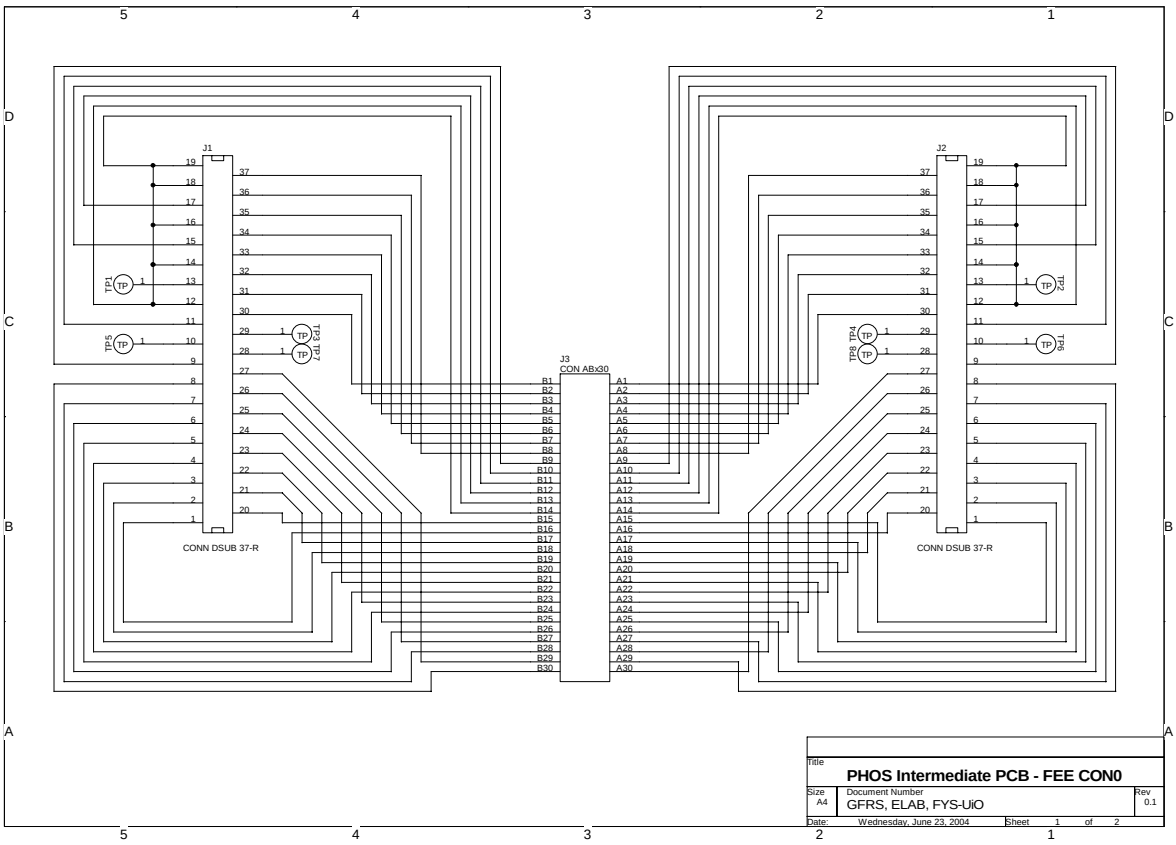


Appendix 8 Adaper PCB strip for FEE card front connectors

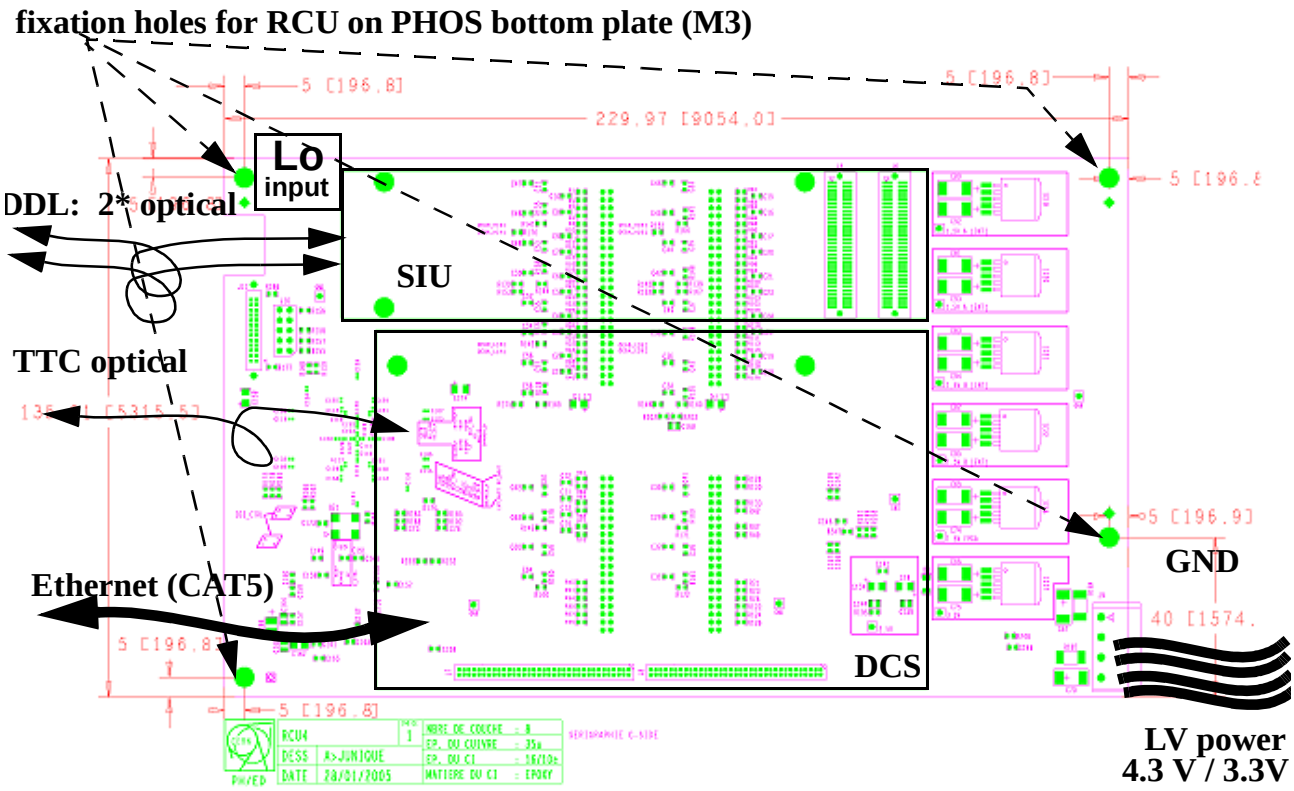


Appendix 9 Intermediate PCB

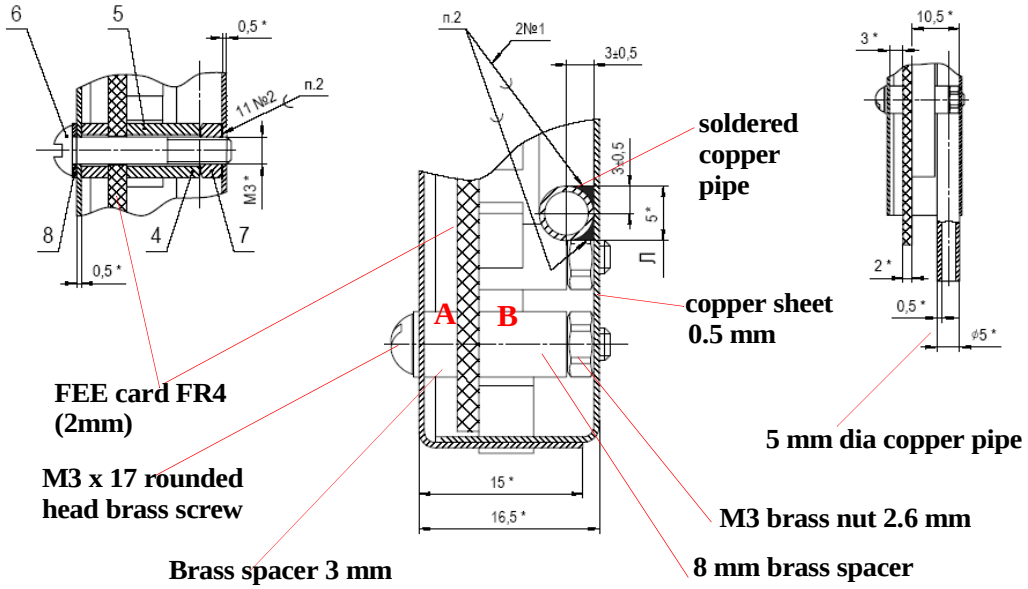




Appendix 10 RCU dimensions and Power/Signal cables indications



Appendix 11 FEE cooling cassette dimensions



Appendix 12 All FEE card components (except R and C)

LICE PHOS Front End Card v1.1 (CERN-0000042476)
rototype 2 C/W shaper [for (4us shaper) mount (Pref)] [for (2us shaper) replace by (Alt1*)]
ate: 2005/01/27

rt Name	JEDEC_TYPE	Reference of components	VALUE	VOLTAGE	Qty	MANUFACTURER	PART_NUMBER	DESCRIPTION
LC256	DIP8_3	IC146			1	MICROCHIP	24LC256	256K I2C CMOS SERIAL EEPROM
GTL16612_TSSOP	TSSOP56MC_050	IC6,IC7,IC8,IC9,IC10,IC11,IC12			7	TEXAS_INSTRUMENTS	GTLPH16612DGG	
7417_TSSOP	TSOP16MA_065	IC13,IC14,IC15			3	ANALOG DEVICES	08.AD7417ARU	
8039_SOIC	SOIC8S_127	IC34,IC38,IC42,IC46,IC50,IC54,IC58,IC62,IC110,IC114,			16	ANALOG DEVICES	AD8039AR	VOLTAGE FEEDBACK AMPLIFIERS
		IC118,IC122,IC126,IC130,IC134,IC138						
8544	SOIC14S_127	IC67,IC68,IC78,IC79,IC89,IC90,IC100,IC101			8	ANALOG DEVICES	AD8544AR	
TRO-ST	TQFP176_050	IC32,IC33,IC147,IC148			4	CERN	ALTRO-ST	
T54	SOT23	U1,U2,U3,U4,U5,U6,U7,U8			5	PHILIPS	BAT54	SCHOTTKY <.1A
N10P-BARD2X5	CONHE13D2X5M	J5			1		BARD2X5	FLAT CABLE CONN. 2.54mm
N16P-FTSH_10801LDH	CON16MC	J4			1	SAMTEC	FTSH10801LDHK	1.27mm MICRO HEADER FTSH
N26P-EHT113_RA_LC	CON26MC	J7			1	SAMTEC	EHT11301SDRALC	2MM EJECTOR HEADER EHT
N50P-EHT125_RA_LC	CON50MC	J6			1	SAMTEC	EHT12501SDRALC	2MM EJECTOR HEADER EHT
N5P-USB_0578	CON5USB_0578	J8			1	MOLEX	USB_0578	MINI USB TYPE B 90D SMD
N60P-LS2_13001RA1	CON60MFC_LS2	J2,J3			2	SAMTEC	LS213001SDRA1	2MM TERMINAL/SOCKET LS2
N8P-MSTB258GF508	CON8MC_258GF508	J1			1	PHOENIX CONTACT	MSTB258GF508	EMBASES MINICONNEC 5.08MM
7C68013_TQFP128	TQFP128R_050	IC145			1	CYPRESS	CY7C68013_128AC	USB MICROCONTROLLER
ODE_TRANS-SUP-1.5KE-400CA	DO201AE	D7	.5KE-400CA		1	PANJIT	1.5KE400CA	TRANSIENT VOLTAGE SUPPRES
1K100-208_PQFP	PQFP208_050	IC2			1	ALTERA	EP1K100-208	
C16	PQFP100R_065	IC144			1	ALTERA	EPC16	
C452	SOIC4MA_254	IC69,IC70,IC71,IC72,IC73,IC74,IC75,IC76,IC80,IC81,			32	COSMO	KPC452	PHOTO COUPLER
		IC82,IC83,IC84,IC85,IC86,IC87,IC91,IC92,IC93,IC94,						
		IC95,IC96,IC97,IC98,IC102,IC103,IC104,IC105,IC106,						
		IC107,IC108,IC109						
D-HSMG-C670	D0805	D1,D3,D4,D5,D6			5	AGILENT	HSMG-C670	LED SMD GREEN HP TYPE 0805
D-HSMY-C670	D0805	D2			1	AGILENT	HSMY-C670	LED SMD YELLOW HP TYPE 0805
D-HSMH-C670	D0805	D8			1	AGILENT	HSMH-C670	LED SMD RED HP TYPE 0805
4040-CIM3-2.5V,0.5%	SOT23	IC26			1	MICREL	LM4040CIM3-2.5	Precision Micropower Shunt VoltageReferenc
4041_1V2	SOT23	IC1,IC25			2	NATIONAL SEMI.	LM4041_1V2	
1175_SOIC	SOIC8S_127	REG1			1	LINEAR	LT1175CS8_5	MICROPOWER REGULATOR
X4454_TSSOP	TSSOP14MA_065	IC19,IC20,IC21,IC22,IC23,IC24,IC35,IC36,IC37,IC39,			54	MAXIM	MAX4454EUD	OP AMP WITH RAIL-TO-RAIL OUTPUT
		IC40,IC41,IC43,IC44,IC45,IC47,IC48,IC49,IC51,IC52,						
		IC53,IC55,IC56,IC57,IC59,IC60,IC61,IC63,IC64,IC65,						
		IC111,IC112,IC113,IC115,IC116,IC117,IC119,IC120,						
		IC121,IC123,IC124,IC125,IC127,IC128,IC129,IC131,						
		IC132,IC133,IC135,IC136,IC137,IC139,IC140,IC141						
X5308_TSSOP	TSSOP16MA_065	IC66,IC77,IC88,IC99			4	MAXIM	MAX5308EUE	OCTAL 10-BIT VOLTAGE-OUTPUT DACs
X6033-A,5.0V	SOT23_6	IC30,IC31		5.0V	2	MAXIM	MAX6033AAUT50-T	ULTRA-HIGH PRECISION VOLTAGE REF.
C29151_TO263_5-3.3V	TO263_5	RE4		3.3V	1	MICREL	MIC29151-3.3BU	1.5Amp HIGHT-CURRENT LDO REGULATOR
C39151_TO263	TO263_5	RE1,RE2,RE3		2.5V	3	MICREL	MIC39151-2.5BU	1.5Amp HIGHT-CURRENT LDO REGULATOR
C5239_SOIC-5.0V	SOIC8S_127	IC16,IC18		5.0V	2	MICREL	MIC5239-5.0BM	500 mA uCAP LDO
C5239_SOIC-ADJ	SOIC8S_127	IC17		ADJ	1	MICREL	MIC5239BM	500 mA uCAP LDO
C940L	TQFP32_080	IC3,IC4,IC5			3	MOTOROLA	MPC940LFA	CLOCK DISTRIBUTER CHIP
A4364_TSSOP	TSSOP14MA_065	IC27,IC28,IC29,IC149,IC150			5	BURR-BROWN	OPA4364AIPW	HIGT PERFORMANCE CMOS OPAMP
EMO2CI-DUPLEX-VME	DUPLEX_VME	PX2			1	LEMO	DUPLEX_VME	LEMO DUPLEX SIZE 50OHM RA HORIZONTA
SMD4P-24MHZ,14SMX	QZSMD4P_75X50	QZ2	24MHz		1	C-MAC	24MHZ14SMX-5050	XTAL 24MHz
SMD4P_VS-40MHZ,CFPT_125	QZSMD4P_5X7	QZ1	40MHz		1	C-MAC	40MHz_CFPT125	OSCILATOR TRI-STATE HCMOS (3.3V) 40MH
SMD-2K2 0.031W 1%	LCC10_1206	RS1	2K2		1	PHICOMP		8 RES-NETWORK WITH COMMON
74CBTLV1G125	SOT23_5	IC151,IC152,IC153,IC154			4	TEXAS INSTRUMENTS	SN74CBTLV1G125DBVR	Low-Voltage Single FET Bus Switch
2222A	SOT23	Q1,Q2			2	ST		SMALL SIGNAL NPN TRANSISTOR
PB1UNI-SKHHAJA010	SW4PMJTP1230	PB1,PB2,PB3			3	ALPS	SKHHAJA010	MOMENTARY PUSHBUTTON
SL2POL3POS-25149NAB	SW6P_141X125	SW1			1	APEM	25149NAB	Slide Switch 2pol 3pos ON-OFF-ON
C7733_SOIC	SOIC8S_127	IC142,IC143			2	TEXAS INSTRUMENTS	TLC7733ID	
SFET_GSD-FDV301N,SOT23	SOT23	T1,T2	FDV301N		2	FAIRCHILD	FDV301N	Digital FET, N_Channel
NER_SOT23-BZX84C8V2	SOT23	Z1,Z2			2	FAIRCHILD	BZX84C8V2	ZENER DIODE 350mW
SOCKET 8 Pin 2.54mm		To Place in the IC146 place			1			IC Socket
EX.CABL.WIRE,RED 0,50mm2		H.V. Cable to connect TP1 to TP11 through H.V hole			1	HUBER SUHNER	12516089-665834	(Radox 125 Flexibel 0.5 mm)2 ~40cm per bos
assis ties 2mm		Tie up H.V cable to the 2 middle holes of PCB near RS2 and PB1			2			www.hellermanntyton.co.uk/HT/dokument?id=9465
BULATING TAPES – KAPTON		Tape to insulate the H.V. Disk capacitors Top and bottom						

Appendix 13 FEE card 10 layer stackup

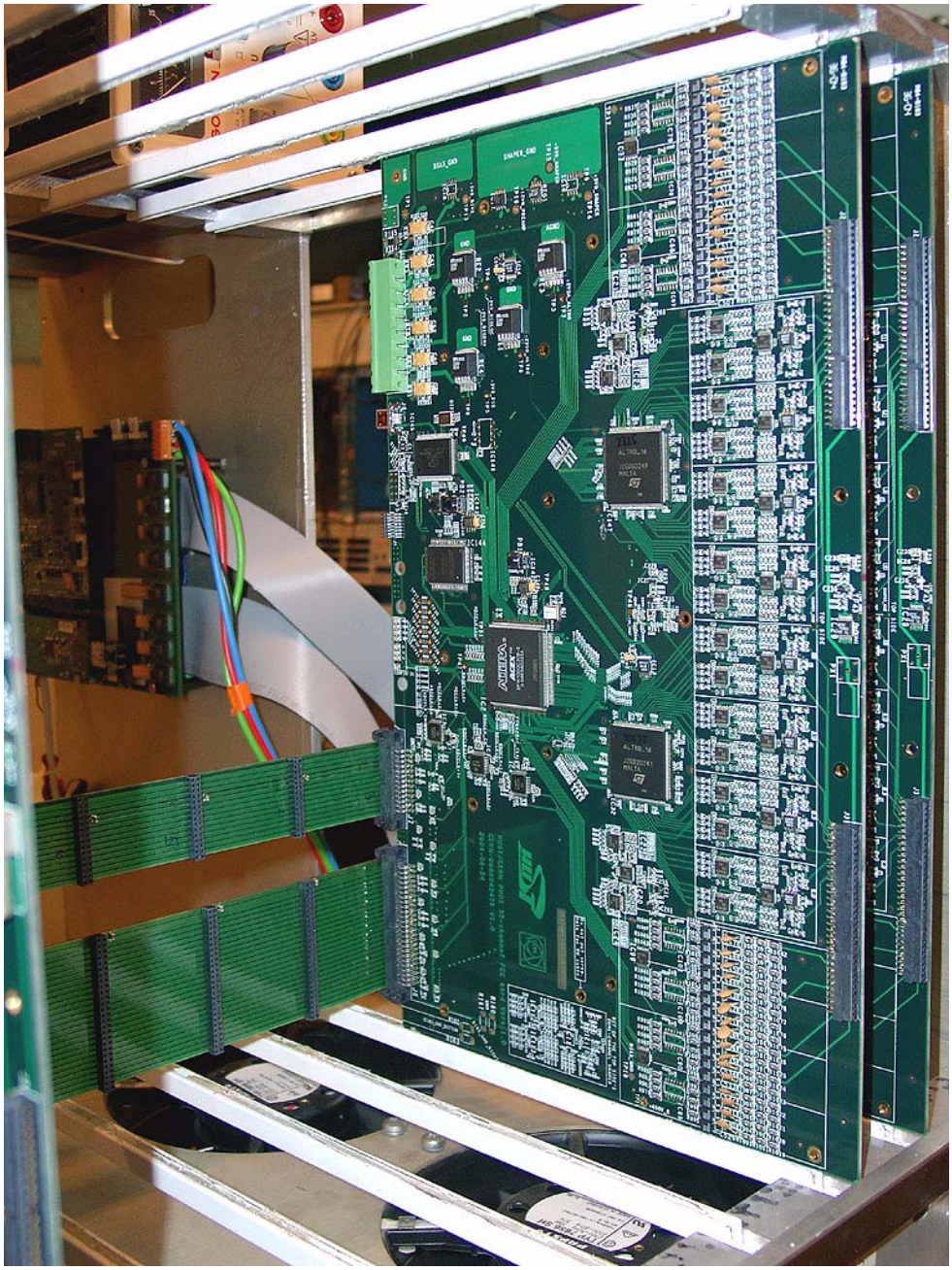
FEE card 10 layer stackup

ALICE FEE –Printed Circuit Board Stack-Up

(10 conductive layers PCB, Total thickness 1800~2000 µm.)

Note: The Ppreg Layer is composed by two types of semi-solidified slices.Their types are 1080 and 2116,whose thickness are 2.6mil and 4.2mil respectively.The final thickness of Ppreg layer can be adjusted to fit the total thickness of the FEE board.

Appendix 14 FEE cards in test cradle with GTL bus and RCU



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