

SER/DES CONNECTOR

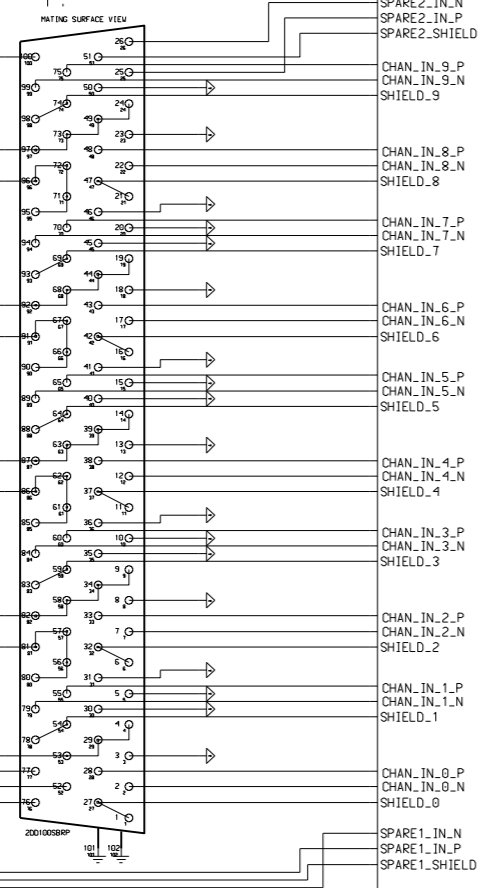
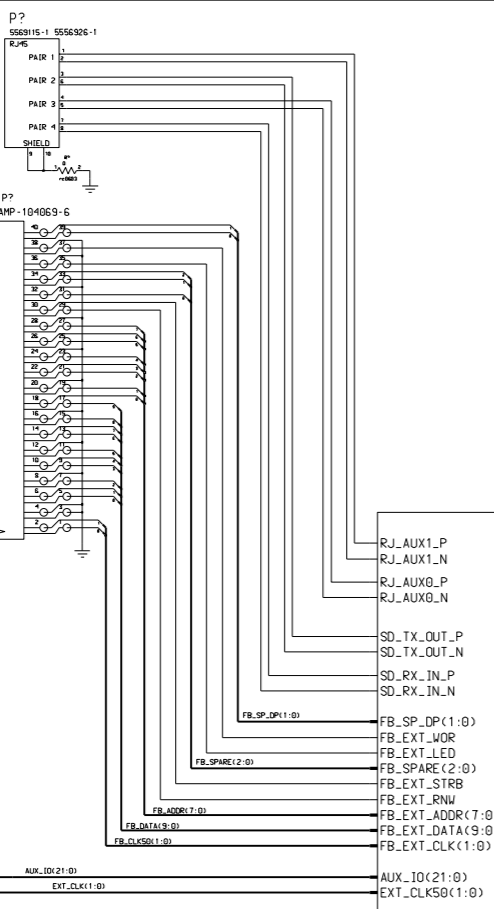
FRONTBUS CONNECTOR

AUX INTERFACE

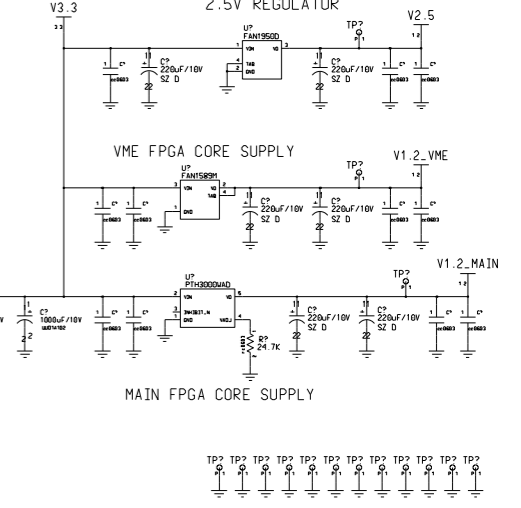
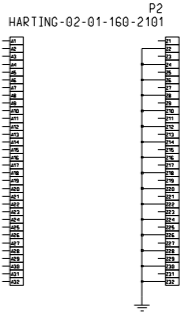
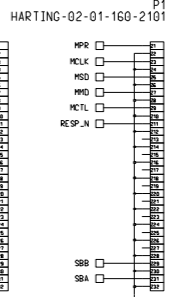
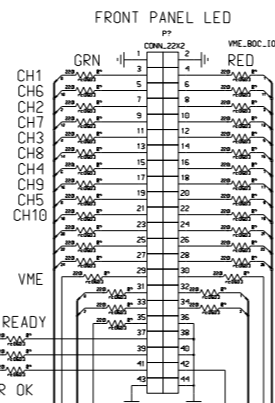
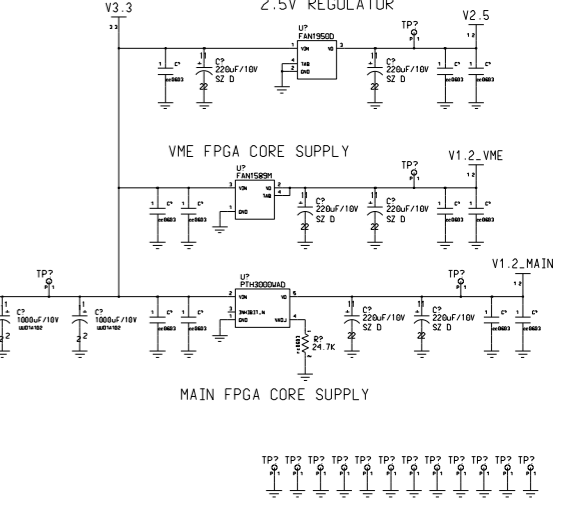
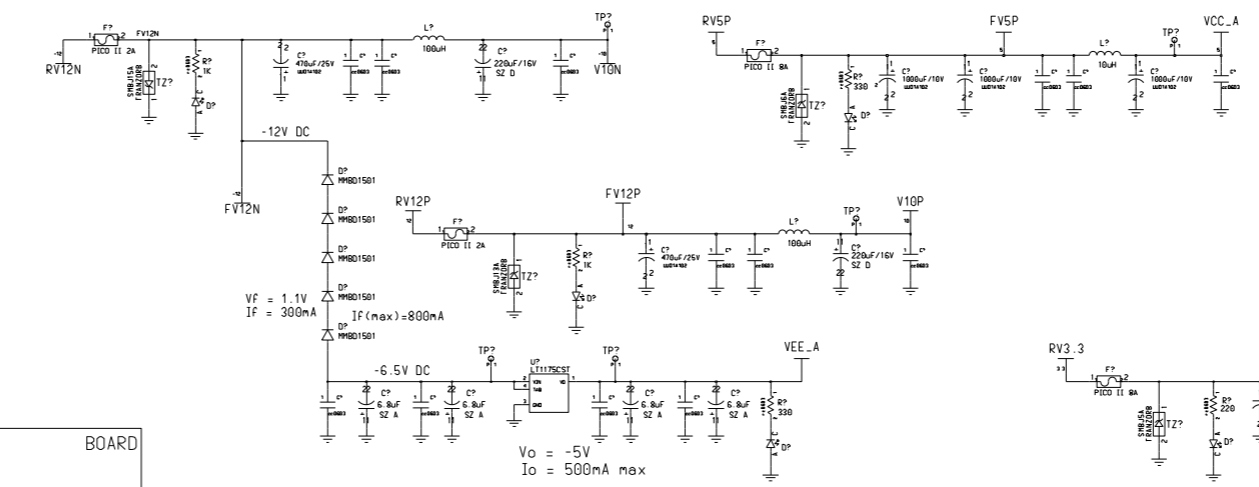
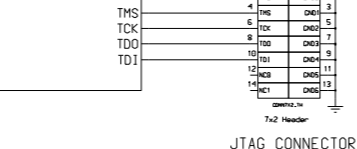
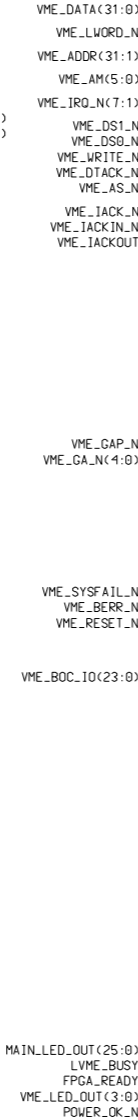
FE INPUT CONNECTOR

CENTER CONTACT REPEATER OUTPUT

ANALOG DAC OUTPUTS

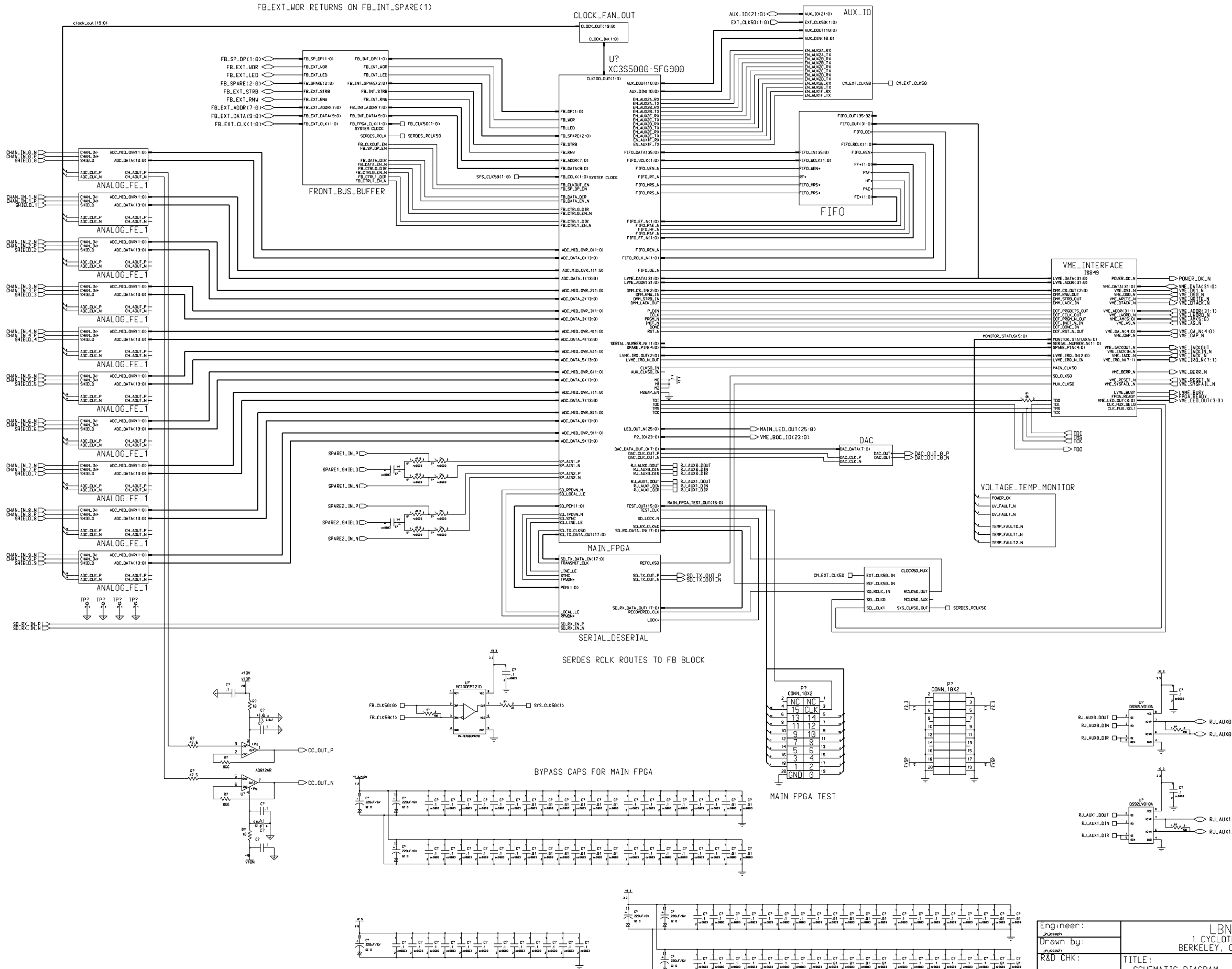


BOARD



Engineer:	LBNL 1 CYCLOTRON RD BERKELEY, CA 94720	
Drawn by:	TITLE: SCHEMATIC DIAGRAM, GRETINA - 10 CHANNEL DIGITIZER TOP REV 4.1	
R&D CHK:	DOC CTRL CHK:	MFG ENGR CHK:
QA CHK:	REV: 4.1	DWG NUMBER: 31Y334
Changed by:	Date Changed: Thursday, September 4, 2008	Time Changed: 10:04:18 am
Page:	8	Page:

FB\_EXT\_LED RETURNS ON FB\_INT\_SPARE(2)  
 FB\_EXT\_WOR RETURNS ON FB\_INT\_SPARE(1)



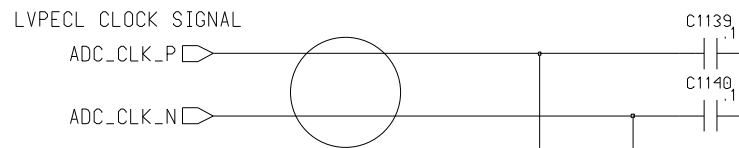
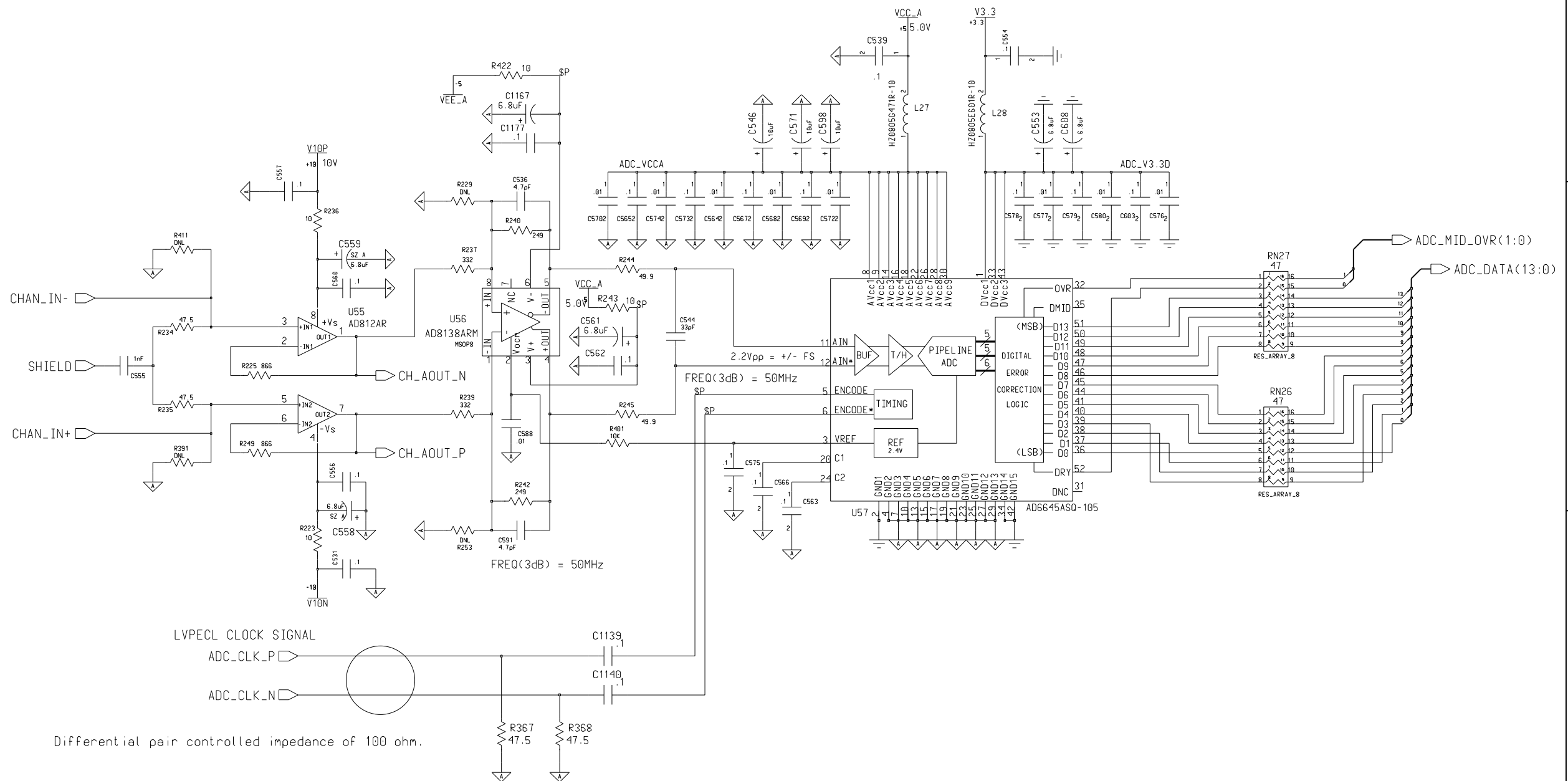
Engineer: J. Joseph  
 Drawn by: J. Joseph  
 R&D CHK: J. Joseph  
 DOC CTRL CHK: J. Joseph  
 MFG ENGR CHK: J. Joseph

LBNL  
 1 CYCLOTRON RD  
 BERKELEY, CA 94720

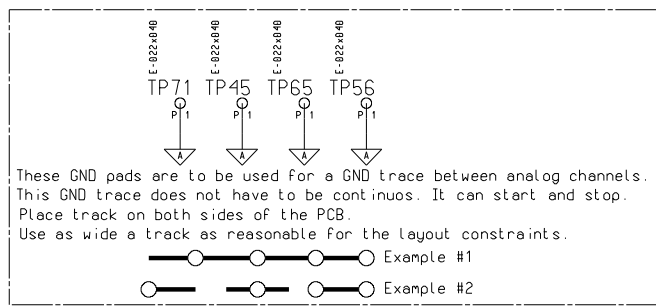
TITLE: SCHEMATIC DIAGRAM, GRETINA - 10 CHANNEL DIGITIZER BOARD BLOCKS

SIZE: 8.1 x 8.6

Changed by: J. Joseph  
 Date Changed: Wednesday, April 25, 2007  
 Time Changed: 12:09:14 pm  
 QA CHK: J. Joseph  
 REV: 4.1  
 DWG NUMBER: 31Y334  
 Page: 1



Differential pair controlled impedance of 100 ohm.

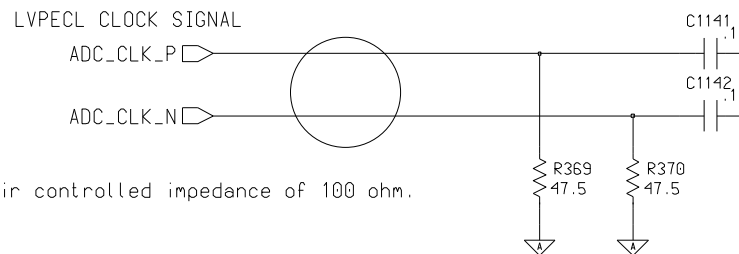
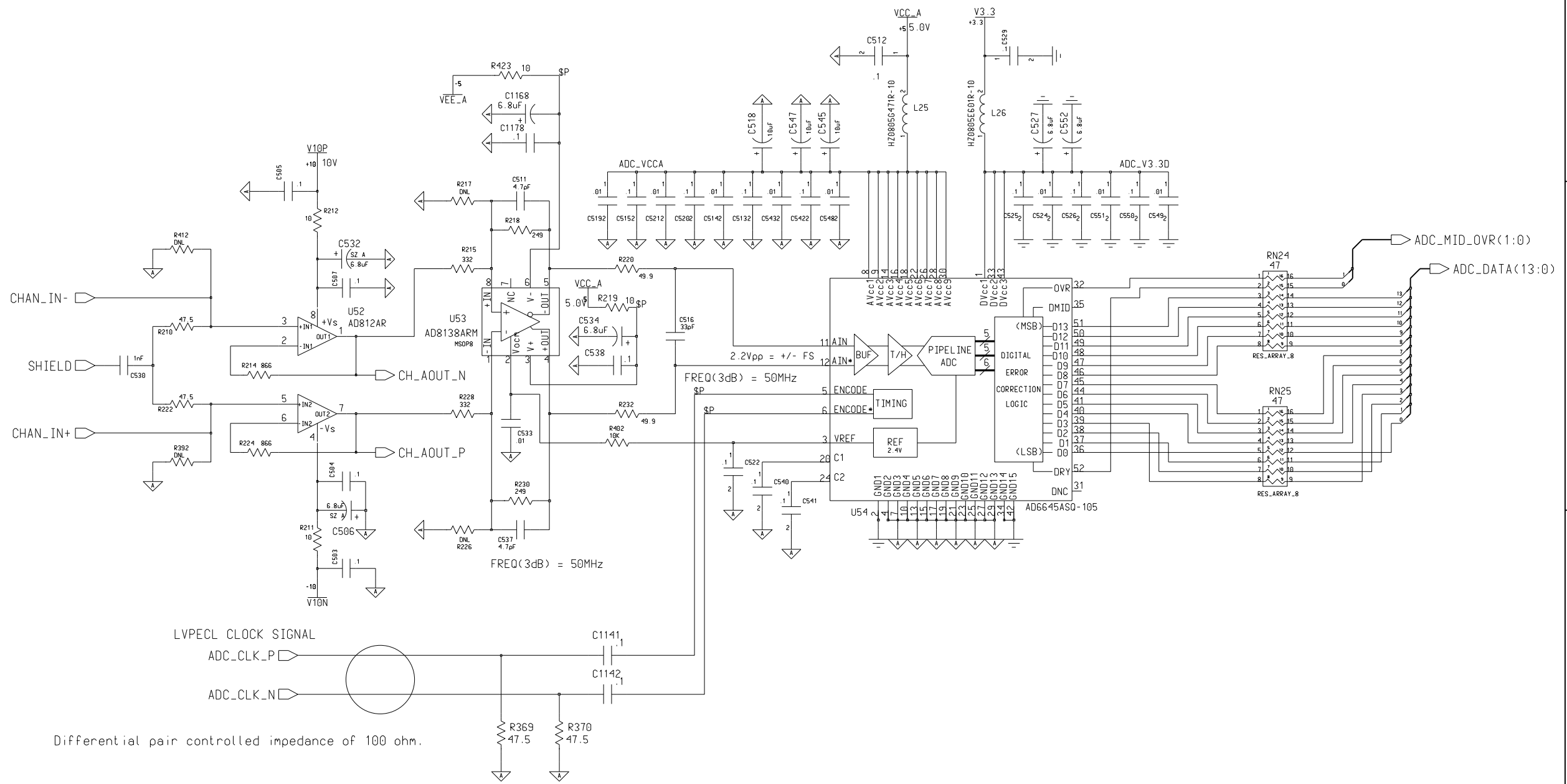


These GND pads are to be used for a GND trace between analog channels. This GND trace does not have to be continuous. It can start and stop. Place track on both sides of the PCB. Use as wide a track as reasonable for the layout constraints.

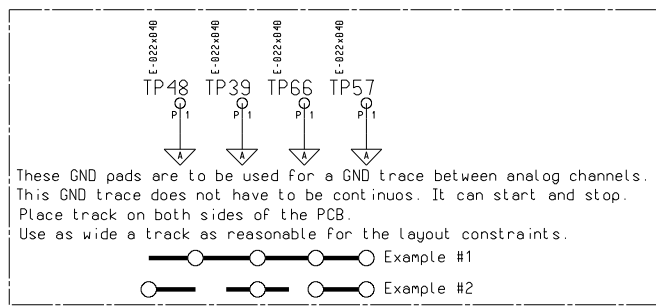
AD8138 GAIN	CHAN
0.25	0 (CC)
0.75	1-9 (SEG)

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: Harold Yaver			TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END
R&D CHK:	REV:		Page: 1
DOC CTRL CHK:	Drawing Number:		
MFG ENGR CHK:	QA CHK:		

Changed by: jn_joseph	Date Changed: Wednesday, April 25, 2007	Time Changed: 12:14:38 pm	QA CHK:	REV:	Drawing Number:	Page: 1
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Differential pair controlled impedance of 100 ohm.

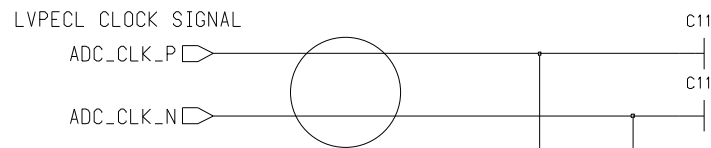
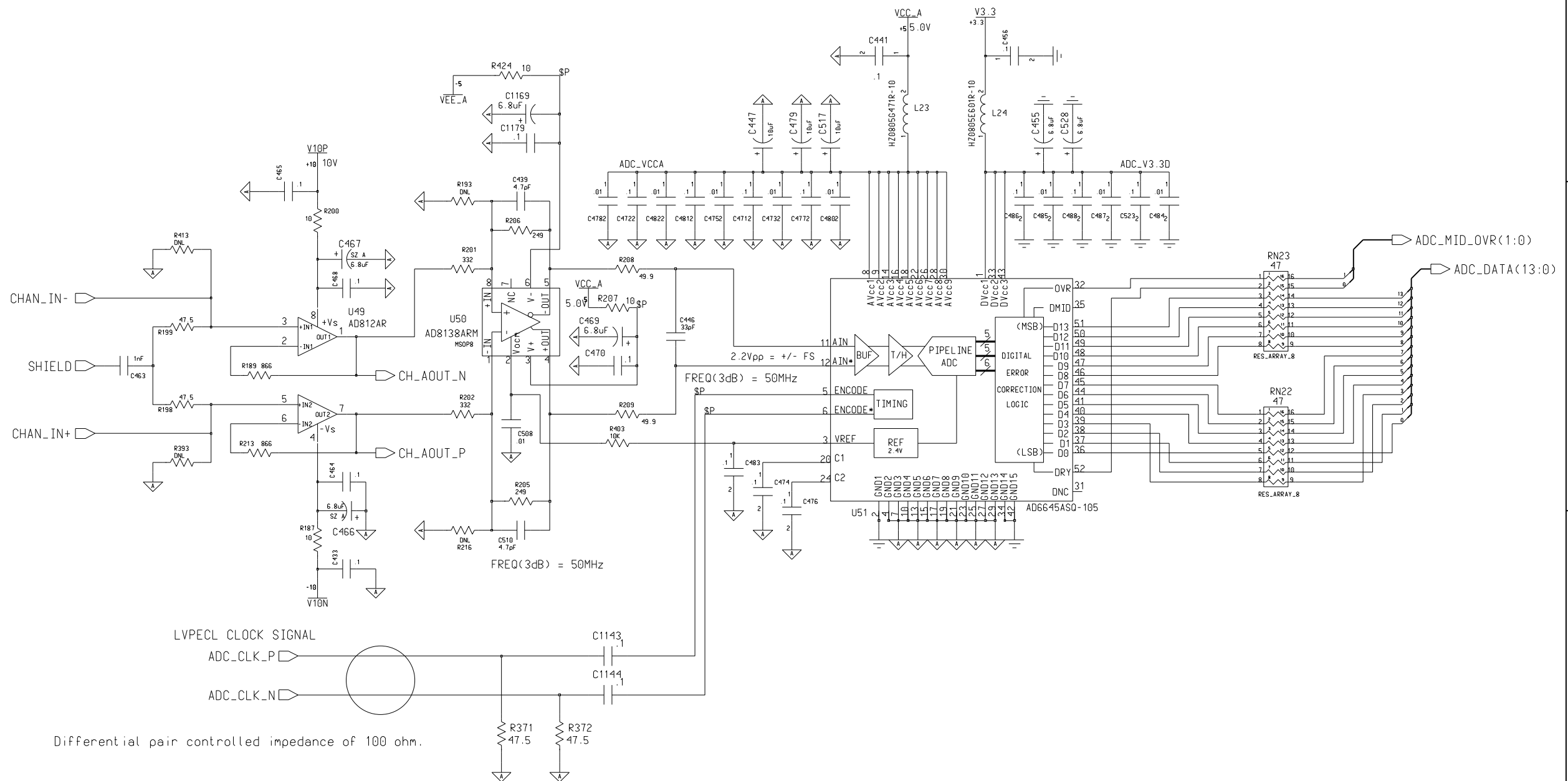


These GND pads are to be used for a GND trace between analog channels. This GND trace does not have to be continuous. It can start and stop. Place track on both sides of the PCB. Use as wide a track as reasonable for the layout constraints.

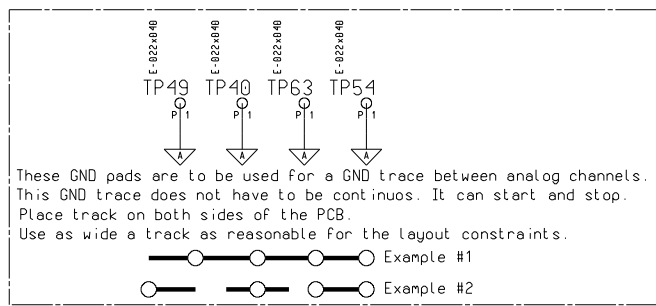
AD8138 GAIN	CHAN
0.25	0 (CC)
0.75	1-9 (SEG)

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: Harold Yaver			
R&D CHK:	TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END		414 A
DOC CTRL CHK:			
MFG ENGR CHK:			

Changed by: jn_joseph	Date Changed: Wednesday, April 25, 2007	Time Changed: 12:14:38 pm	QA CHK:	REV:	Drawing Number:	Page: 1
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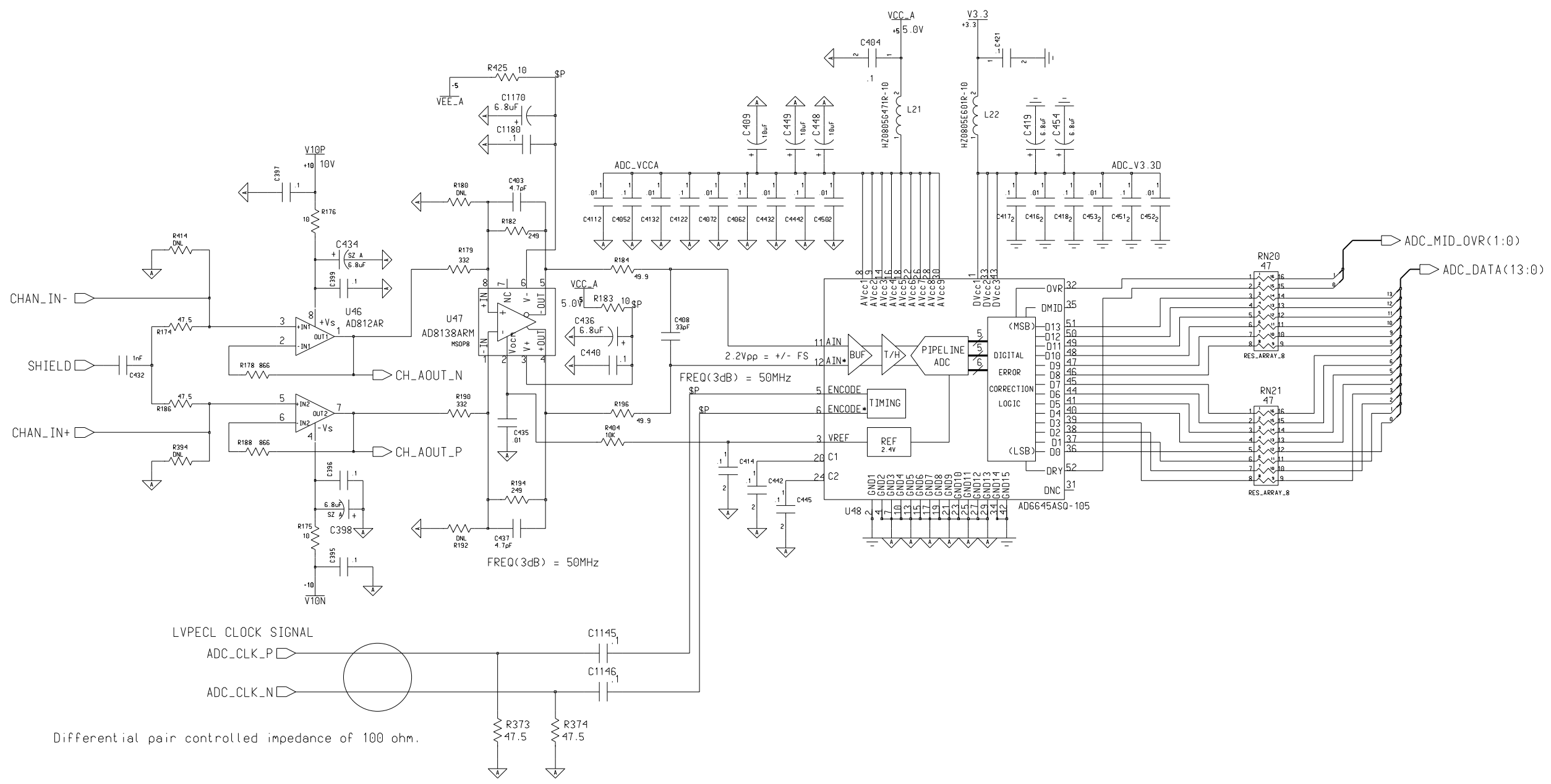
Differential pair controlled impedance of 100 ohm.



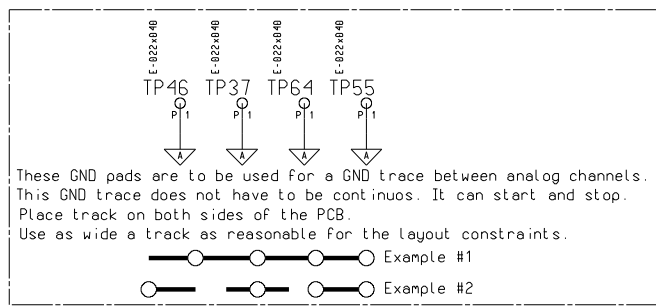
AD8138 GAIN	CHAN
0.25	0 (CC)
0.75	1-9 (SEG)

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: Harold Yaver			TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END
R&D CHK:	REV:		
DOC CTRL CHK:	Drawing Number:		
MFG ENGR CHK:	Page:		

Changed by: jn_joseph	Date Changed: Wednesday, April 25, 2007	Time Changed: 12:14:38 pm	QA CHK:	REV:	Page: 1
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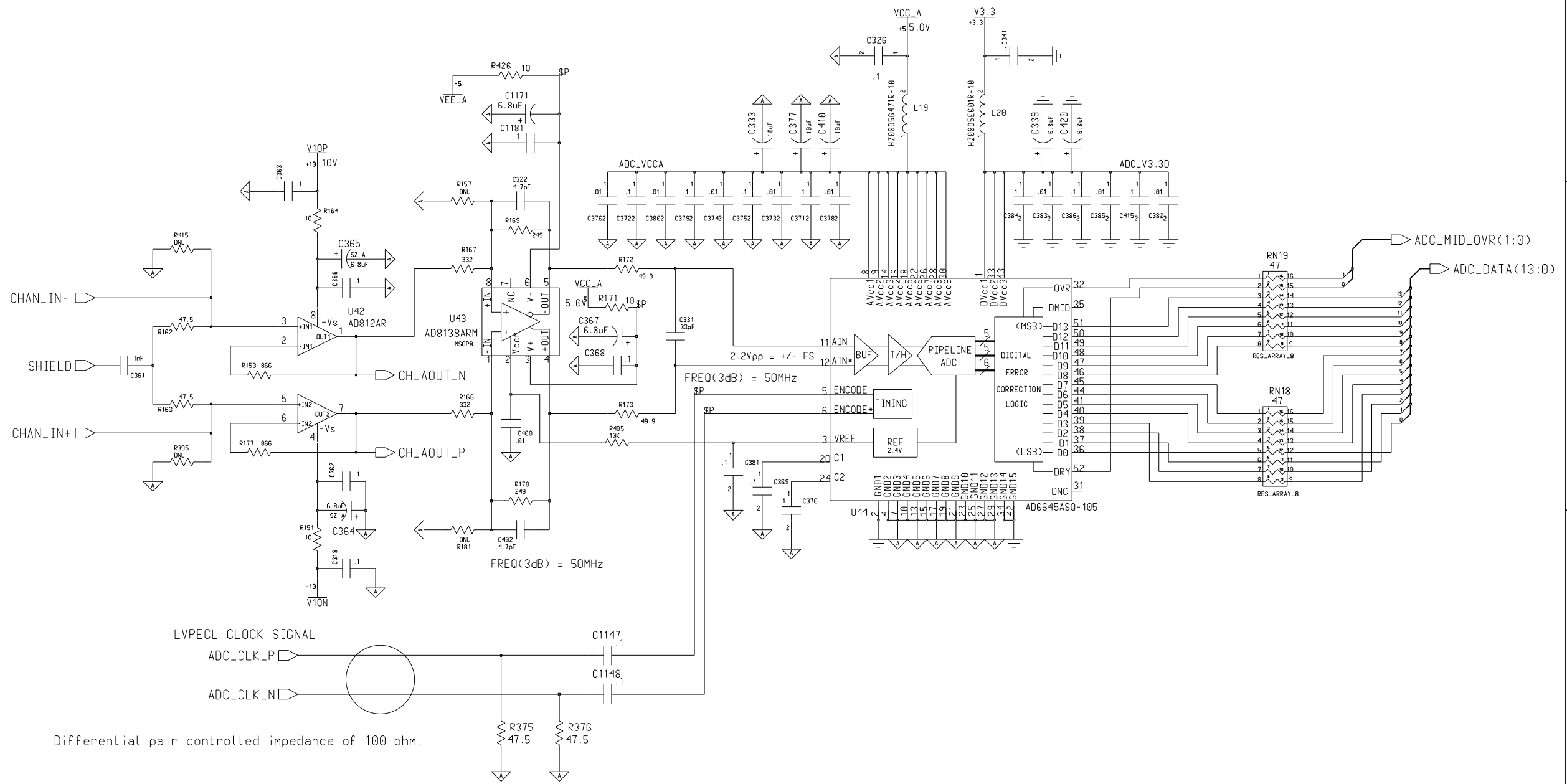
Differential pair controlled impedance of 100 ohm.



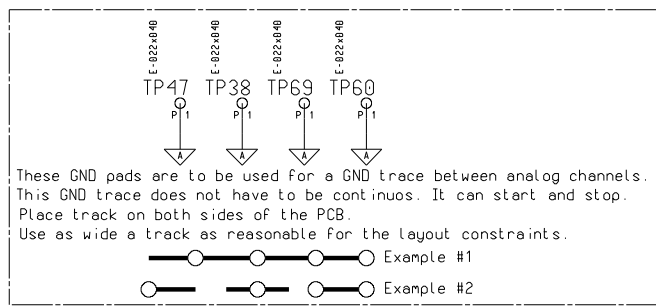
AD8138 GAIN	CHAN
0.25	0 (CC)
0.75	1-9 (SEG)

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: Harold Yaver			TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END
R&D CHK:	REV:		414 A
DOC CTRL CHK:	MFG ENGR CHK:		Page: 1

Changed by: jn_joseph	Date Changed: Wednesday, April 25, 2007	Time Changed: 12:14:38 pm	QA CHK:	Drawing Number:	Page: 1
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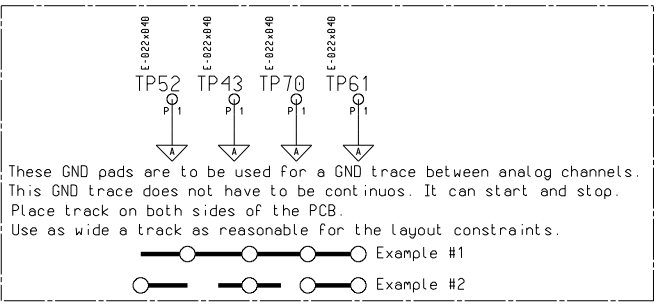
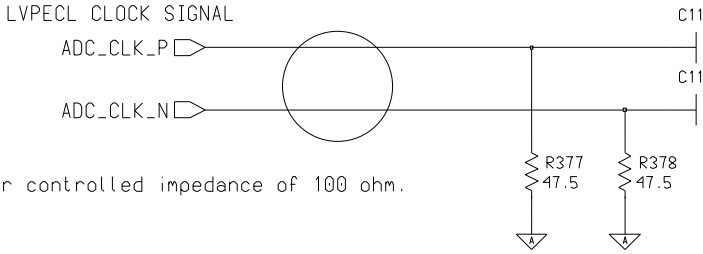
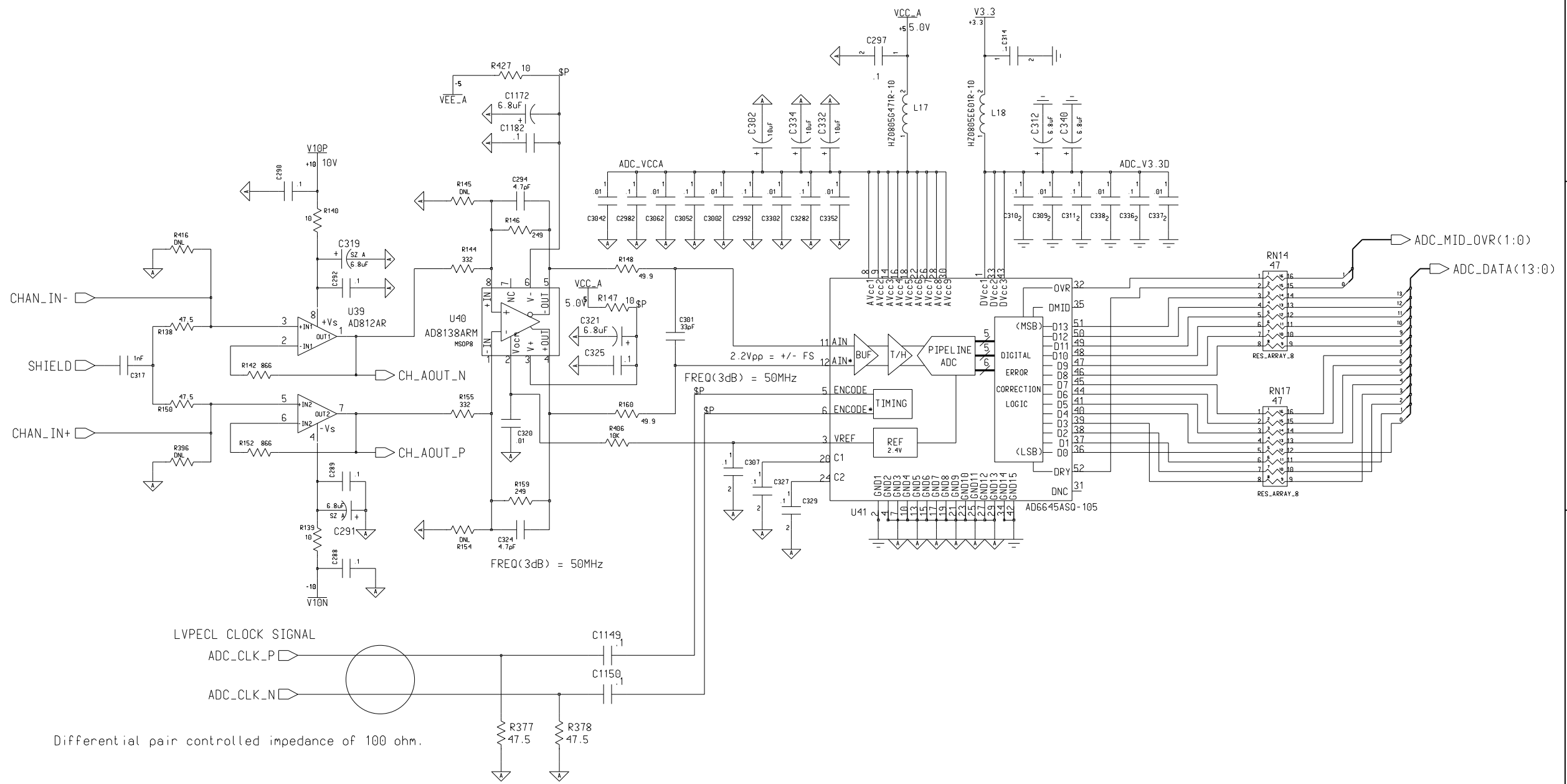
Differential pair controlled impedance of 100 ohm.



AD8138 GAIN	CHAN
0.25	0 (CC)
0.75	1-9 (SEG)

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: Harold Yaver			TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END
R&D CHK:	REV:		
DOC CTRL CHK:	Drawing Number:		
MFG ENGR CHK:	Page:		

Changed by: jn_joseph	Date Changed: Wednesday, April 25, 2007	Time Changed: 12:14:38 pm	QA CHK:	REV:	Page: 1
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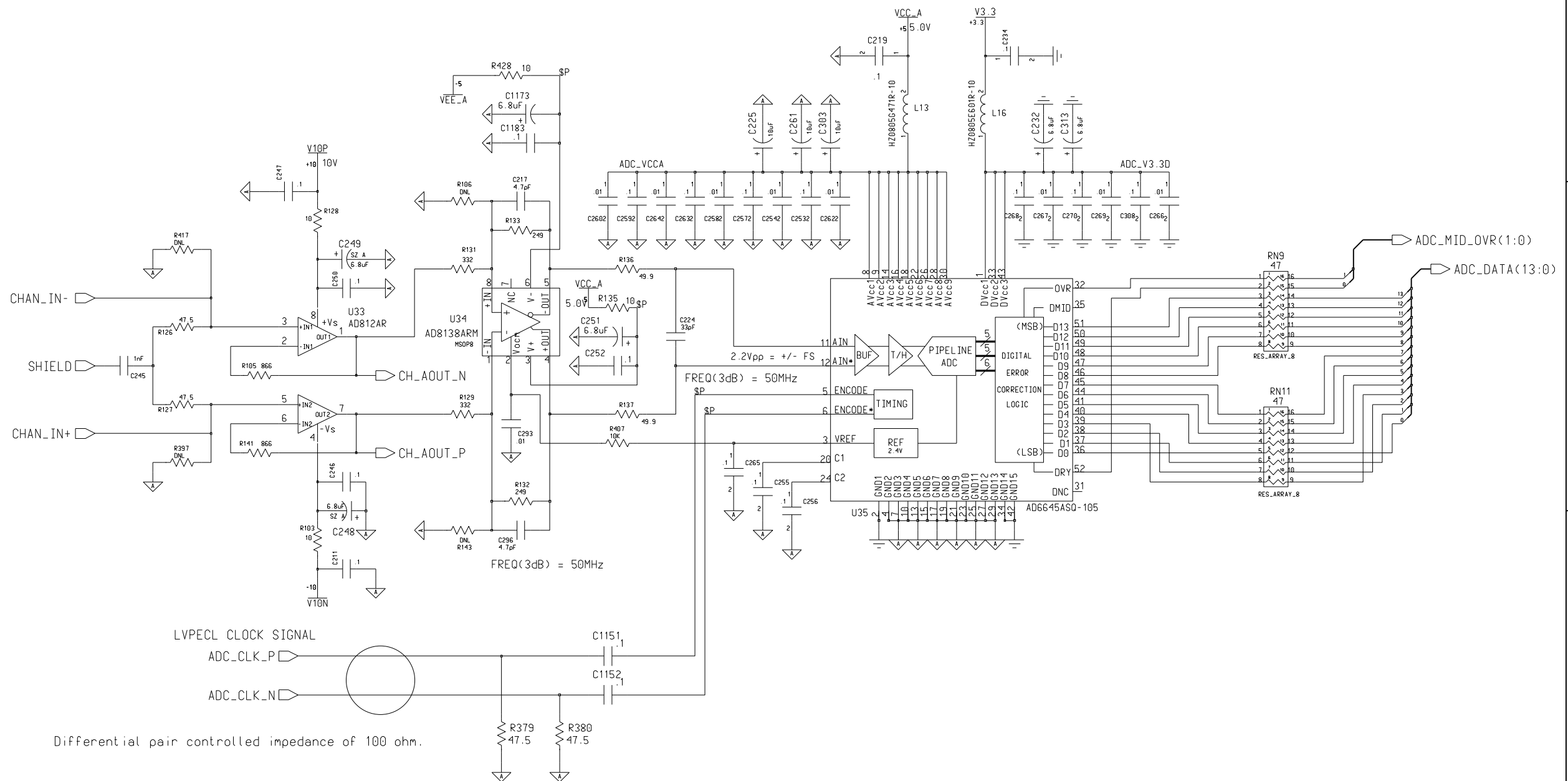


AD8138 GAIN	CHAN
0.25	0 (CC)
0.75	1-9 (SEG)

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: Harold Yaver			TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END
R&D CHK:	REV:		Page: 1
DOC CTRL CHK:	Drawing Number:		
MFG ENGR CHK:	QA CHK:		

Changed by: jn_joseph	Date Changed: Wednesday, April 25, 2007	Time Changed: 12:14:38 pm	REV:	Drawing Number:	Page: 1
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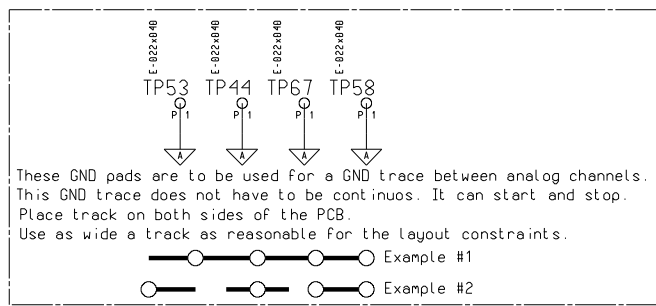




LVPECL CLOCK SIGNAL  
 ADC\_CLK\_P  
 ADC\_CLK\_N

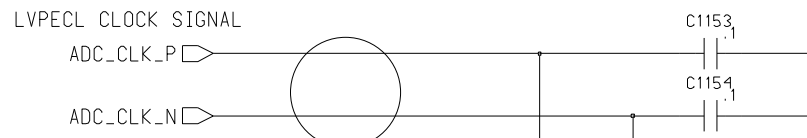
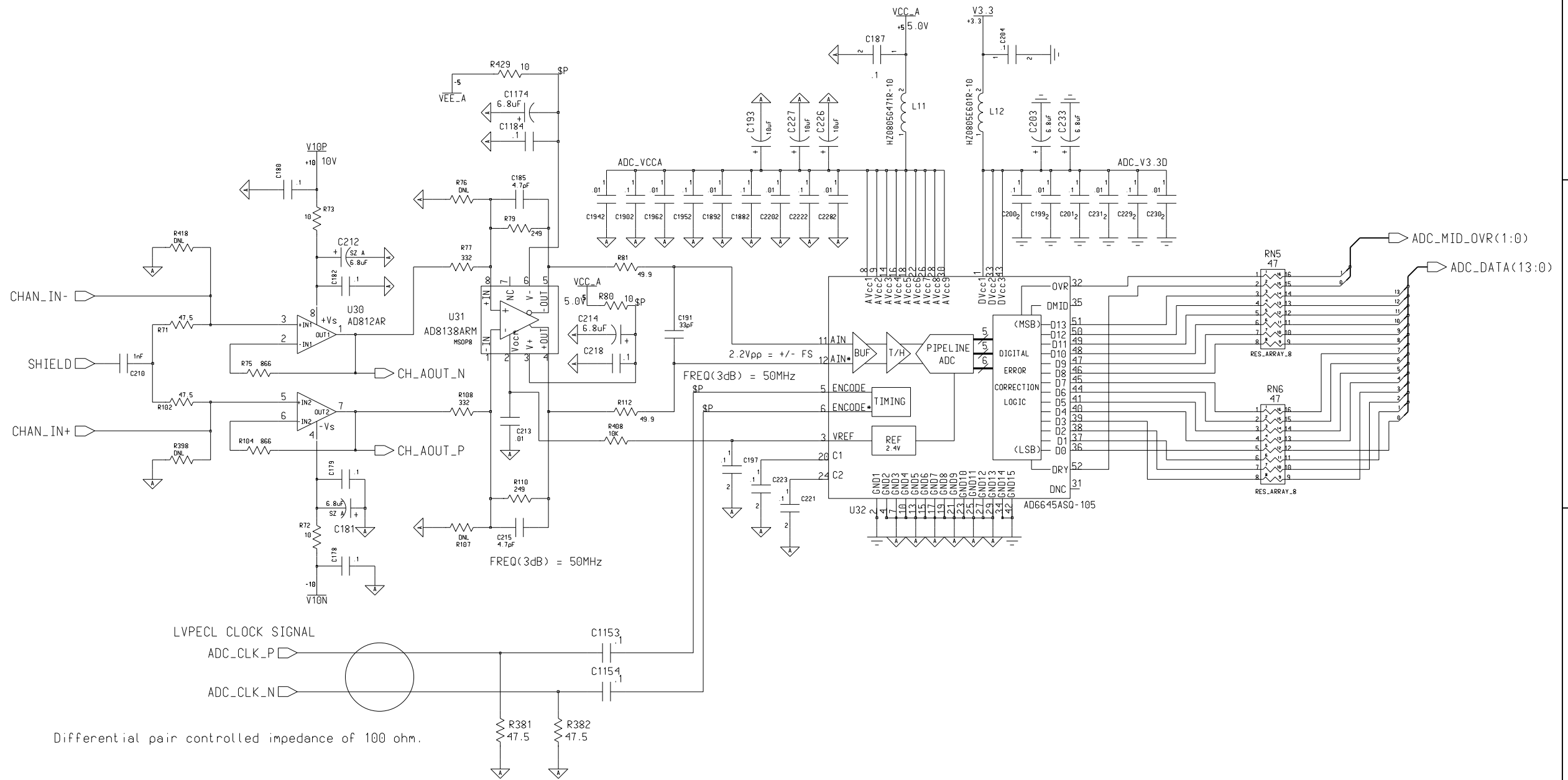
Differential pair controlled impedance of 100 ohm.

AD8138 GAIN	CHAN
0.25	0 (CC)
0.75	1-9 (SEG)

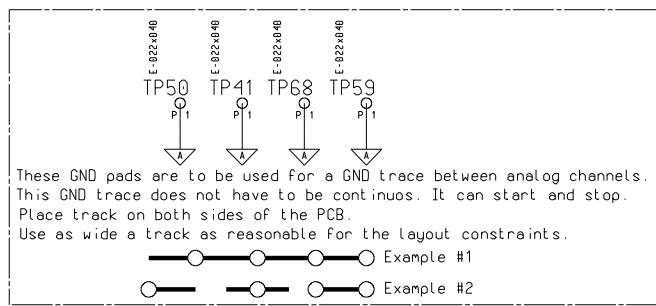


Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: Harold Yaver			TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END
R&D CHK:	REV:		414 A
DOC CTRL CHK:	MFG ENGR CHK:		Page: 1

Changed by: jn_joseph	Date Changed: Wednesday, April 25, 2007	Time Changed: 12:14:38 pm	QA CHK:	REV:	Drawing Number:	Page: 1
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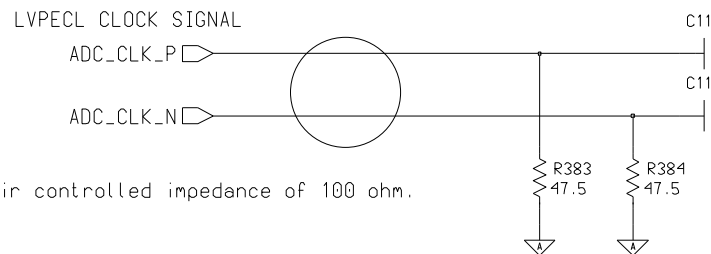
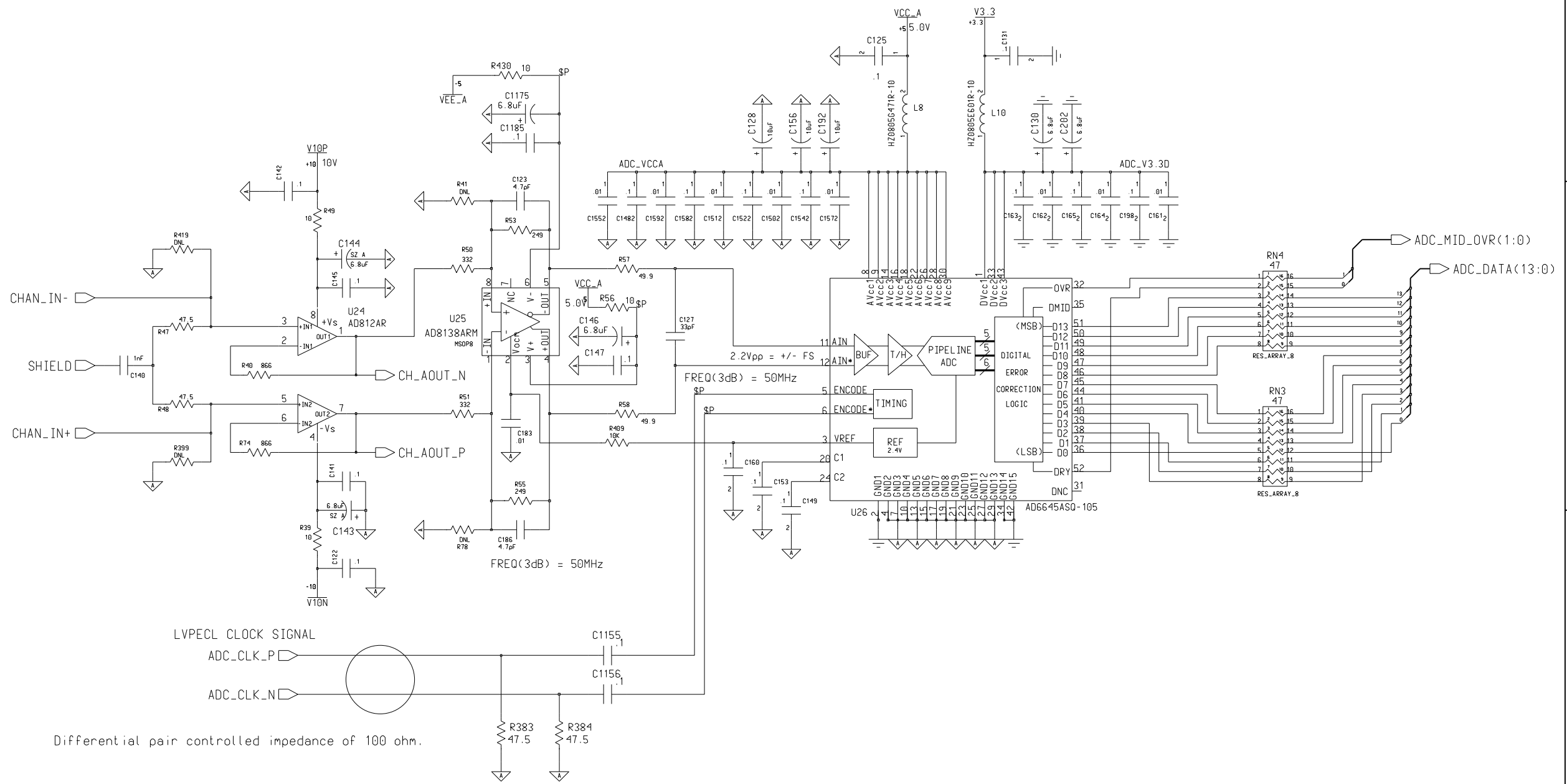
Differential pair controlled impedance of 100 ohm.



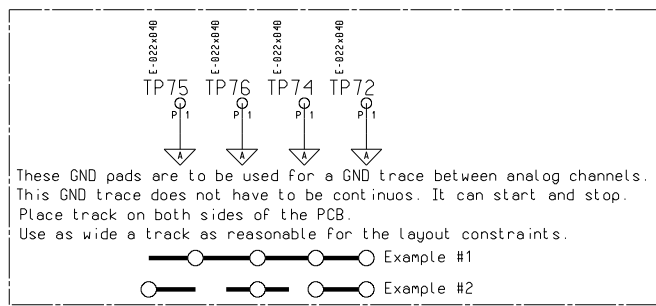
AD8138 GAIN	CHAN
0.25	0 (CC)
0.75	1-9 (SEG)

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: Harold Yaver			
R&D CHK:	TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END	4 1 4 A	
DOC CTRL CHK:			
MFG ENGR CHK:			

Changed by: jn_joseph	Date Changed: Wednesday, April 25, 2007	Time Changed: 12:14:38 pm	QA CHK:	REV:	Drawing Number:	Page: 1
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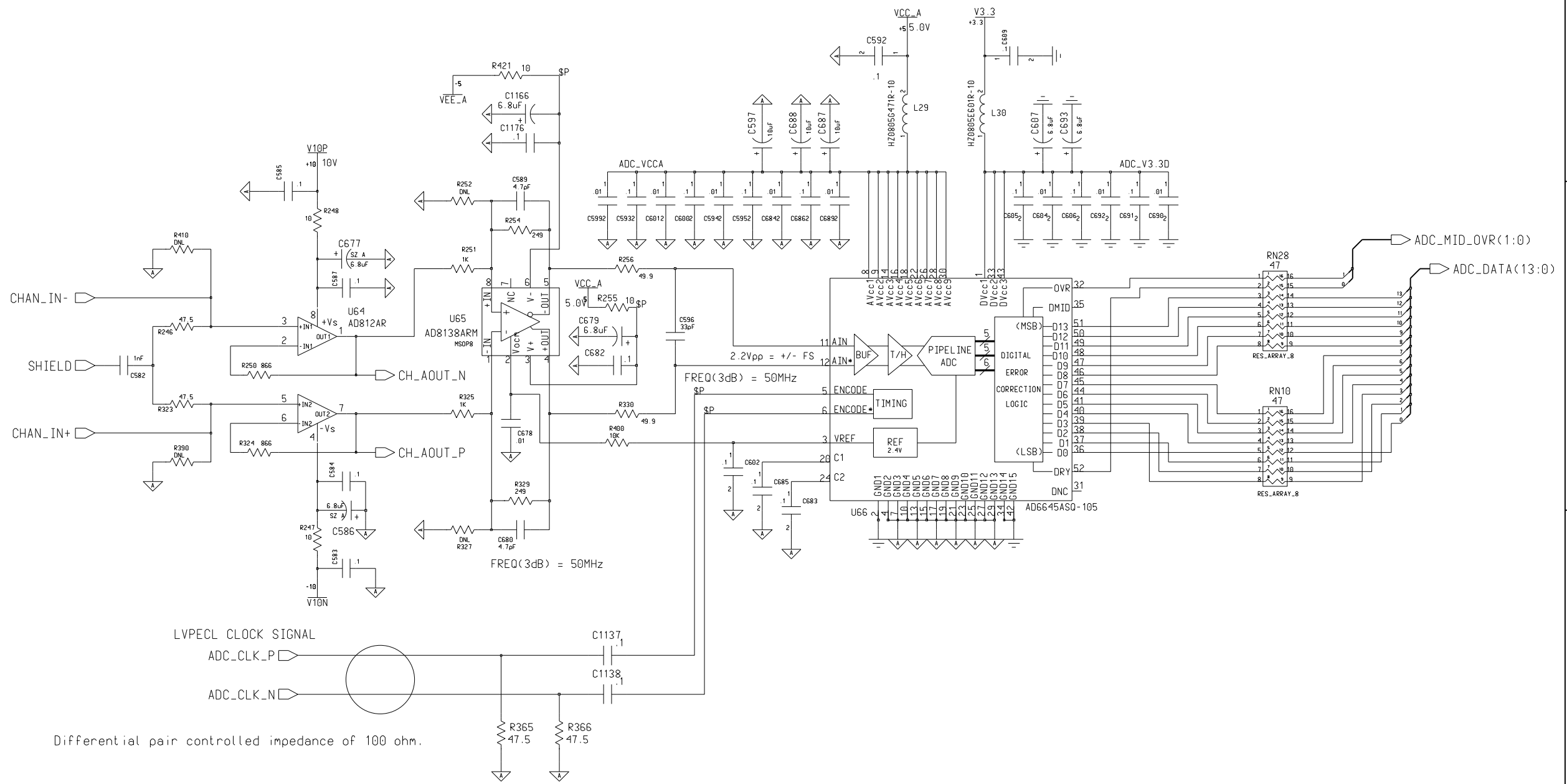
Differential pair controlled impedance of 100 ohm.



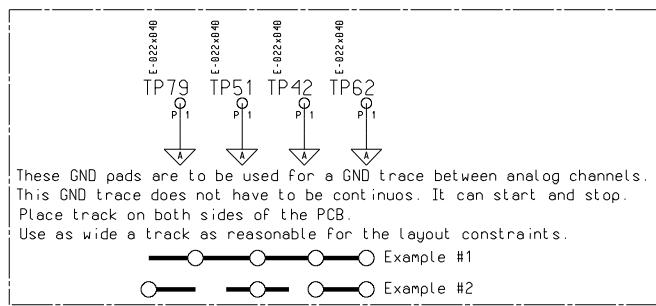
AD8138 GAIN	CHAN
0.25	0 (CC)
0.75	1-9 (SEG)

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: Harold Yaver			TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END
R&D CHK:	REV:		
DOC CTRL CHK:	Drawing Number:		
MFG ENGR CHK:	Page:		

Changed by: jn_joseph	Date Changed: Wednesday, April 25, 2007	Time Changed: 12:14:38 pm	QA CHK:	REV:	Page: 1
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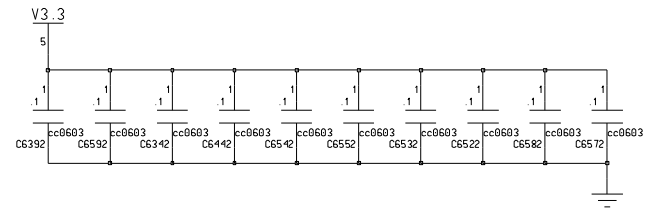
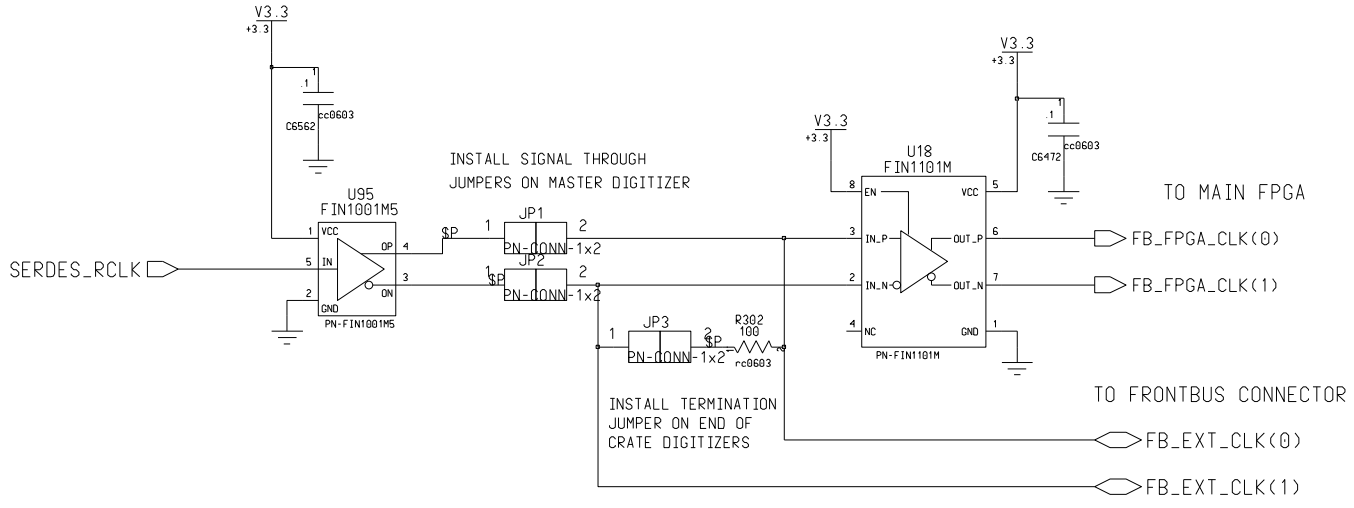
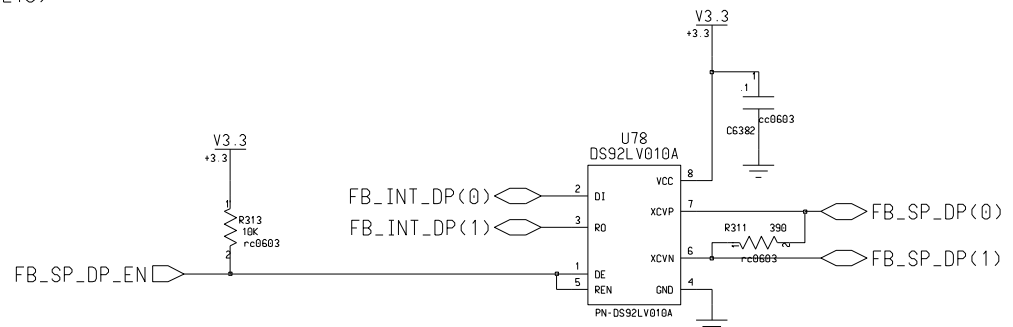
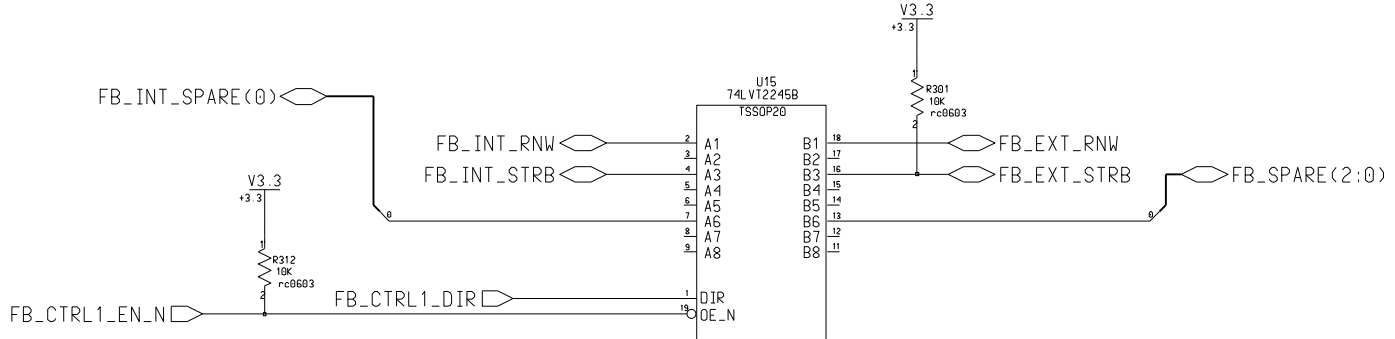
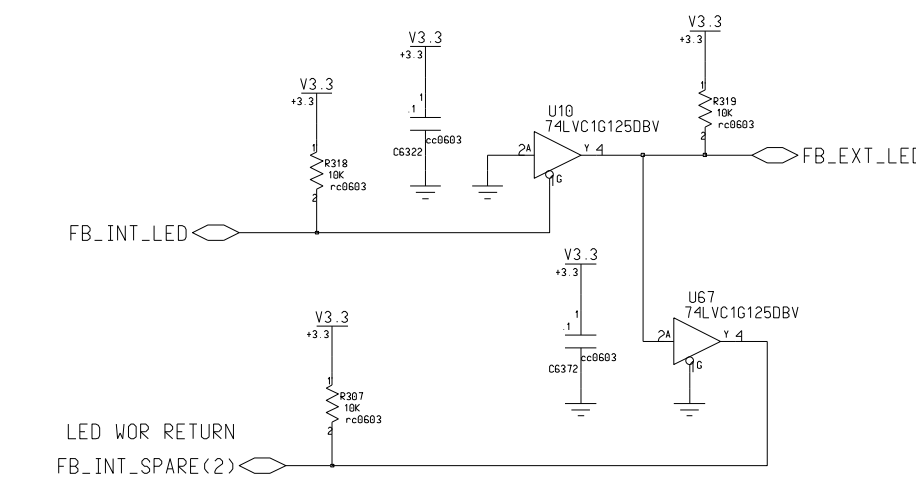
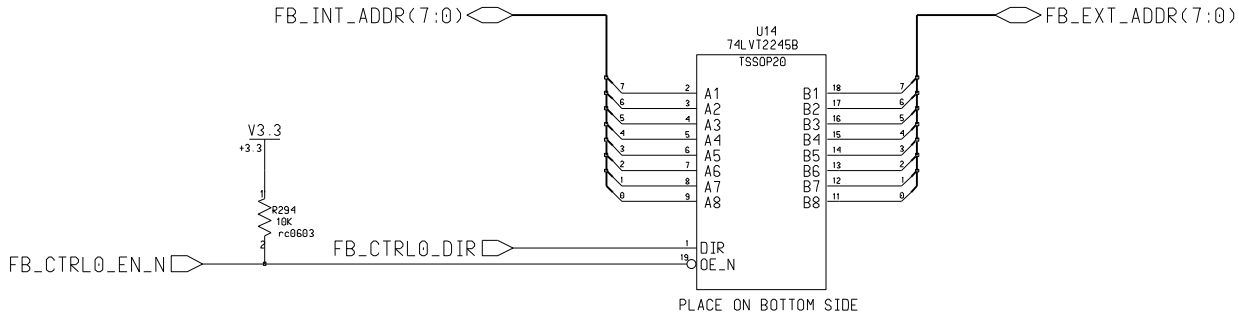
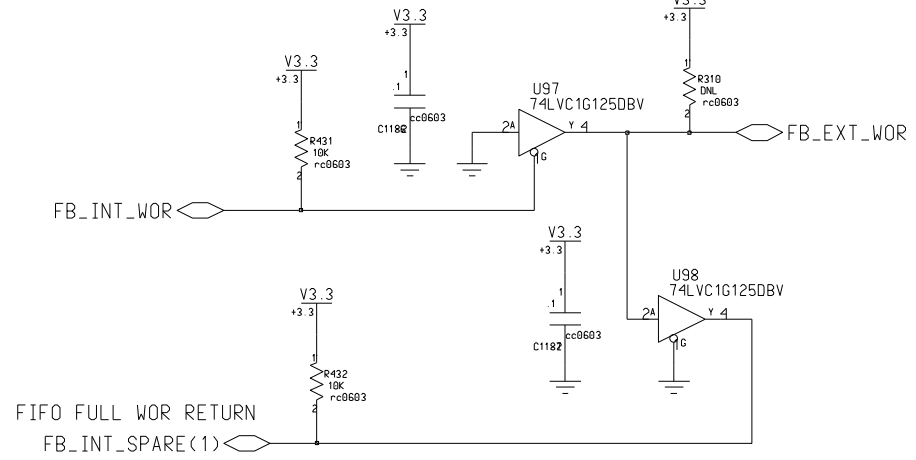
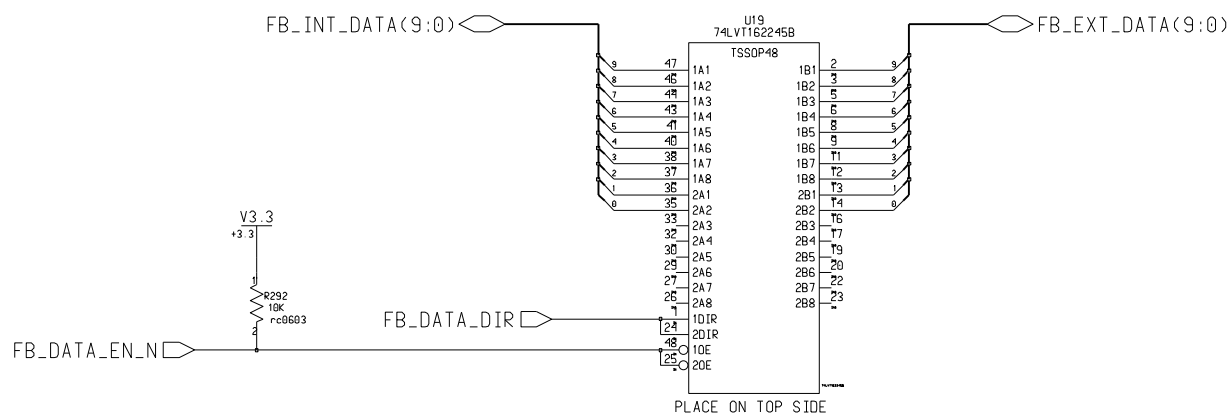
Differential pair controlled impedance of 100 ohm.



AD8138 GAIN	CHAN
0.25	0 (CC)
0.75	1-9 (SEG)

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: Harold Yaver			TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END
R&D CHK:	REV:		414 A
DOC CTRL CHK:	MFG ENGR CHK:		Page: 1

Changed by: jn_joseph	Date Changed: Wednesday, April 25, 2007	Time Changed: 12:14:38 pm	QA CHK:	REV:	Drawing Number:	Page: 1
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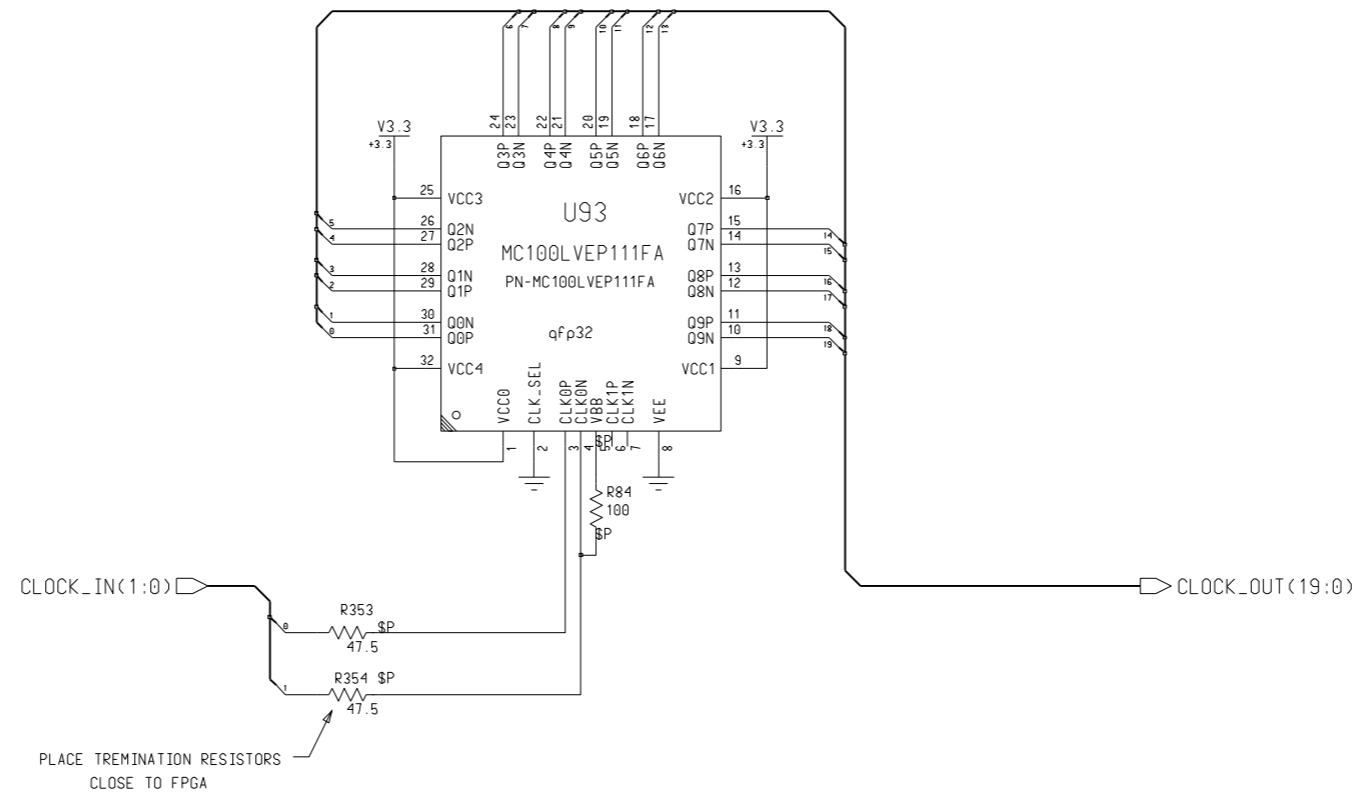
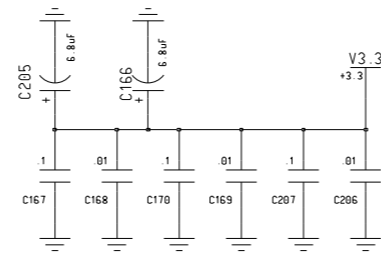


NOT USED

FB\_CLKOUT\_EN

Engineer:	LBNL	
jmjoseph	1 CYCLOTRON RD.	
Drawn by:	BERKELEY, CA 94720	
jmjoseph	TITLE:	Size:
R&D CHK:	SCHEMATIC DIAGRAM:	c
DOC CTRL CHK:	GRETINA - FRONTBUS BUFFERS	4 1 4 A
MFG ENGR CHK:	REV:	Page:
QA CHK:	Drawing Number:	1

Changed by:	Date Changed:	Time Changed:	QA CHK:	REV:	Drawing Number:	Page:
jmjoseph	Monday, March 26, 2007	4:57:47 pm				1



Engineer: jmjoseph	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: jmjoseph			TITLE: SCHEMATIC DIAGRAM, GRETINA - CLOCK FAN OUT
R&D CHK:	REV: A	Drawing Number:	
DOC CTRL CHK:	QA CHK:		
MFG ENGR CHK:			

Changed by: jmjoseph	Date Changed: Monday, March 26, 2007	Time Changed: 5:01:42 pm	REV: A	Drawing Number:	Page: 1
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A

A

B

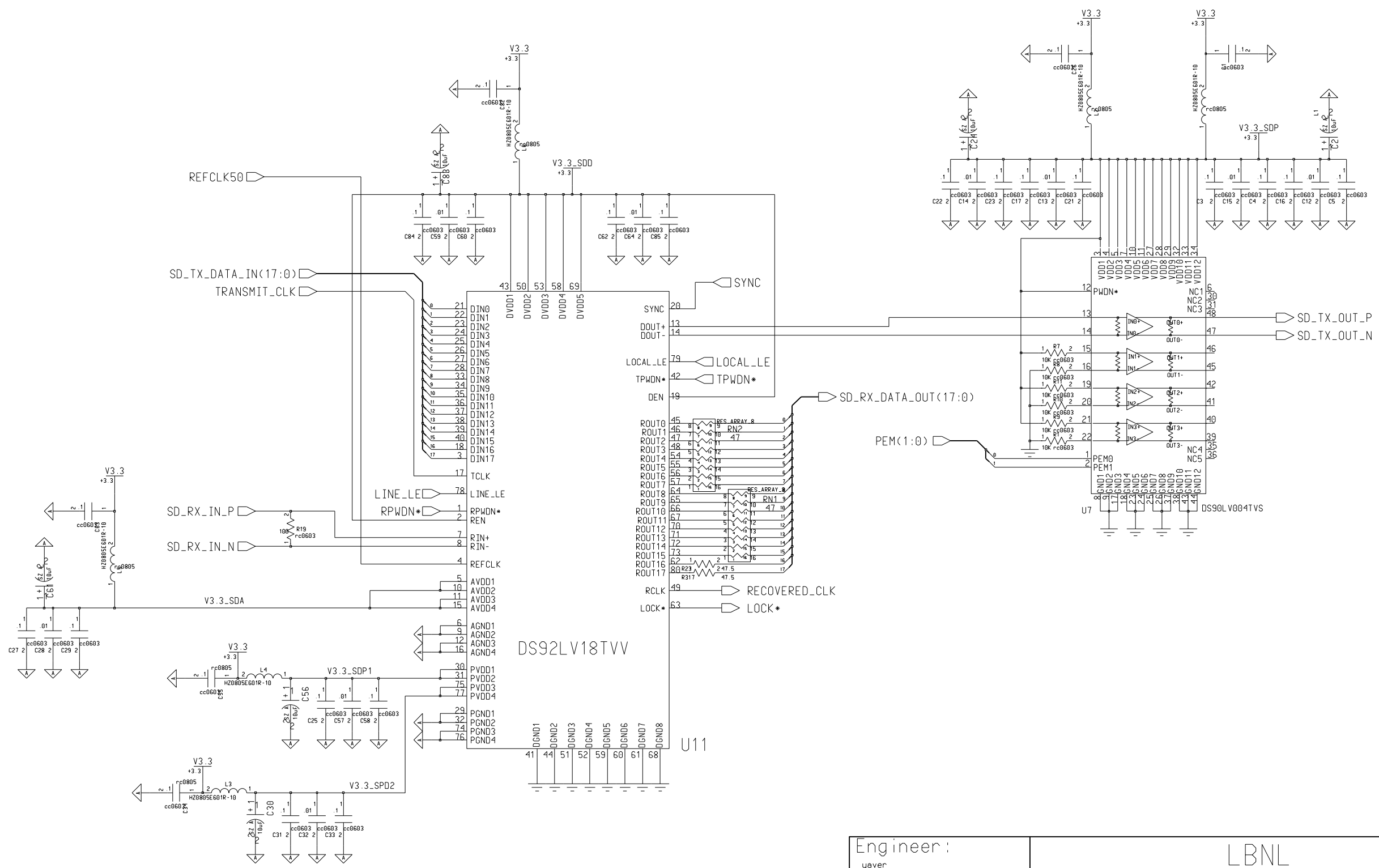
B

C

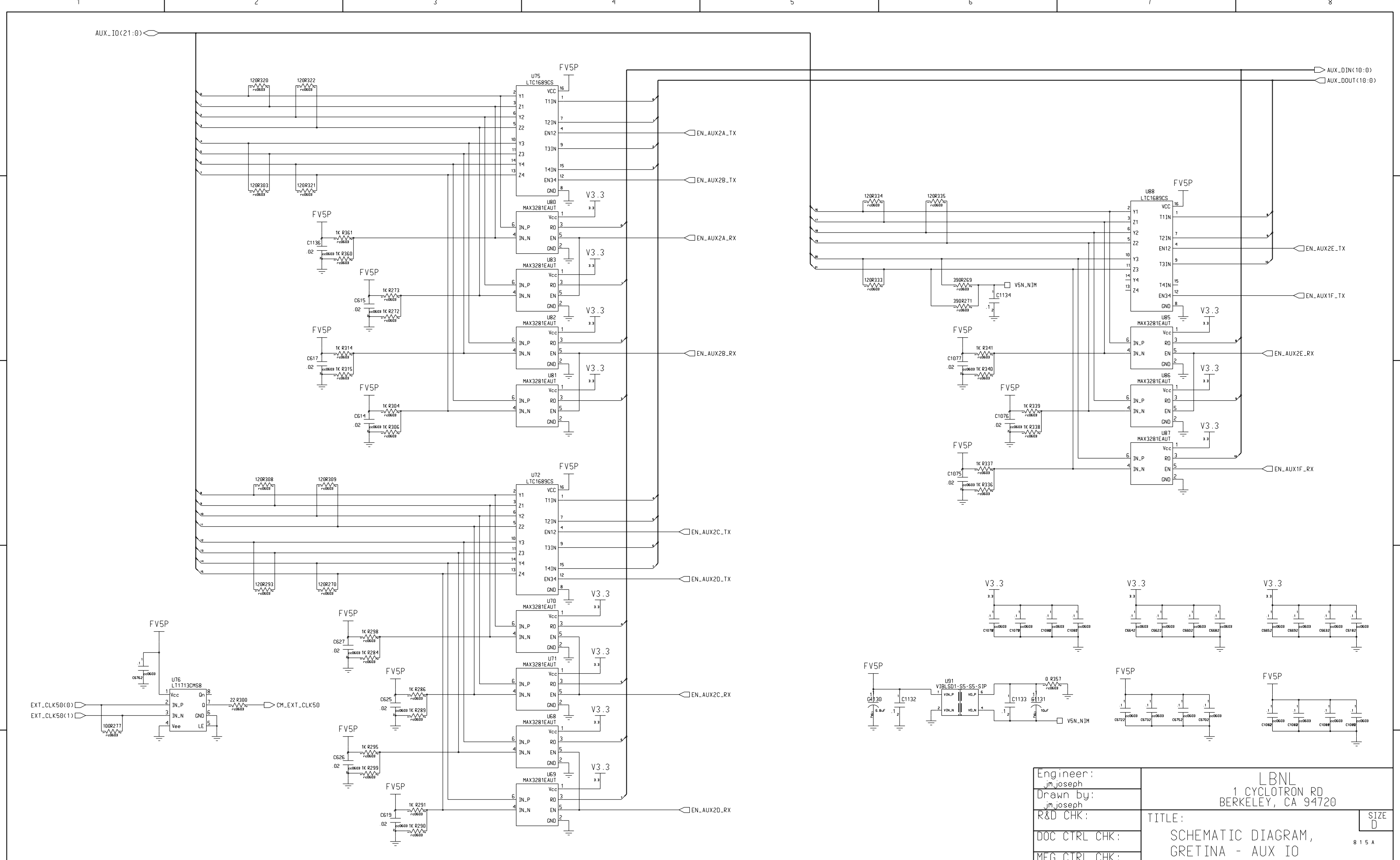
C

D

D



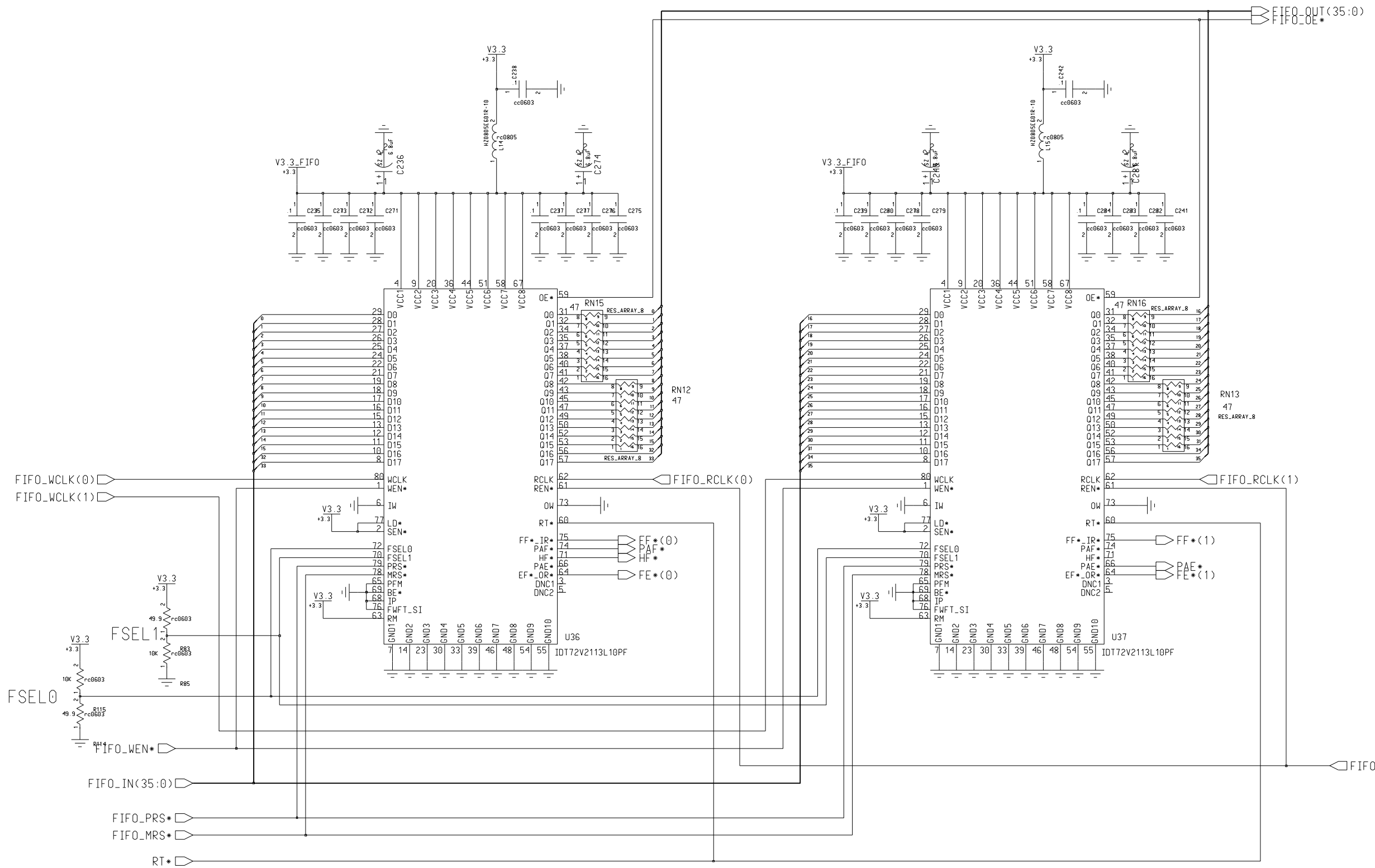
Engineer: yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: yaver			TITLE: SCHEMATIC DIAGRAM, GRETINA - SERIALIZER DESERIALIZER
R&D CHK:	REV:	Drawing Number:	Page: 1
DOC CTRL CHK:	Time Changed: 5:02:35 pm	QA CHK:	414A
MFG ENGR CHK:	Changed by: jm_joseph	Date Changed: Monday, March 26, 2007	



Engineer: jm_joseph	LBNL 1 CYCLOTRON RD BERKELEY, CA 94720  TITLE: SCHEMATIC DIAGRAM, GRETINA - AUX IO	SIZE D	
Drawn by: jm_joseph		815 A	
R&D CHK:			
DOC CTRL CHK:			
MFG CTRL CHK:			
QA CHK:	REV	Drawing Number:	Page: 1

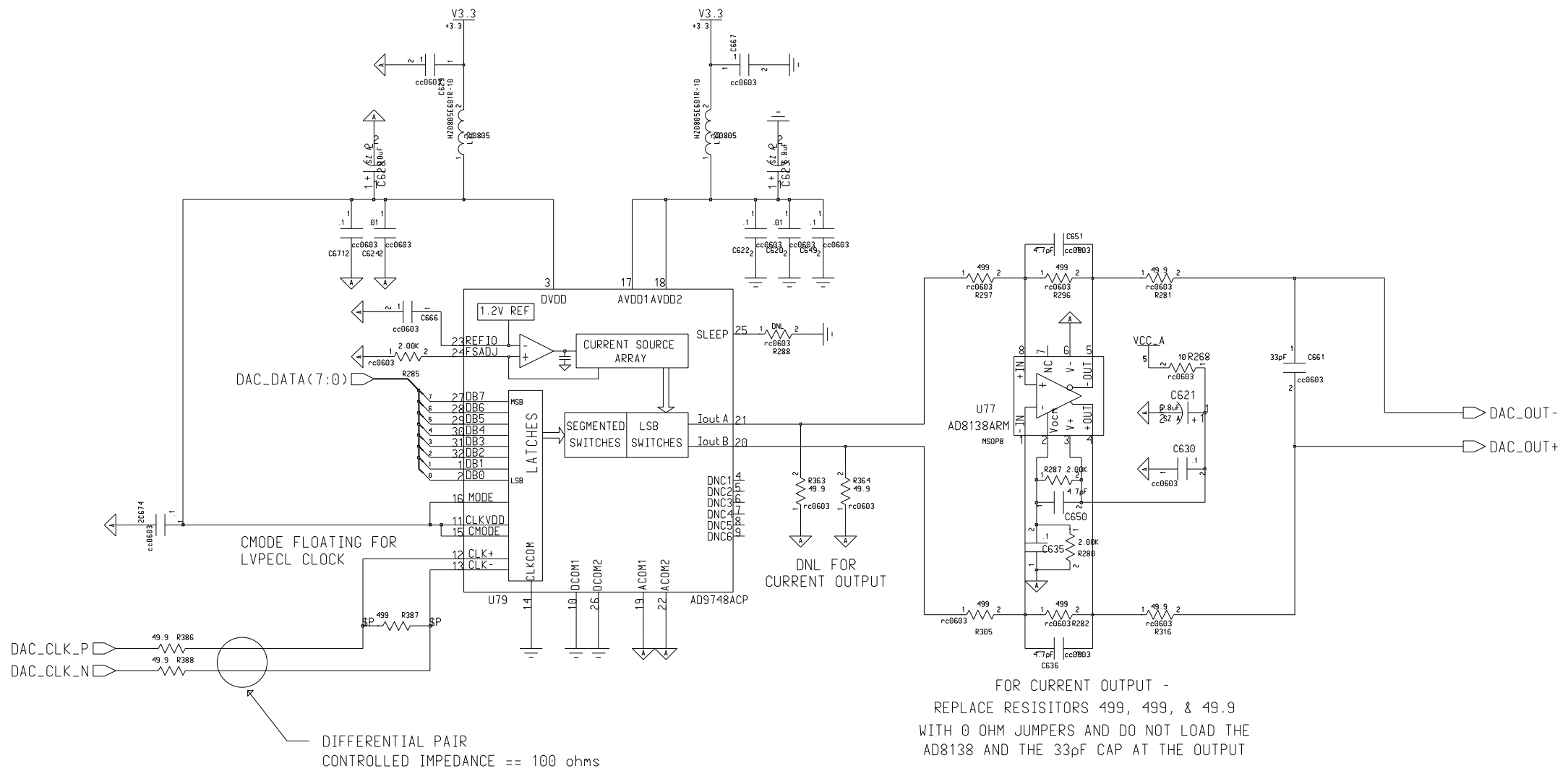
Changed by: jm_joseph	Date Changed: Monday, March 26, 2007	Time: 5:01:56 pm
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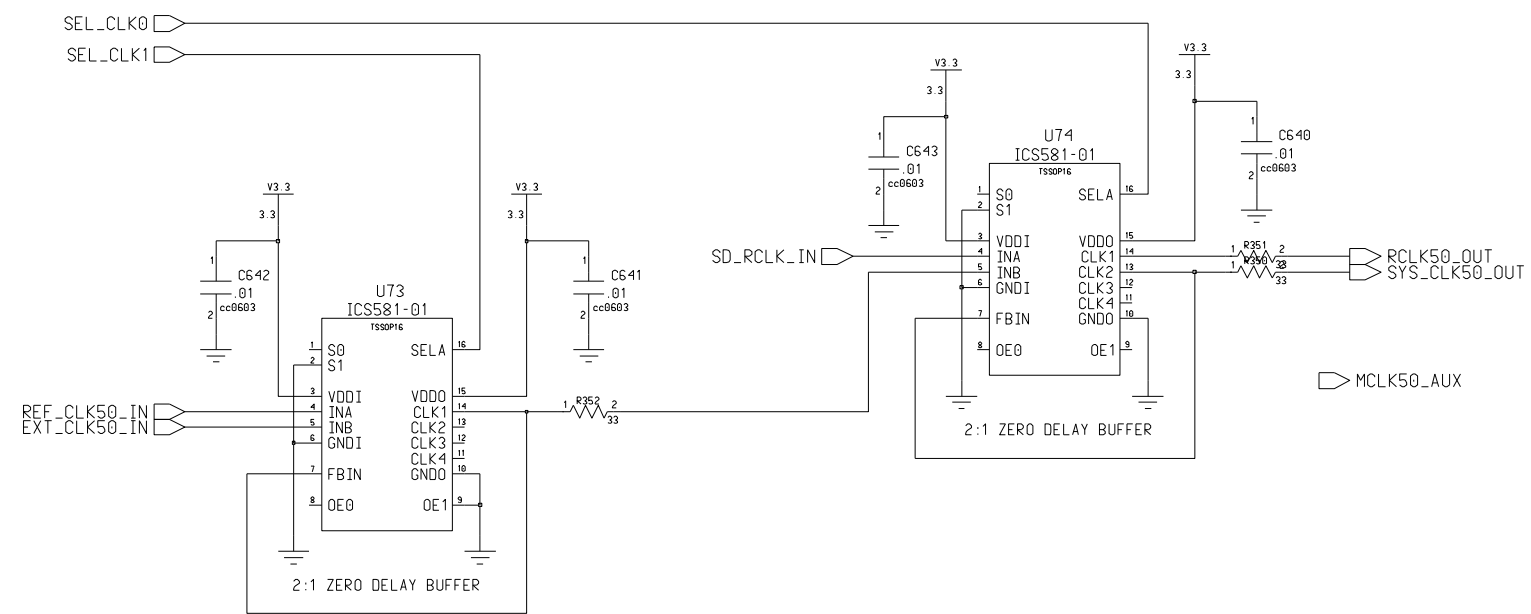
Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: Harold Yaver			
R&D CHK:	TITLE: SCHEMATIC DIAGRAM, GRETINA - READOUT FIFO	414A	
DOC CTRL CHK:	REV:	Drawing Number:	Page: 1
MFG ENGR CHK:	Time Changed: 5:02:16 pm	QA CHK:	

Changed by: jn_joseph	Date Changed: Monday, March 26, 2007
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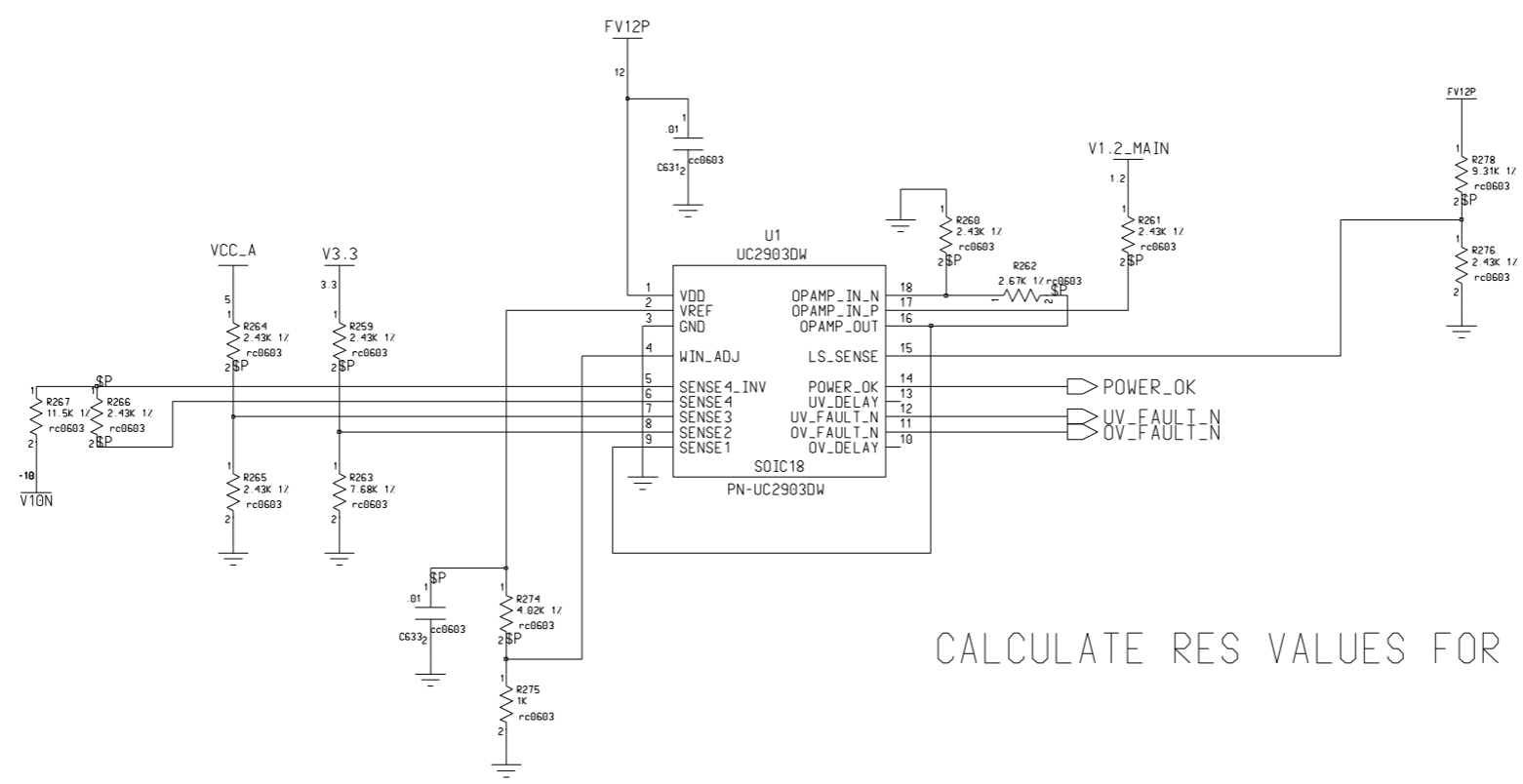
Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: Harold Yaver			TITLE: SCHEMATIC DIAGRAM, GRETINA - DAC OUTPUT
R&D CHK:	REV:	Drawing Number:	
DOC CTRL CHK:	QA CHK:		
MFG ENGR CHK:	Time Changed: 5:03:22 pm	REV:	414A

Changed by: jm_joseph	Date Changed: Monday, March 26, 2007	Time Changed: 5:03:22 pm
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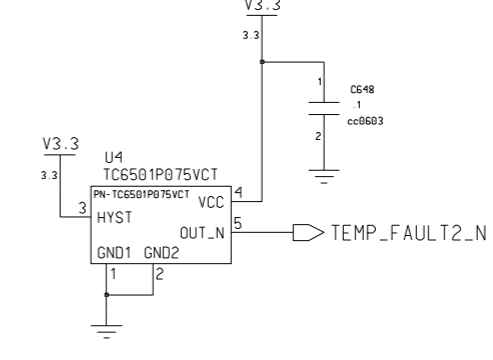
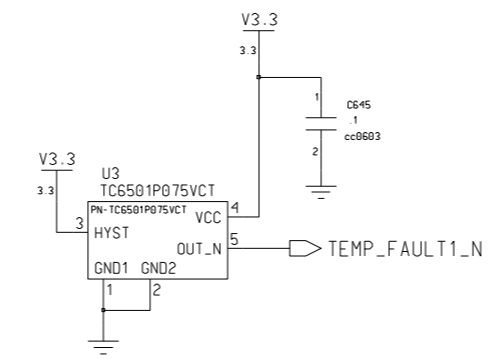
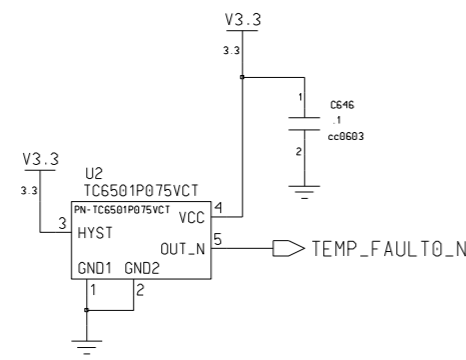


Engineer: jmjoseph	LBNL 1 CYCLOTRON RD BERKELEY, CA 94707	Size: c
Drawn by: jmjoseph		
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MFG ENGR CHK:	50MHZ CLOCK MUX	

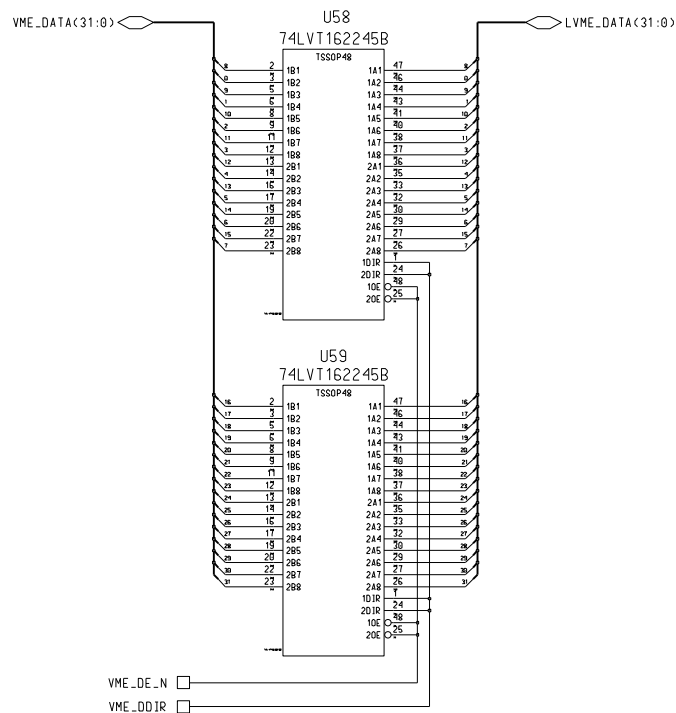
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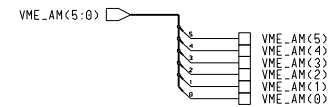
CALCULATE RES VALUES FOR VOLTAGE MONITORING



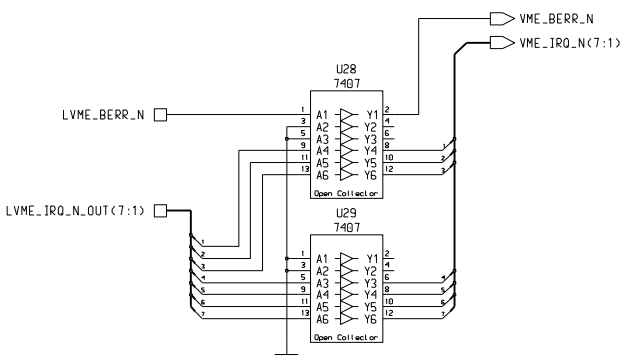
Engineer : jm_joseph	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		SIZE C
Drawn by: jm_joseph			
R&D CHK:	TITLE:	414A SCHEMATIC DIAGRAM, GRETINA - VOLTAGE & TEMP MONITOR	
DOC CTRL CHK:			
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Time Changed: 5:03:08 pm	QA CHK:	REV: A	Page: 1
Changed by: jm_joseph	Date Changed: Monday, March 26, 2007	Drawing Number:	



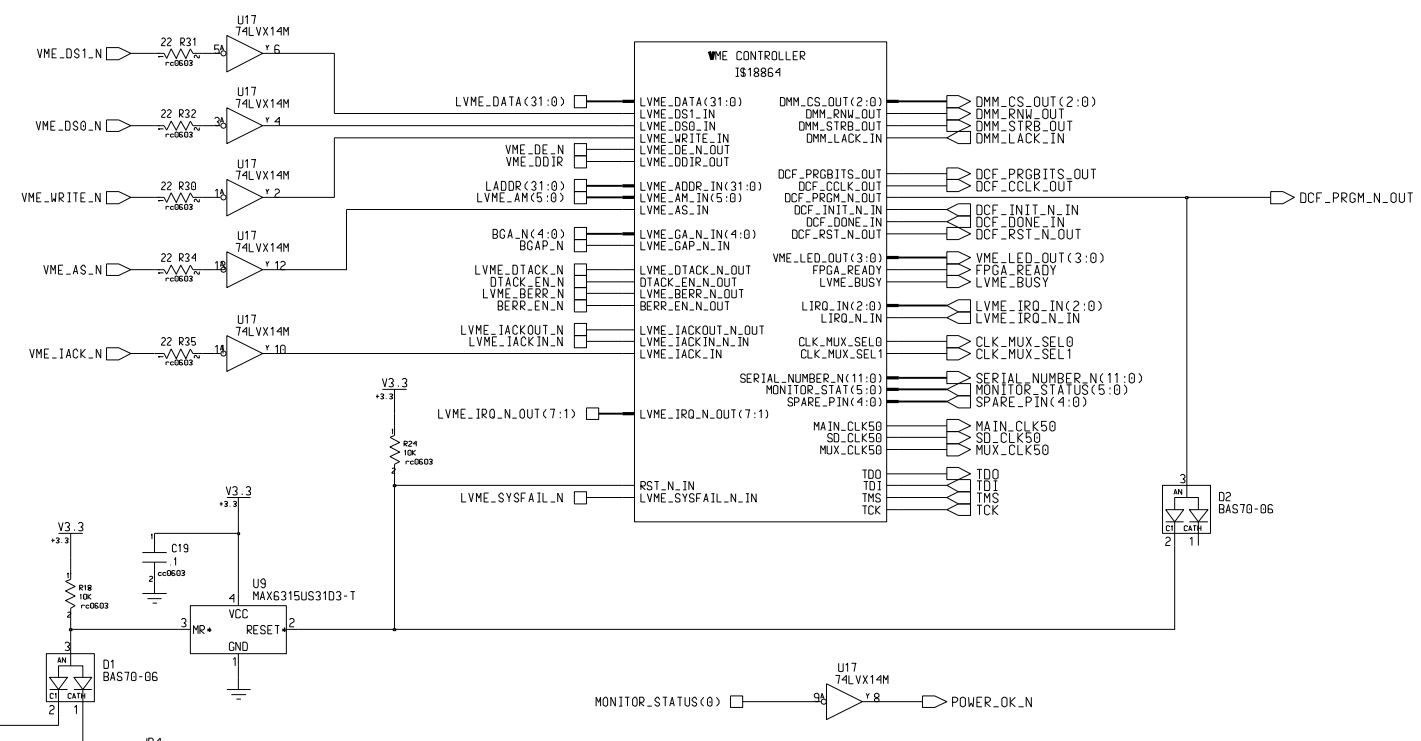
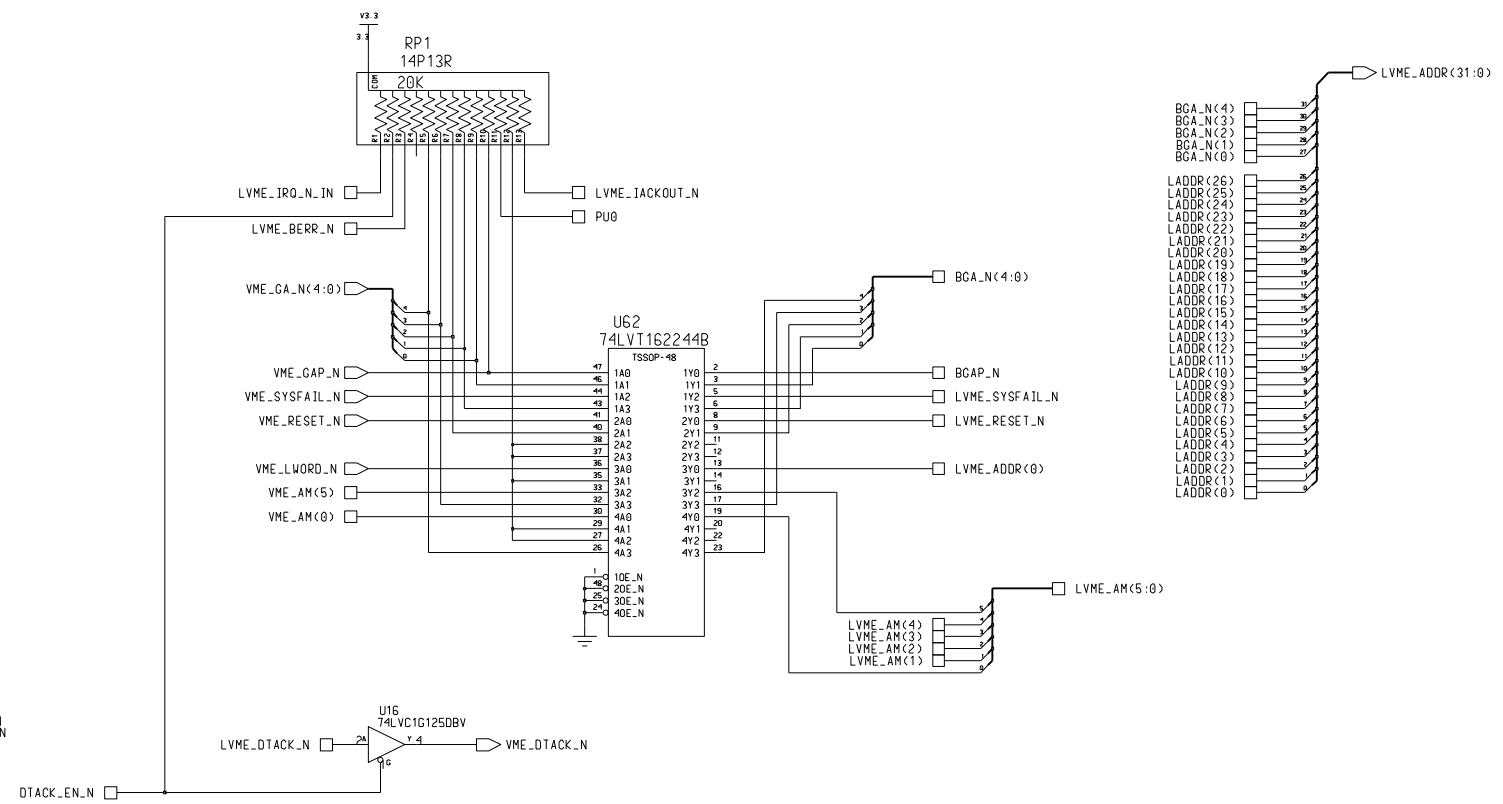
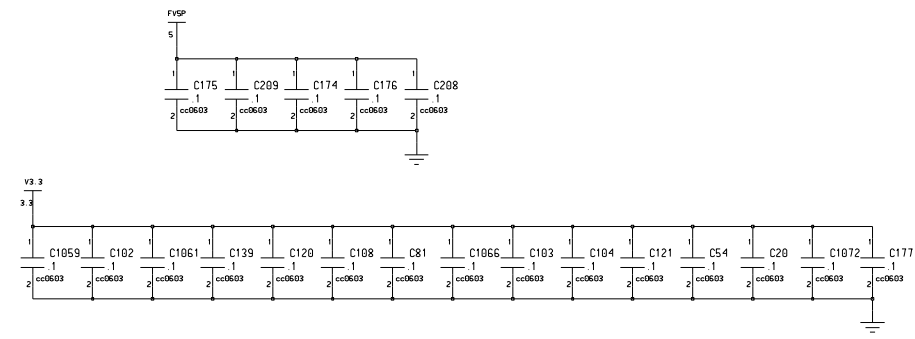
DATA TRANSCEIVERS



ADDR TRANSLATORS

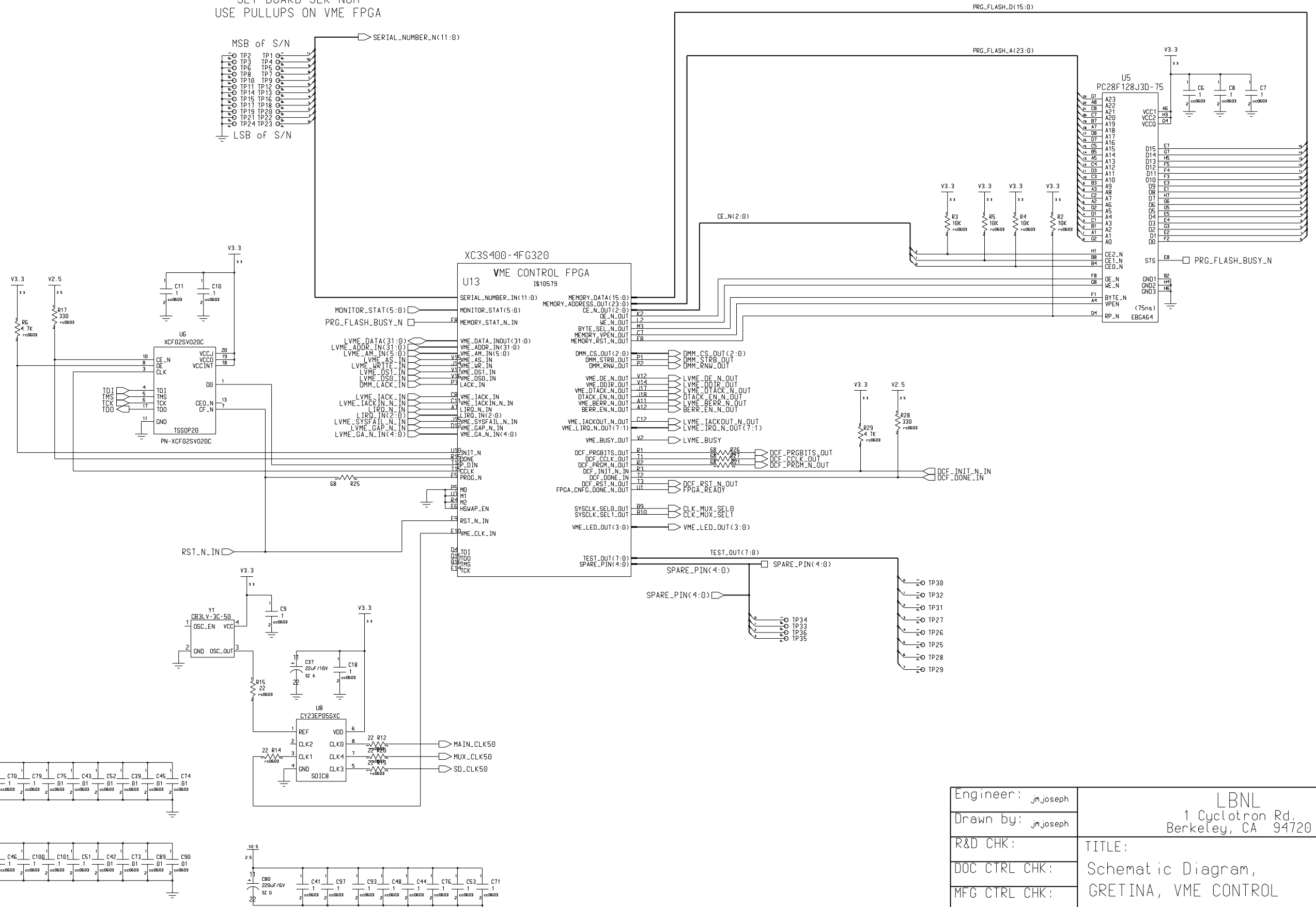
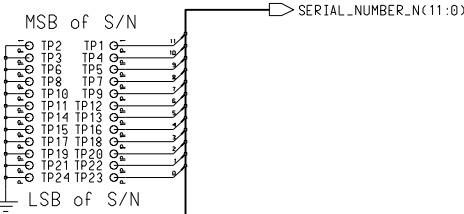


INTERRUPT GEN



Engineer:	JMJOSEPH	<p align="center">LBNL 1 CYCLOTRON ROAD BERKELEY, CA 94720</p>	<p align="right">Size: D 4 1 4 A</p>
Drawn by:	JMJOSEPH		
R&D CHK:		TITLE:	Schematic Diagram,
DOC CTRL CHK:			VME Interface
MFG ENGR CHK:			

SET BOARD SER NUM  
USE PULLUPS ON VME FPGA



Engineer:	jm_joseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720	Size: D
Drawn by:	jm_joseph		
R&D CHK:		TITLE:	Schematic Diagram, GRETINA, VME CONTROL
DOC CTRL CHK:		REV	F
MFG CTRL CHK:		Drawing Number:	
QA CHK:		Page:	xx

Changed by: jm\_joseph  
Date Changed: Monday, March 26, 2007  
Time: 5:03:46 pm

815 A