

VEE_A

ADD 2.5V REGULATOR

VME FPGA CORE SUPPLY

MAIN FPGA CORE SUPPLY

PN-02-01-160-2101

HARTING-02-01-160-2101

MPR
MCLK
MSD
MRD
MCTL
RESP_N

VME CONNECTORS

PN-02-01-160-2101

HARTING-02-01-160-2101

Engineer:

Drawn by:

R&D CHK:

DOC CTRL CHK:

MFG ENGR CHK:

QA CHK:

REV: A

LBNL
1 CYCLOTRON RD
BERKELEY, CA 94720

TITLE:
SCHEMATIC DIAGRAM,
GRETINA - TOP

Drawing Number:

Page:

Changed by:

Date Changed:

Time Changed:

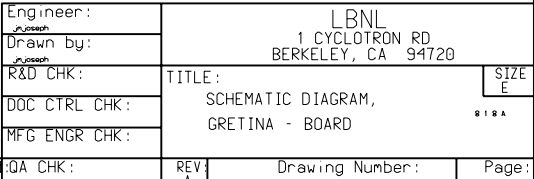
SIZE
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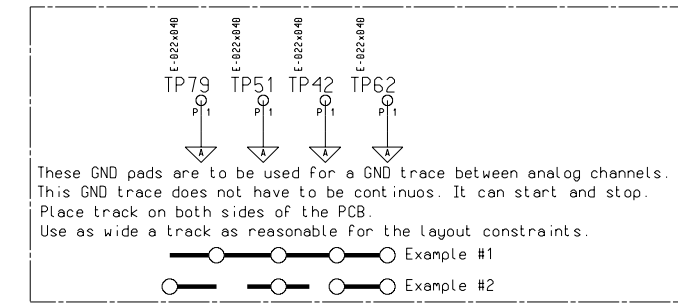
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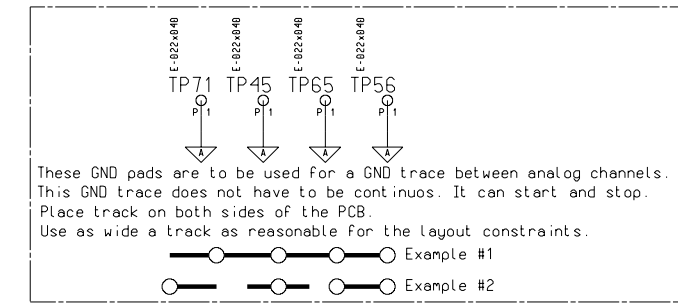
ADC_CLK_P

ADC_CLK_N

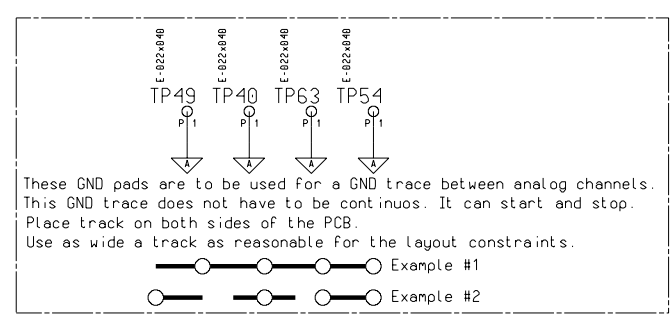
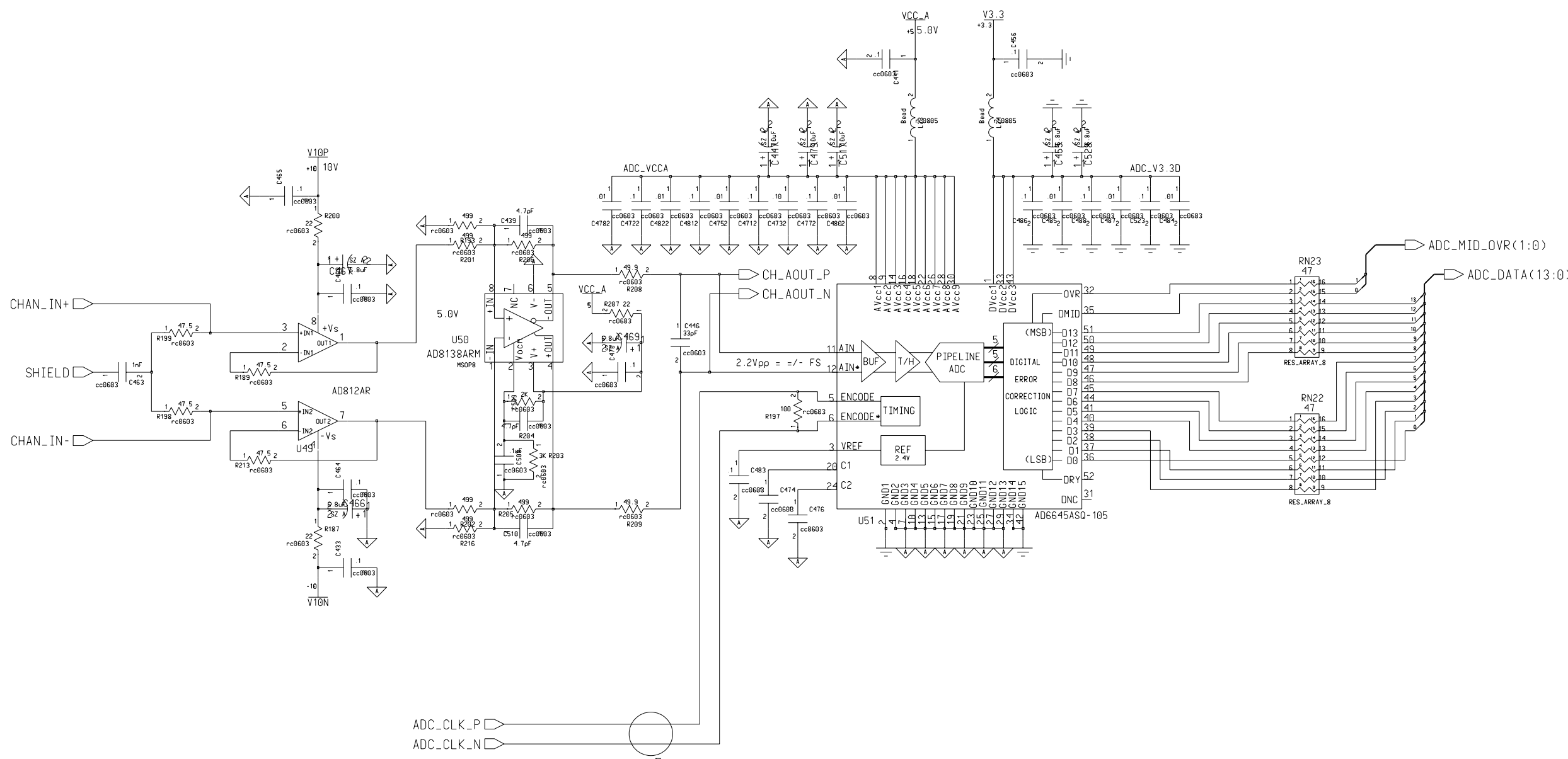
Differential pair controlled impedance of 100 ohm.

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		
Drawn by: Harold Yaver			
R&D CHK:	TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END		SIZE C
DOC CTRL CHK:			4 1 4 A
MFG ENGR CHK:			

Changed by: yaver	Date Changed: Friday, March 15, 2002	Time Changed: 5:56:48 pm	QA CHK:	REV:	Drawing Number:	Page: 1
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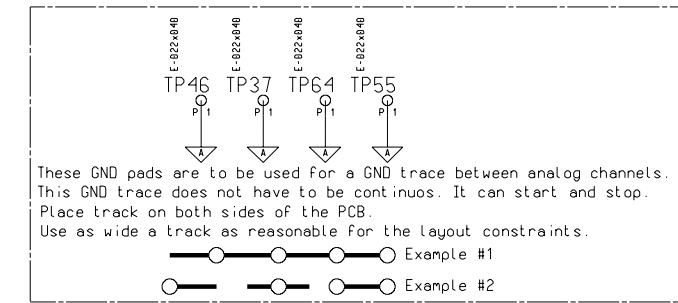
Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		
Drawn by: Harold Yaver			
R&D CHK:	TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END	SIZE C	4 1 4 A
DOC CTRL CHK:			
MFG ENGR CHK:			
Changed by: yaver	Date Changed: Friday, March 15, 2002	Time Changed: 5:56:48 pm	QA CHK:
REV:	Drawing Number:	Page: 1	



Differential pair controlled impedance of 100 ohm.

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		
Drawn by: Harold Yaver			
R&D CHK:	TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END	SIZE C	4 1 4 A
DOC CTRL CHK:			
MFG ENGR CHK:			
QA CHK:	REV:	Drawing Number:	Page: 1

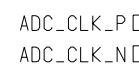
Changed by: yaver	Date Changed: Friday, March 15, 2002	Time Changed: 5:56:48 pm
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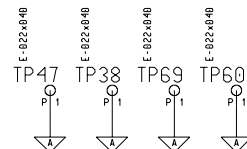
ADC_CLK_P
ADC_CLK_N

Differential pair controlled impedance of 100 ohm.

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		
Drawn by: Harold Yaver			
R&D CHK:	TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END		SIZE C
DOC CTRL CHK:			4 1 4 A
MFG ENGR CHK:			
Changed by: yaver	Date Changed: Friday, March 15, 2002	Time Changed: 5:56:48 pm	QA CHK:
REV:		Drawing Number:	Page: 1



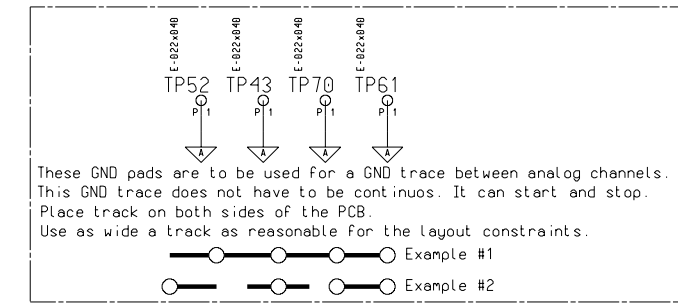
C



Example #1

Example #2

Page :
1

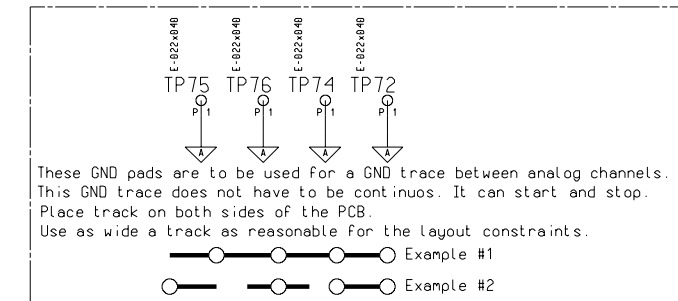


ADC_CLK_P

ADC_CLK_N

Differential pair controlled impedance of 100 ohm.

Engineer:	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		
Drawn by:			
R&D CHK:	TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END		SIZE C
DOC CTRL CHK:			4 1 4 A
MFG ENGR CHK:			
Changed by: yaver	Date Changed: Friday, March 15, 2002	Time Changed: 5:56:48 pm	QA CHK:
REV:		Drawing Number:	Page: 1



ADC_CLK_P

ADC_CLK_N

Differential pair controlled impedance of 100 ohm.

Engineer: Harold Yaver	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		
Drawn by: Harold Yaver			
R&D CHK:	TITLE: SCHEMATIC DIAGRAM, GRETINA - ANALOG FRONT END		SIZE C
DOC CTRL CHK:			4 1 4 A
MFG ENGR CHK:			
Changed by: yaver	Date Changed: Friday, March 15, 2002	Time Changed: 5:56:48 pm	QA CHK:
REV:		Drawing Number:	Page: 1

A

B

C

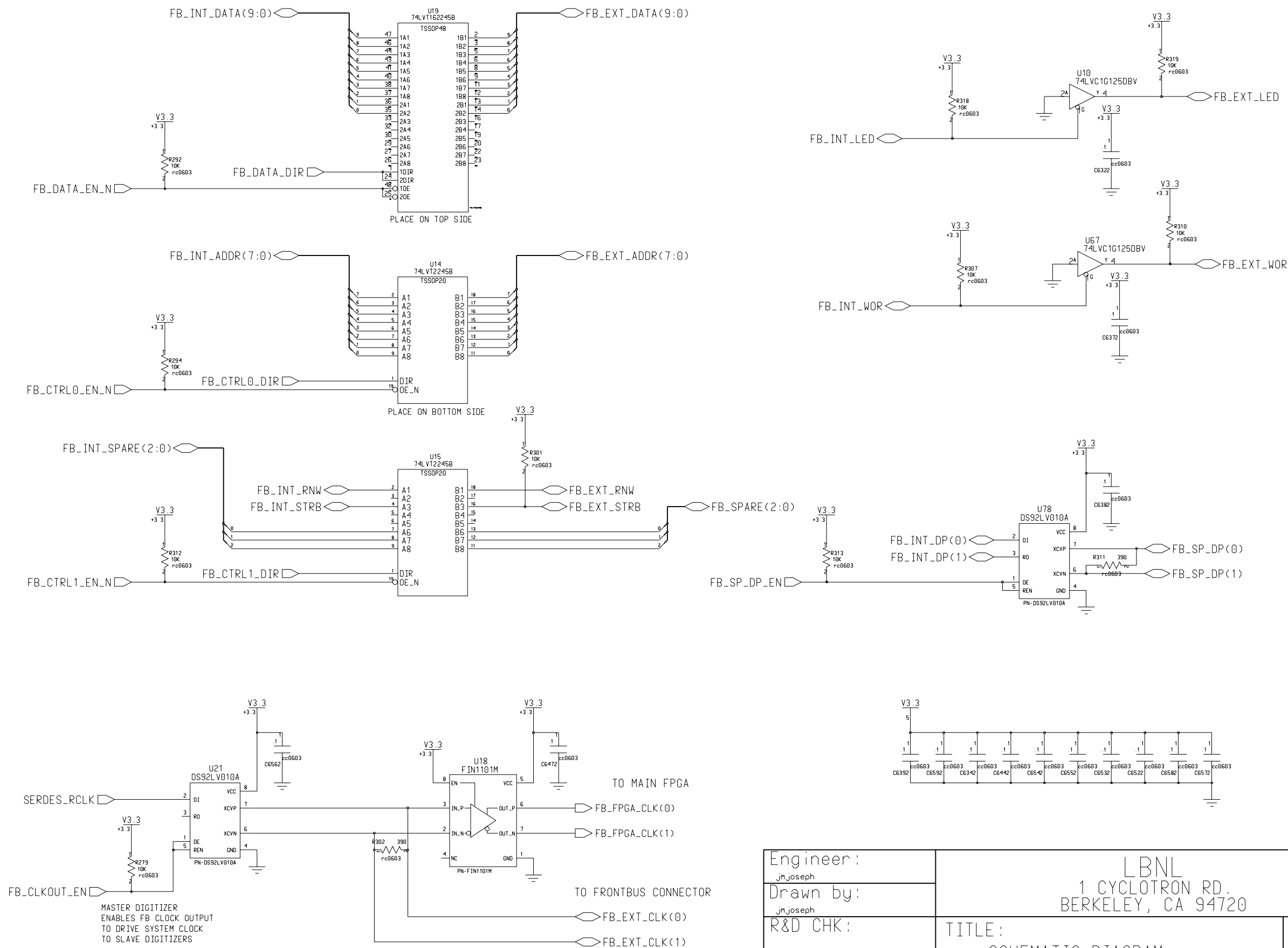
D

A

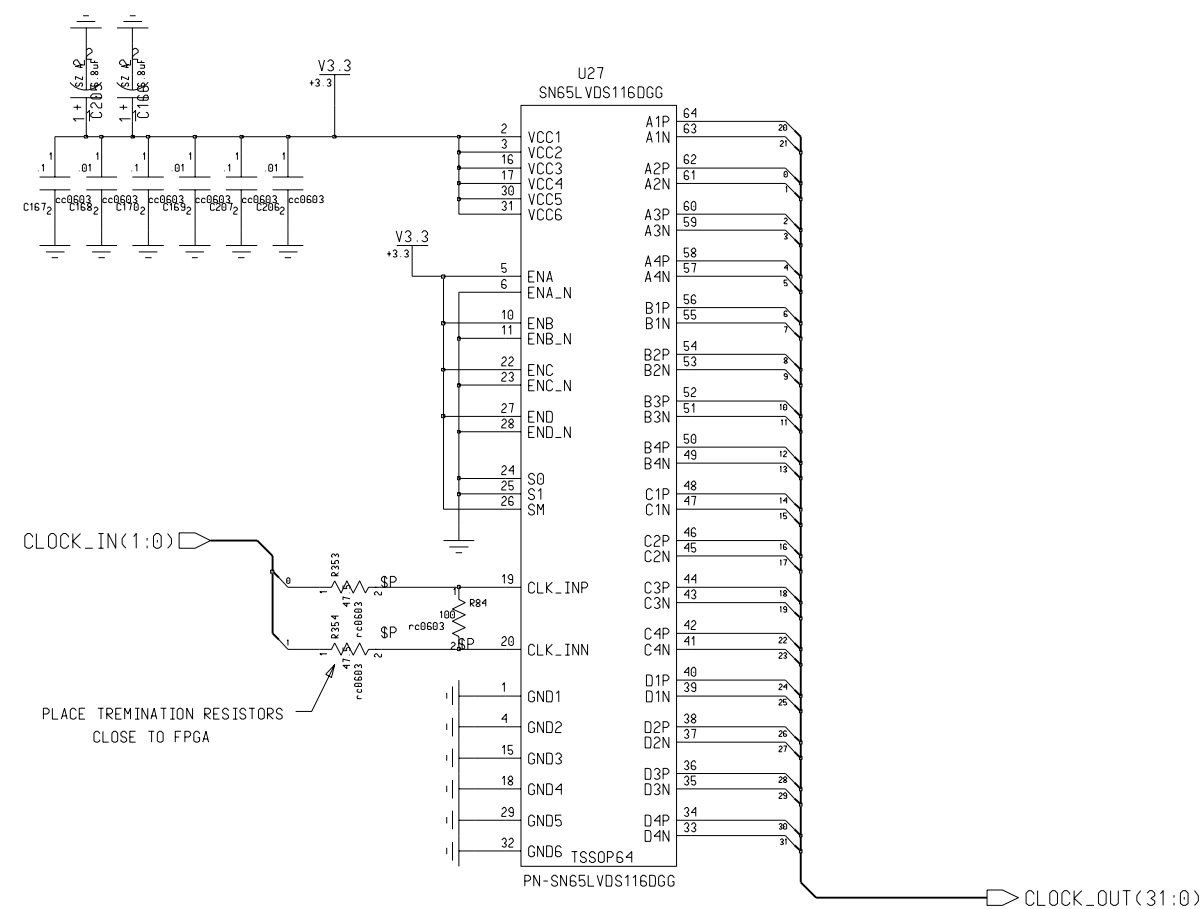
B

C

D

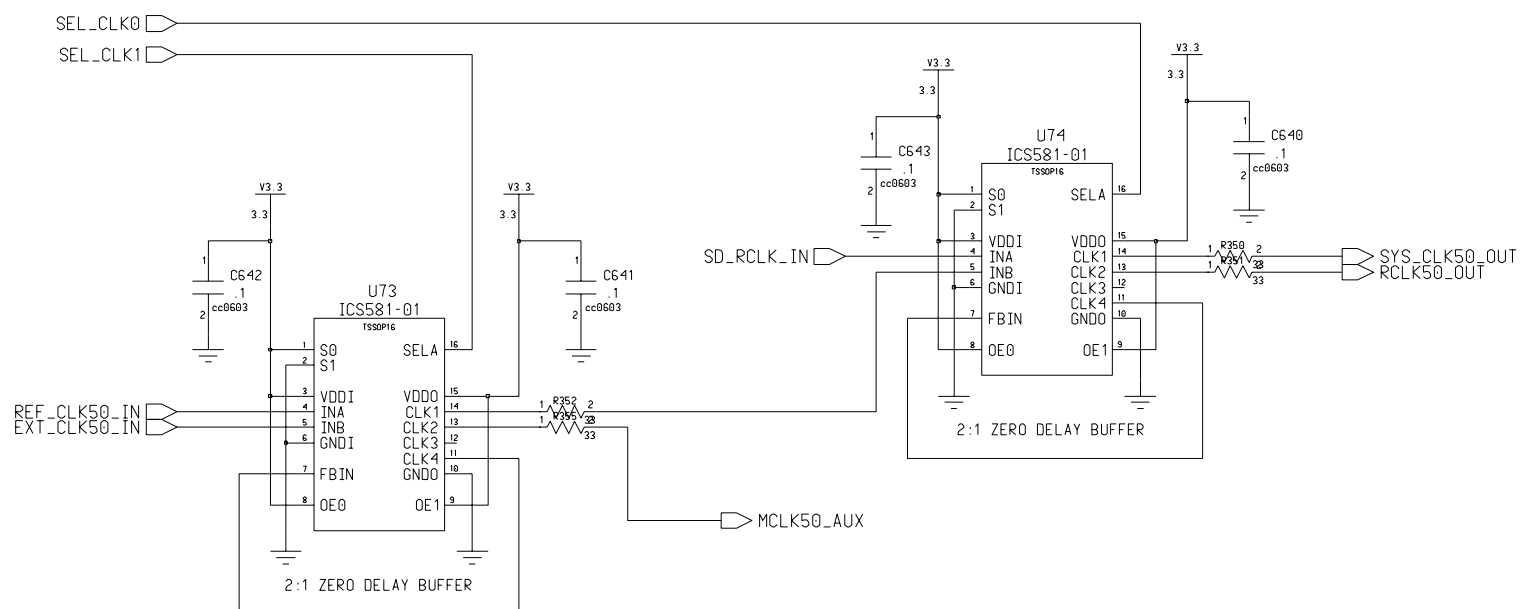


Engineer:	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		
Drawn by:			
R&D CHK:	TITLE: SCHEMATIC DIAGRAM: GRETINA - FRONTBUS BUFFERS		Size: c
DOC CTRL CHK:			4 1 4 A
MFG ENGR CHK:			
QA CHK:	REV:	Drawing Number:	Page: 1



Engineer: jm.joseph	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720		
Drawn by: jm.joseph			
R&D CHK:	TITLE: SCHEMATIC DIAGRAM, GRETINA - CLOCK FAN OUT		SIZE C
DOC CTRL CHK:			4 1 4 A
MFG ENGR CHK:			
QA CHK:	REV: A	Drawing Number:	Page: 1

Changed by: jm.joseph	Date Changed: Wednesday, July 19, 2006	Time Changed: 12:33:44 am
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Engineer: jm.joseph	LBNL 1 CYCLOTRON RD BERKELEY, CA 94707		
Drawn by: jm.joseph			
R&D CHK:	TITLE: GRETINA DIGITIZER SCHEMATIC DIAGRAM 50MHZ CLOCK MUX		Size: c
DOC CTRL CHK:			4 1 4 A
MFG ENGR CHK:			
QA CHK:	REV:	Drawing Number:	Page: 1

Changed by: jm.joseph	Date Changed: Wednesday, August 23, 2006	Time Changed: 11:51:34 pm
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A

B

C

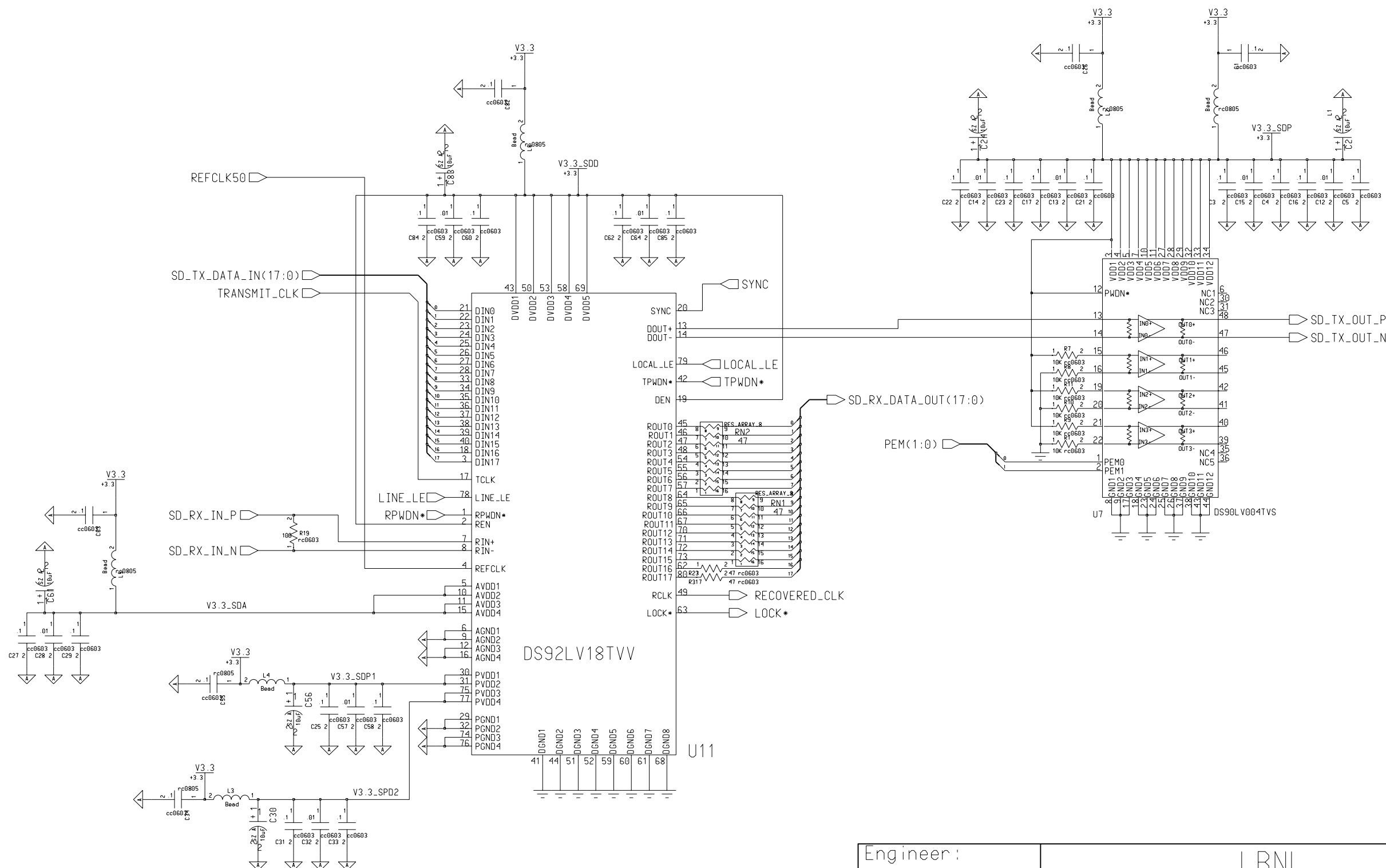
D

A

B

C

D



Engineer:

yaver

Drawn by:

yaver

R&D CHK:

DOC CTRL CHK:

MFG ENGR CHK:

Time Changed:QA CHK:

9:50:52 am

LBNL
1 CYCLOTRON RD.
BERKELEY, CA 94720

TITLE:

SCHEMATIC DIAGRAM,
GRETINA - SERIALIZER DESERIALIZER

SIZE
C

414A

Changed by:

yaver

Date Changed:

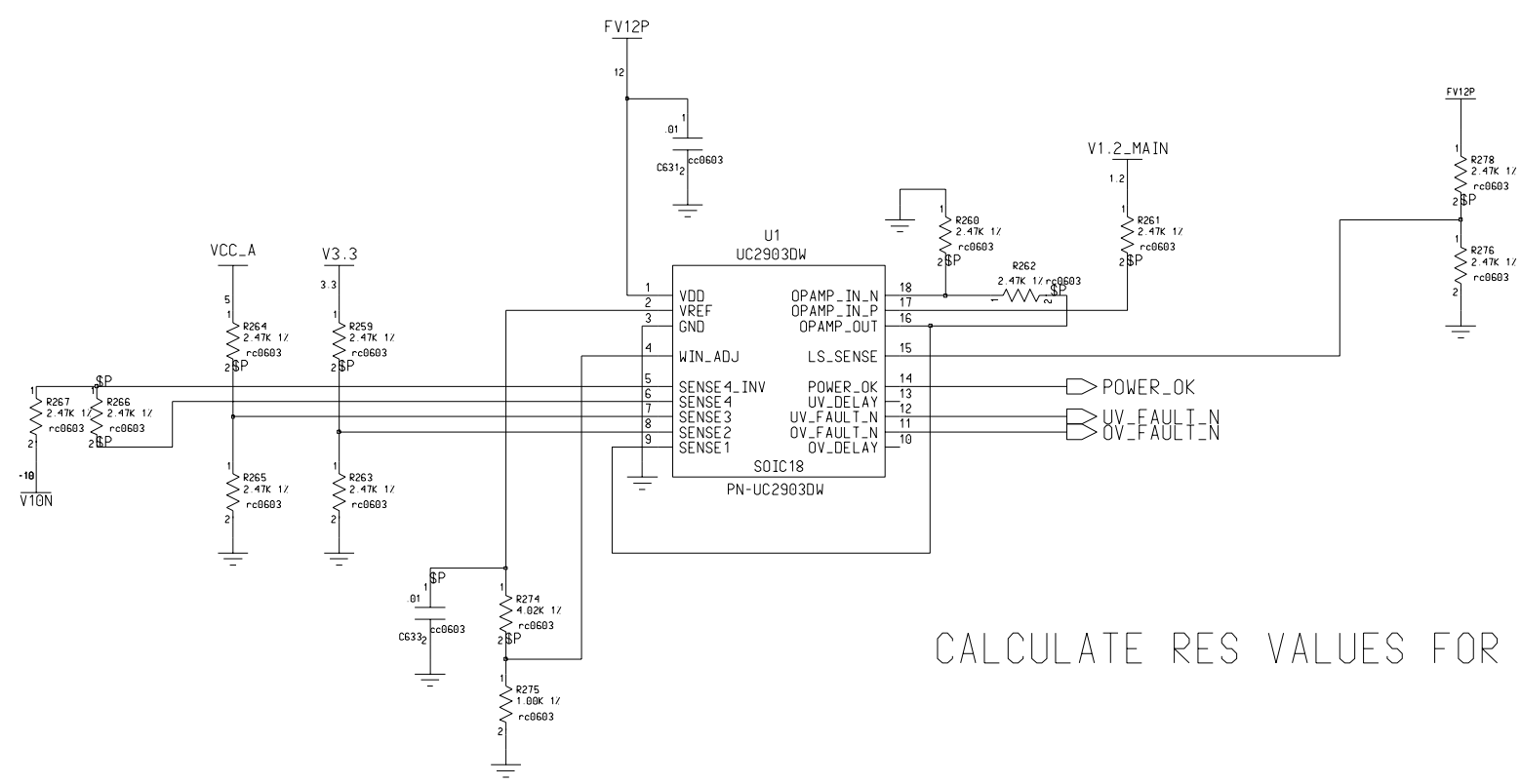
Friday, June 9, 2006

REV:

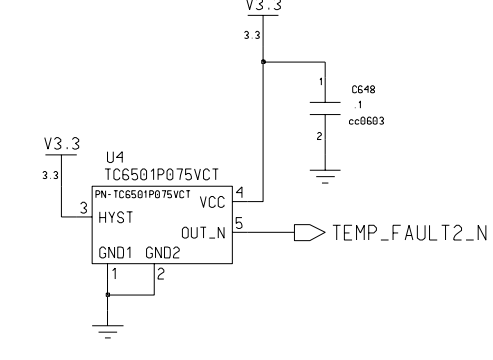
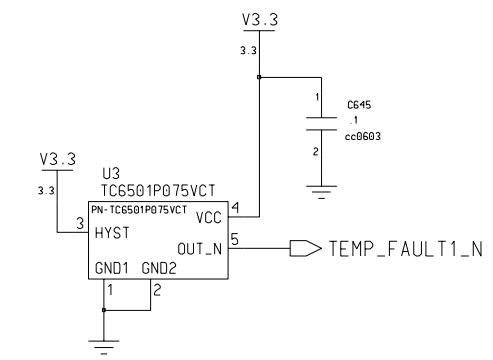
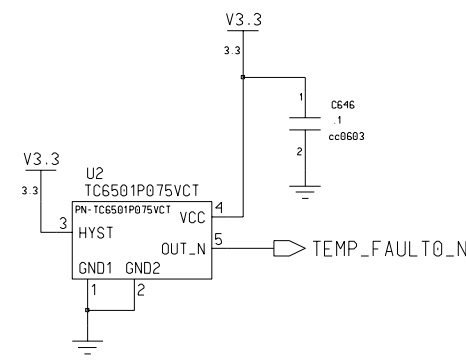
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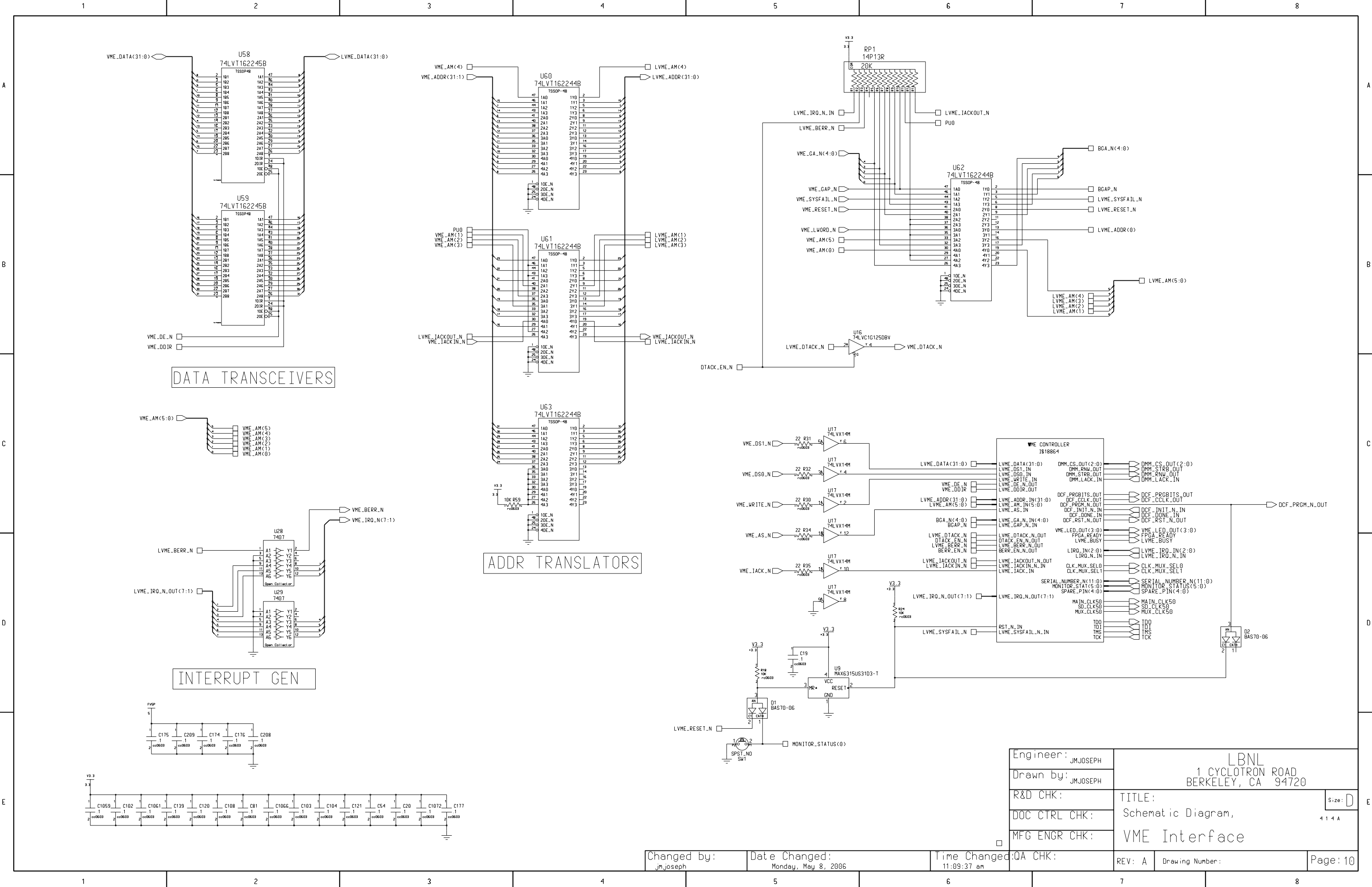
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CALCULATE RES VALUES FOR VOLTAGE MONITORING



Engineer: jm.joseph	LBNL 1 CYCLOTRON RD. BERKELEY, CA 94720			SIZE C
Drawn by: jm.joseph				
R&D CHK:	TITLE: SCHEMATIC DIAGRAM, GRETINA - VOLTAGE & TEMP MONITOR			4 1 4 A
DOC CTRL CHK:				
MFG ENGR CHK:				
d:QA CHK:	REV: A	Drawing Number:		Page: 1



Engineer: JMJOSEPH	LBNL 1 CYCLOTRON ROAD BERKELEY, CA 94720		
Drawn by: JMJOSEPH			
R&D CHK:	TITLE: Schematic Diagram, VME Interface		
DOC CTRL CHK:			
MFG ENGR CHK:			
Changed by: jmjoseph	Date Changed: Monday, May 8, 2006	Time Changed: 11:09:37 am	QA CHK:
REV: A		Drawing Number:	Page: 10

