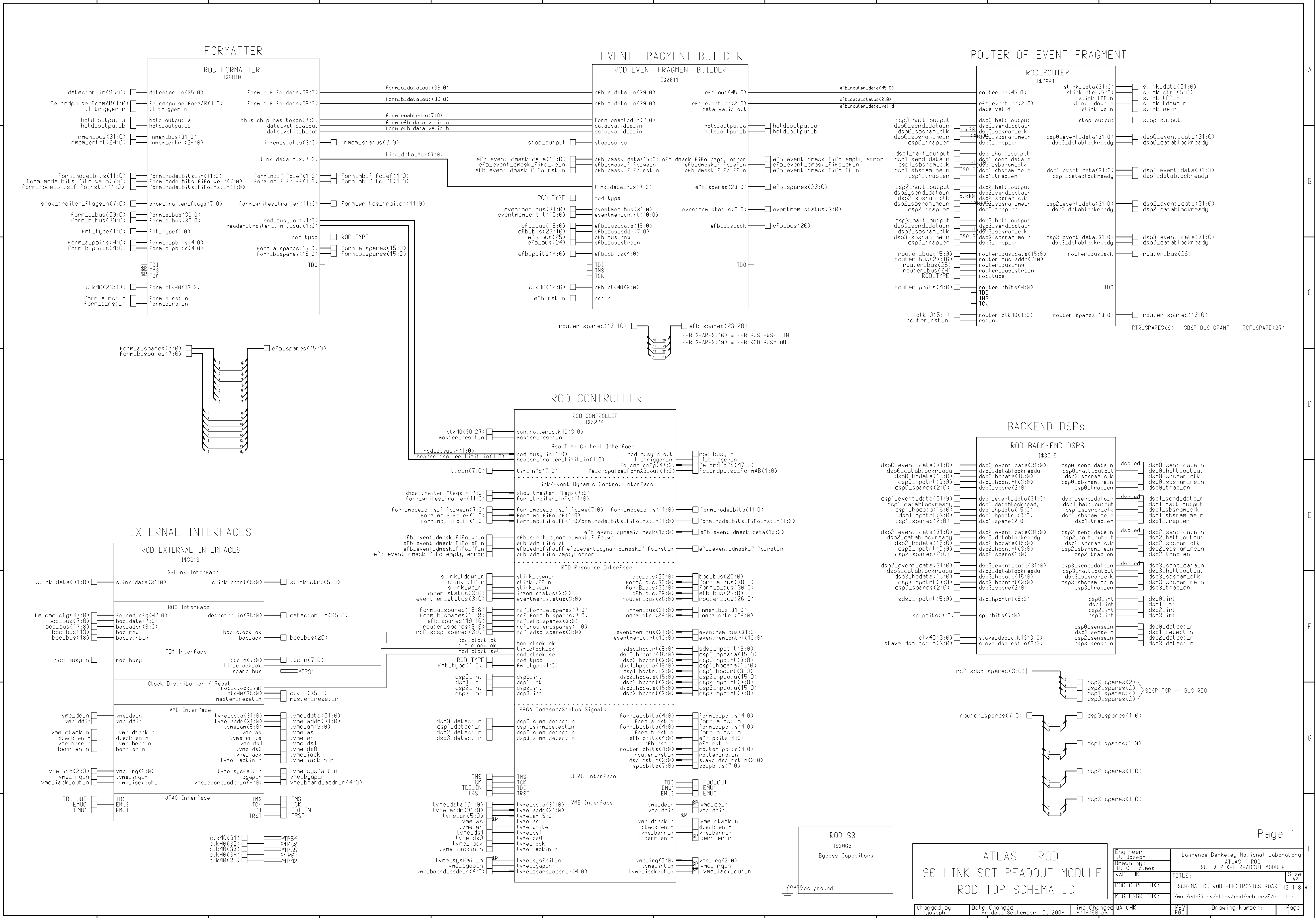
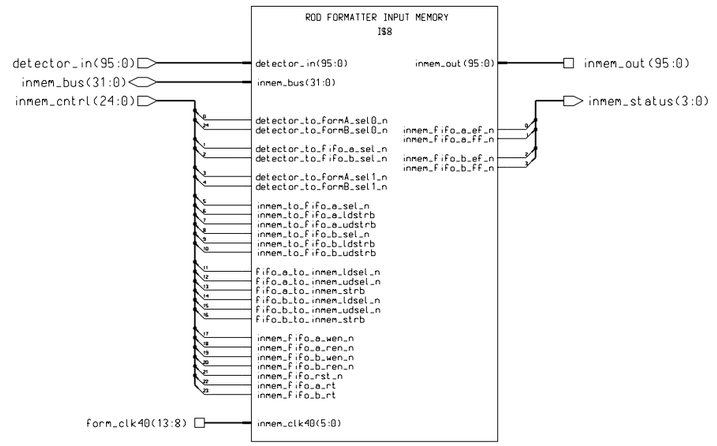
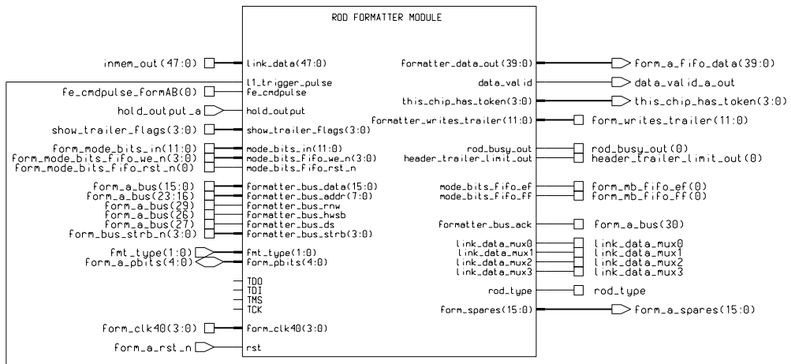
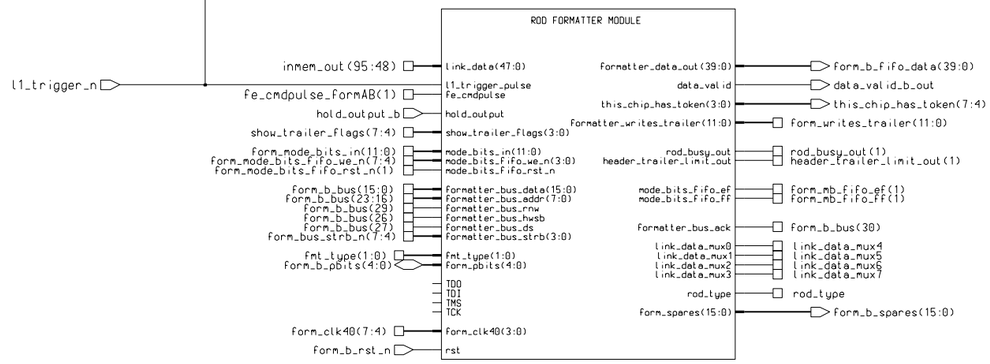
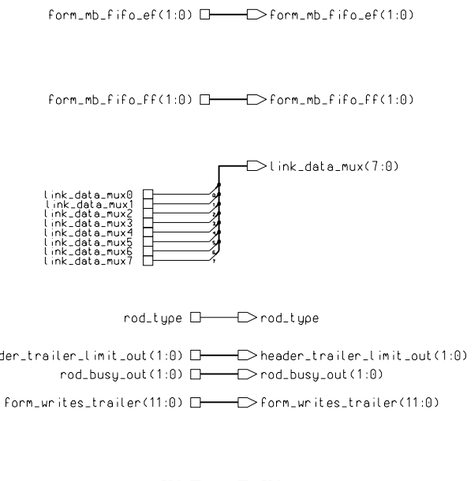


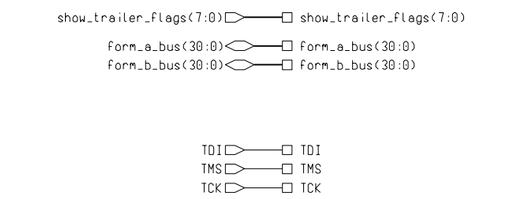
FORMATTER
ROD FORMATTER
I$2810
EVENT FRAGMENT BUILDER
ROD EVENT FRAGMENT BUILDER
I$2811
ROUTER OF EVENT FRAGMENT
ROD_ROUTER
I$7841
RTR_SPARES(9) = SDSP BUS GRANT -- RCF_SPARE(27)
EFB_SPARES(16) = EFB_BUS_HWSEL_IN
EFB_SPARES(19) = EFB_ROD_BUSY_OUT
ROD CONTROLLER
ROD CONTROLLER
I$5274
RealTime Control Interface
Link/Event Dynamic Control Interface
ROD Resource Interface
FPGA Command/Status Signals
JTAG Interface
VME Interface
BACKEND DSPs
ROD BACK-END DSPS
I$3018
SDSP FSR -- BUS REQ
EXTERNAL INTERFACES
ROD EXTERNAL INTERFACES
I$3019
S-Link Interface
BOC Interface
TIM Interface
Clock Distribution / Reset
VME Interface
JTAG Interface
ROD_S8
I$3065
Bypass Capacitors
Page 1
ATLAS - ROD
96 LINK SCT READOUT MODULE
ROD TOP SCHEMATIC
Engineer: J. Joseph
Drawn by: B. C. Holmes
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:
QA CHK:
Lawrence Berkeley National Laboratory
ATLAS - ROD
SCT & PIXEL READOUT MODULE
TITLE:
SCHEMATIC, ROD ELECTRONICS BOARD
Size A2
/mnt/edaFiles/atlas/rod/sch_revF/rod_top
Changed by: jm.joseph
Date Changed: Friday, September 10, 2004
Time Changed: 4:14:50 pm
REV F00
Drawing Number:
Page: 1

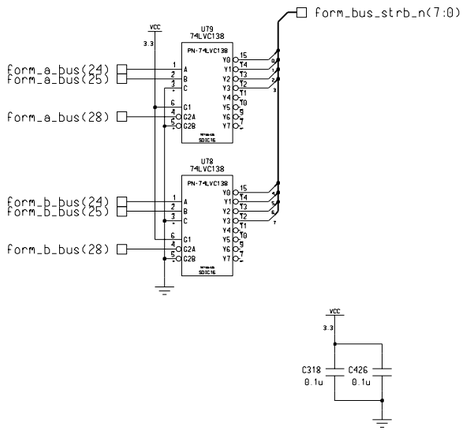






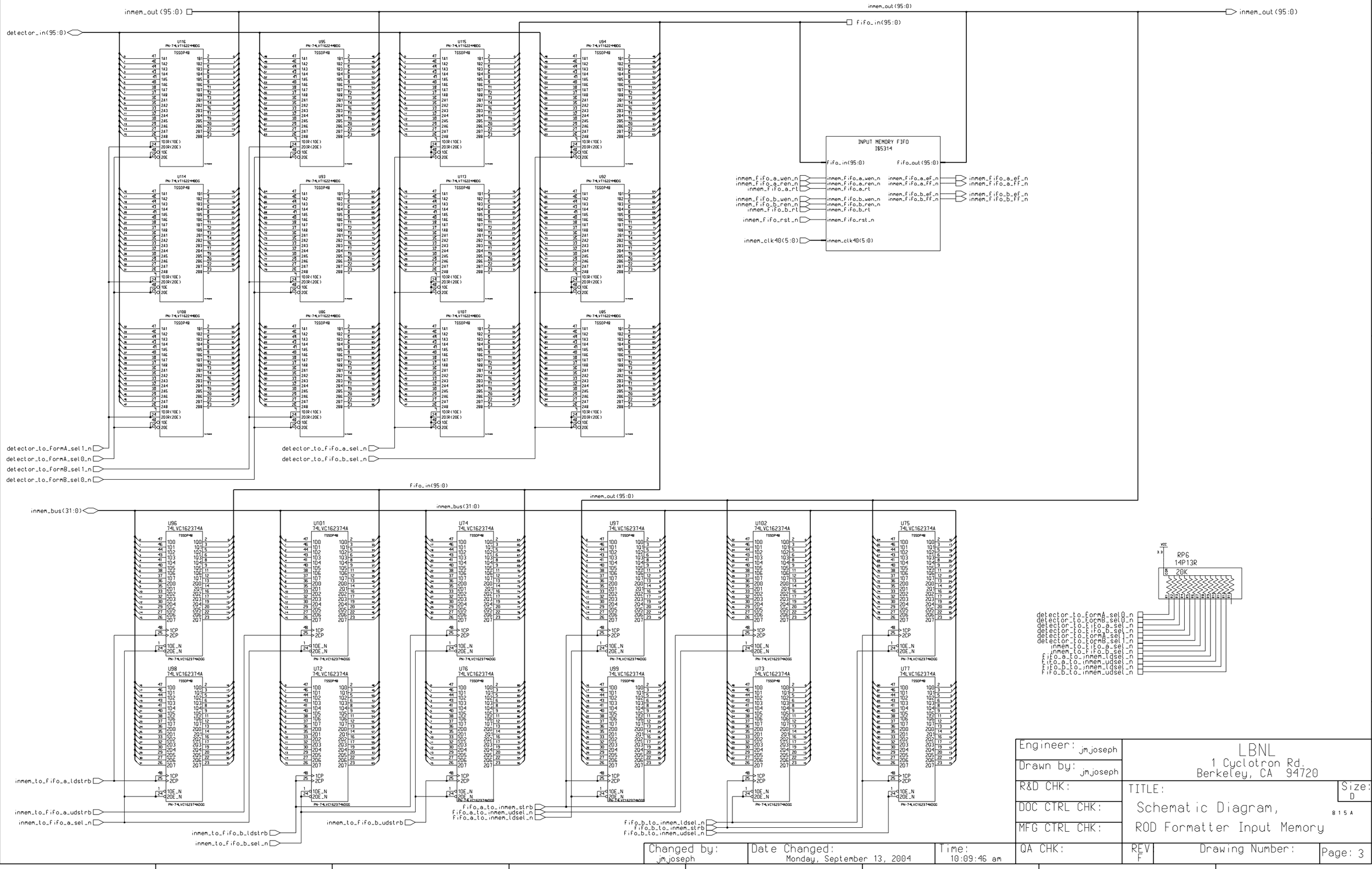




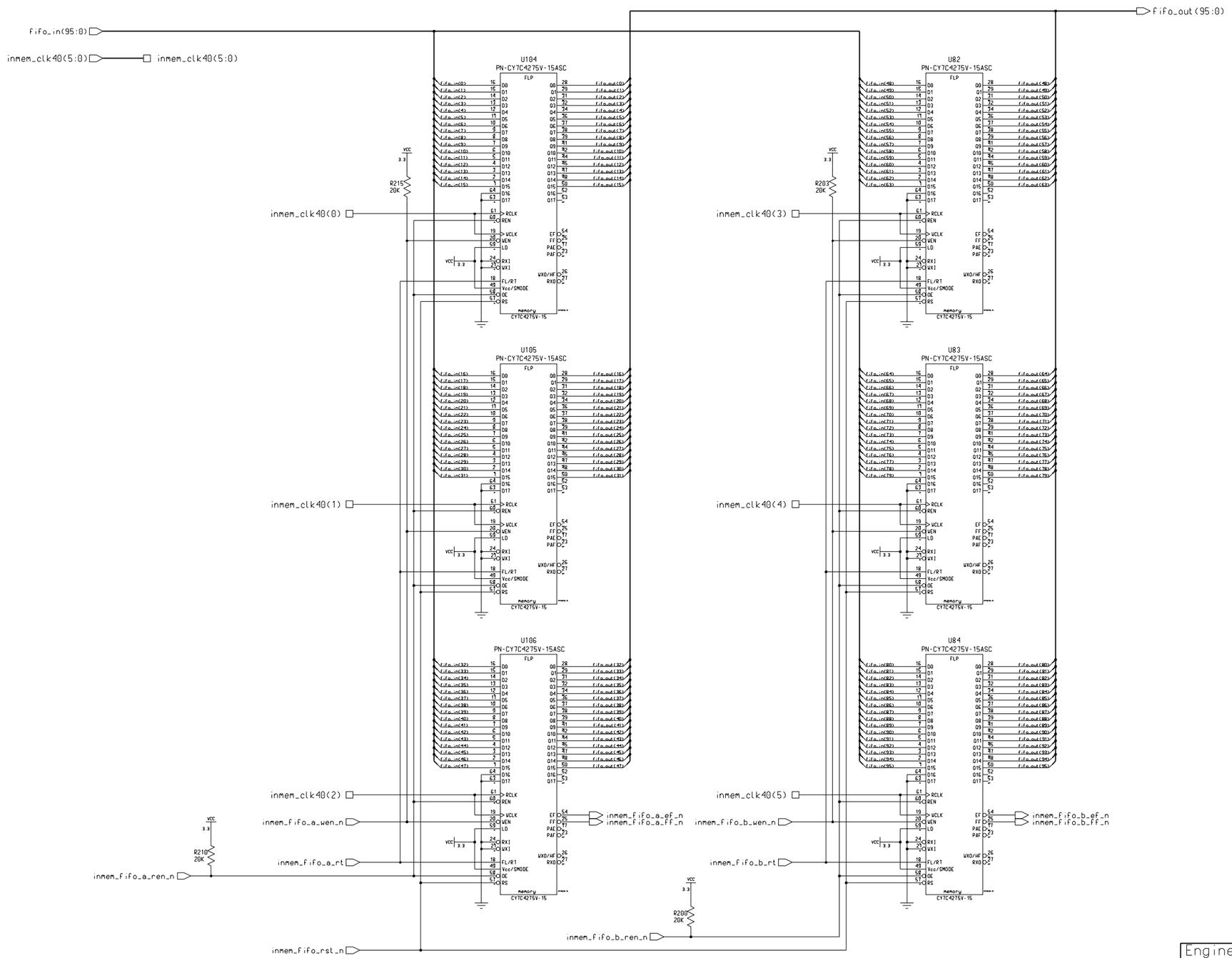


Changed by: jmjoseph	Date Changed: Monday, September 13, 2004	Time: 10:08:43 am	QA CHK:	REV F	Drawing Number:	Page: 2	

Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720
Drawn by: jmjoseph	
R&D CHK:	TITLE: Schematic Diagram, ROD Formatter - Top Level
DOC CTRL CHK:	Size: D
MFG CTRL CHK:	8 1 5 A

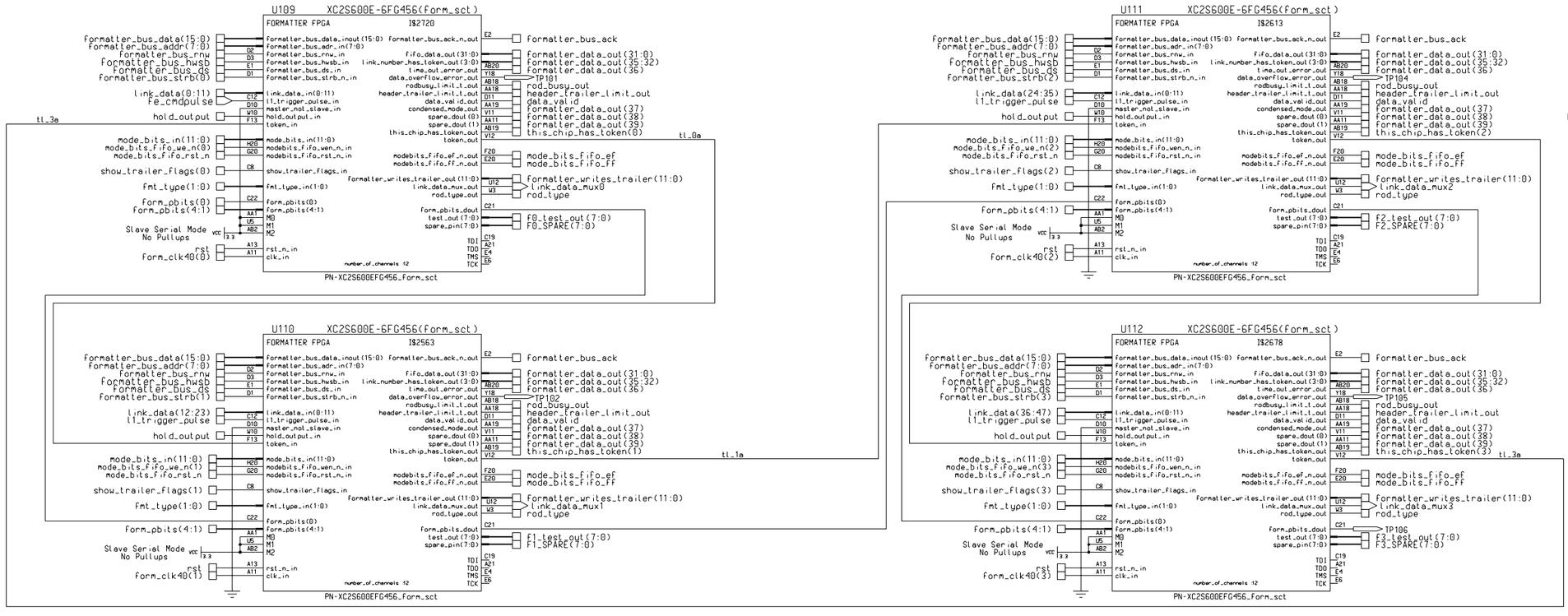


Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720		
Drawn by: jmjoseph			
R&D CHK:	TITLE: Schematic Diagram, ROD Formatter Input Memory	Size: D	8 1 5 A
DOC CTRL CHK:			
MFG CTRL CHK:			
QA CHK:	REV F	Drawing Number:	Page: 3
Changed by: jmjoseph	Date Changed: Monday, September 13, 2004	Time: 10:09:46 am	

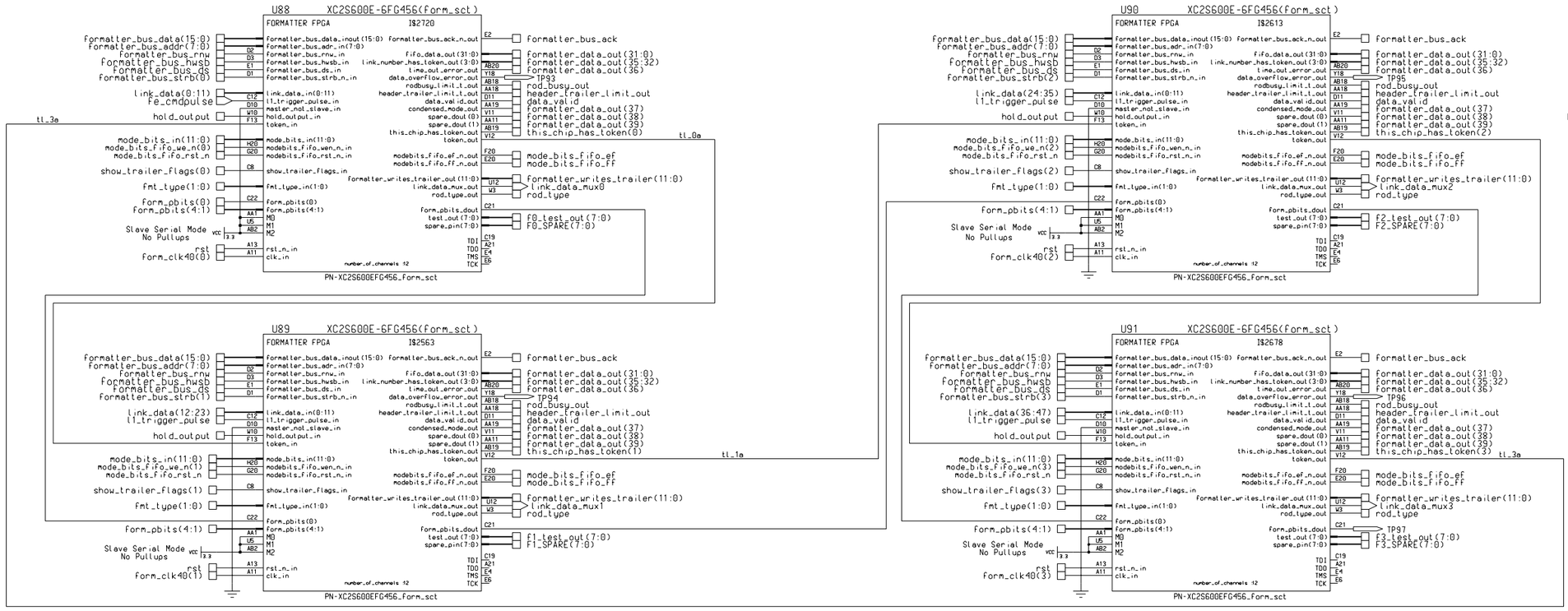


Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720		
Drawn by: jmjoseph			
R&D CHK:	TITLE: Schematic Diagram, ROD Formatter Input Memory FIFO	Size: D (8 1/2 x 11)	
DOC CTRL CHK:			
MFG CTRL CHK:			
QA CHK:	REV F	Drawing Number:	Page: 4

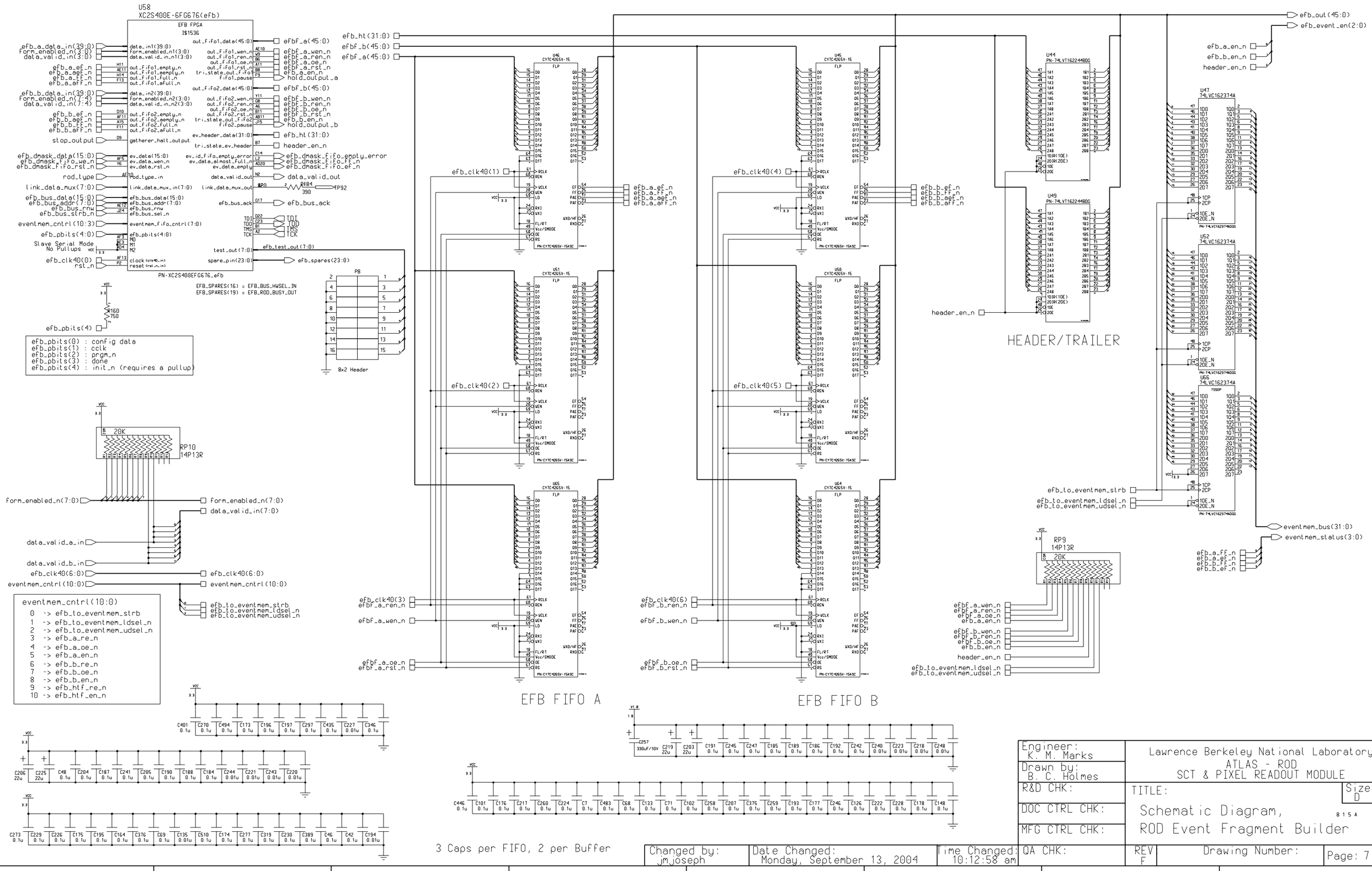
Changed by:	Date Changed:	Time:
jmjoseph	Monday, September 13, 2004	10:10:41 am



Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720		
Drawn by: jmjoseph			
R&D CHK:	TITLE: Schematic Diagram, ROD Formatter Module	Size: D 8 1 5 A	
DOC CTRL CHK:			
MFG CTRL CHK:			
QA CHK:	REV F	Drawing Number:	Page:5/6
Changed by: jmjoseph	Date Changed: Monday, September 13, 2004	Time: 10:12:22 am	



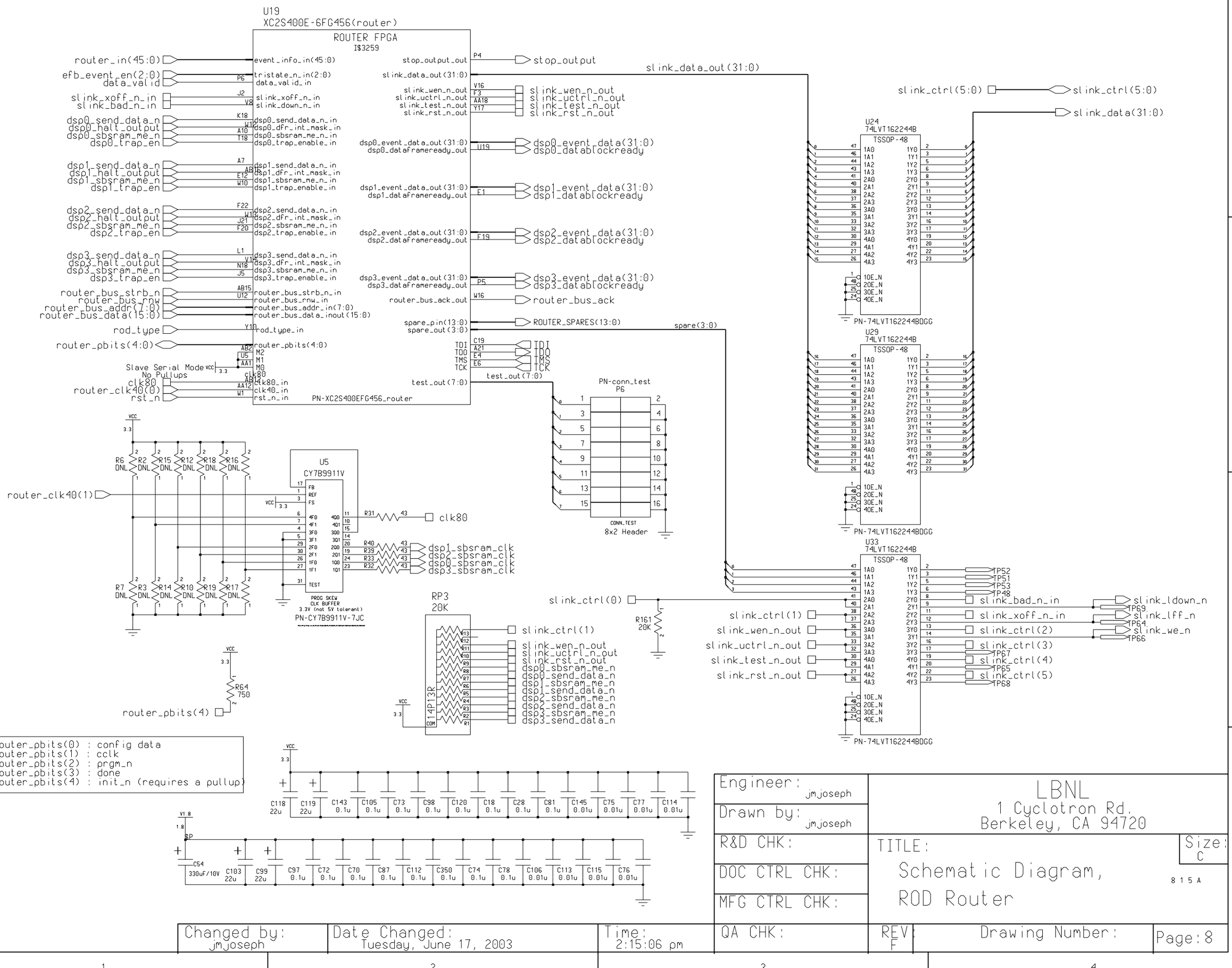
Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720		
Drawn by: jmjoseph			
R&D CHK:	TITLE: Schematic Diagram, ROD Formatter Module	Size: D	8 1 5 A
DOC CTRL CHK:			
MFG CTRL CHK:			
QA CHK:	REV F	Drawing Number:	Page:5/6
Changed by: jmjoseph	Date Changed: Monday, September 13, 2004	Time: 10:12:22 am	



Changed by: jmjoseph	Date Changed: Monday, September 13, 2004	Time Changed: 10:12:58 am	QA CHK:	REV F	Drawing Number:

Engineer: K. M. Marks	Lawrence Berkeley National Laboratory ATLAS - ROD SCT & PIXEL READOUT MODULE	
Drawn by: B. C. Holmes		
R&D CHK:	TITLE: Schematic Diagram, ROD Event Fragment Builder	Size: D 8 1 5 A
DOC CTRL CHK:		
MFG CTRL CHK:		

Page: 7



Changed by: jmjoseph	Date Changed: Tuesday, June 17, 2003	Time: 2:15:06 pm	QA CHK:	REV: F	Drawing Number:

Page: 8

Engineer: jmjoseph

Drawn by: jmjoseph

R&D CHK:

DOC CTRL CHK:

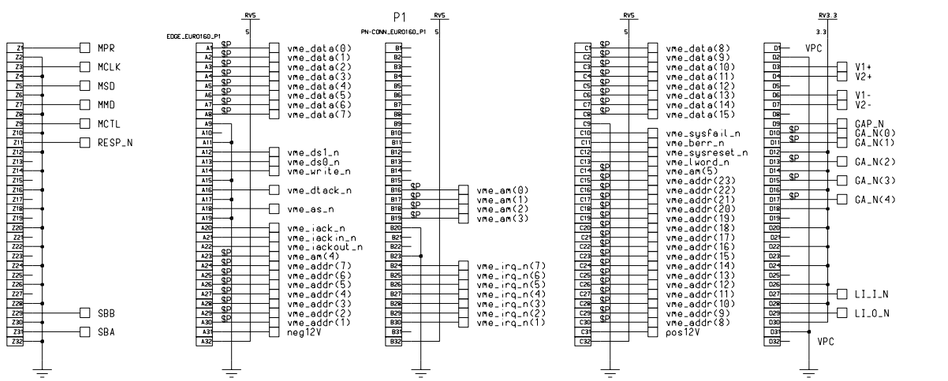
MFG CTRL CHK:

LBNL
1 Cyclotron Rd.
Berkeley, CA 94720

TITLE:
Schematic Diagram,
ROD Router

Size: C

8 1 5 A



Changed by: jmjoseph	Date Changed: Monday, September 13, 2004	Time Changed: 10:14:48 am	QA CHK:	REV: F	Drawing Number:

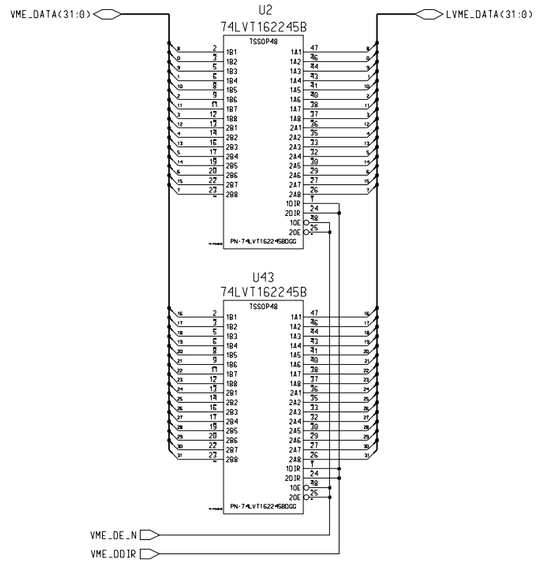
Engineer: J.M. Joseph
Drawn by: B. C. Holmes
R&D CHK:
DOC CTRL CHK:
MFG CTRL CHK:

Lawrence Berkeley National Laboratory
ATLAS - ROD
SCT & PIXEL READOUT MODULE

TITLE:
Schematic Diagram,
ROD - External I/O Top Level

Size: D
8 1 5 A

Page:9



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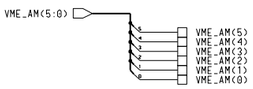

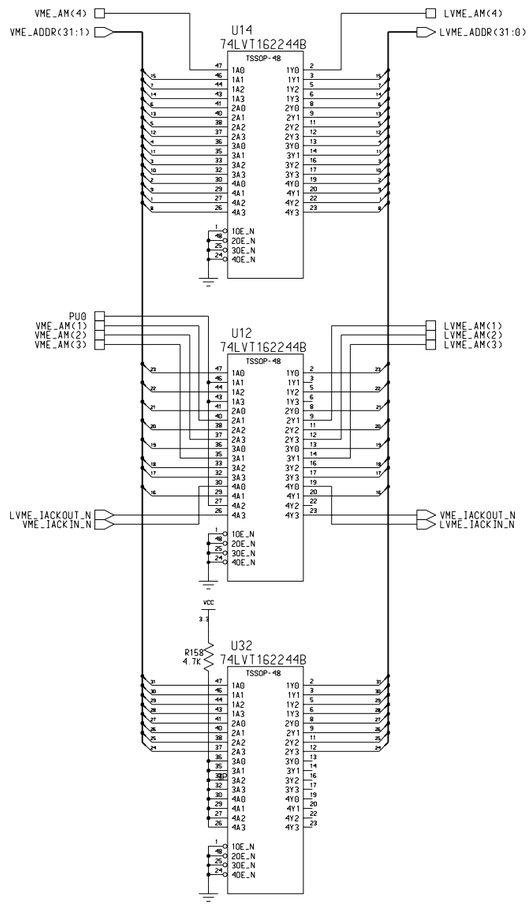

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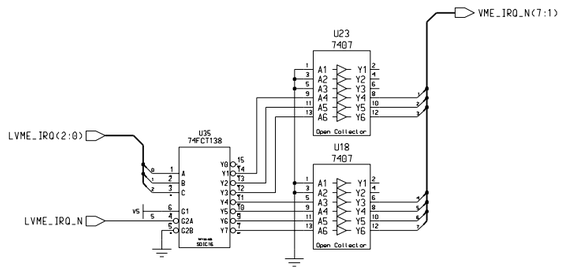
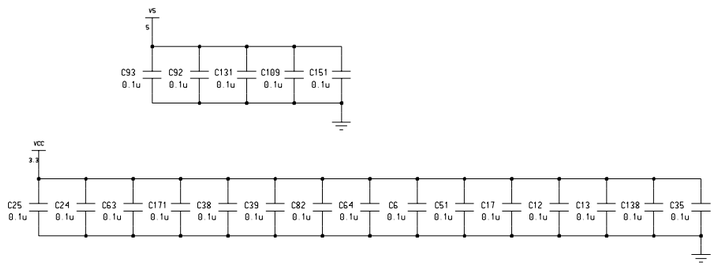
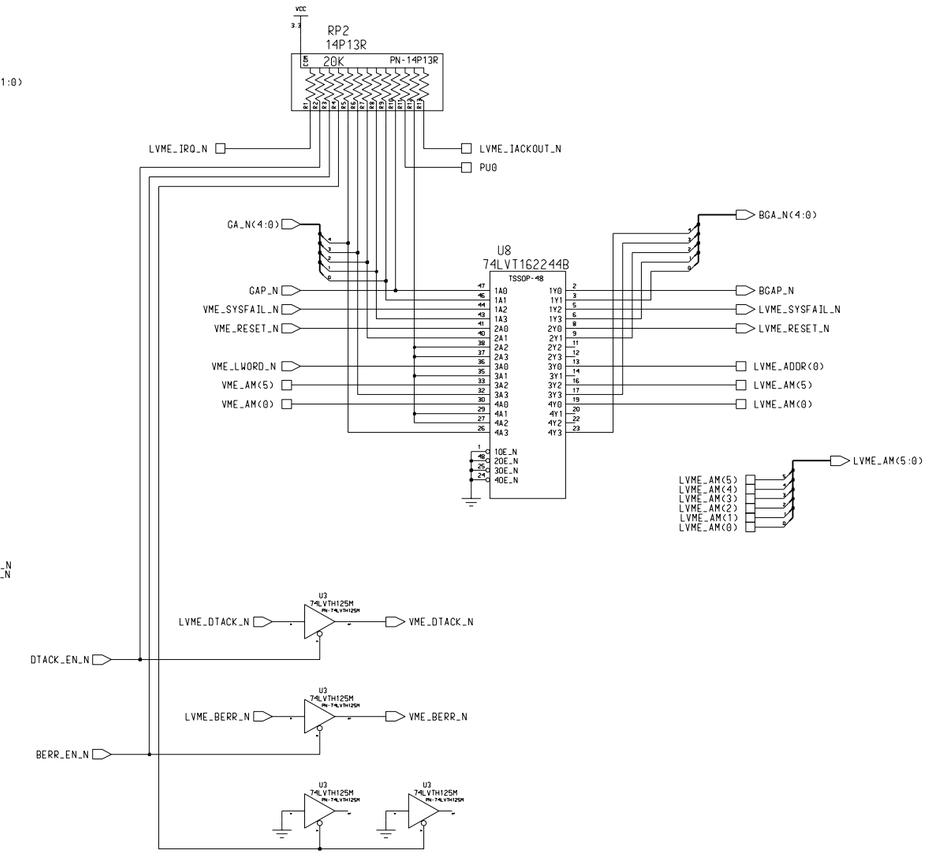
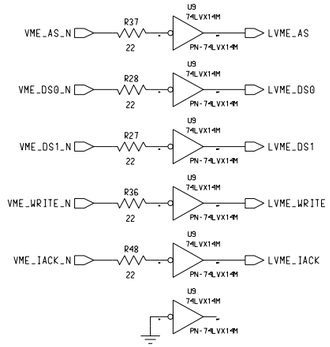


INTERRUPT GEN



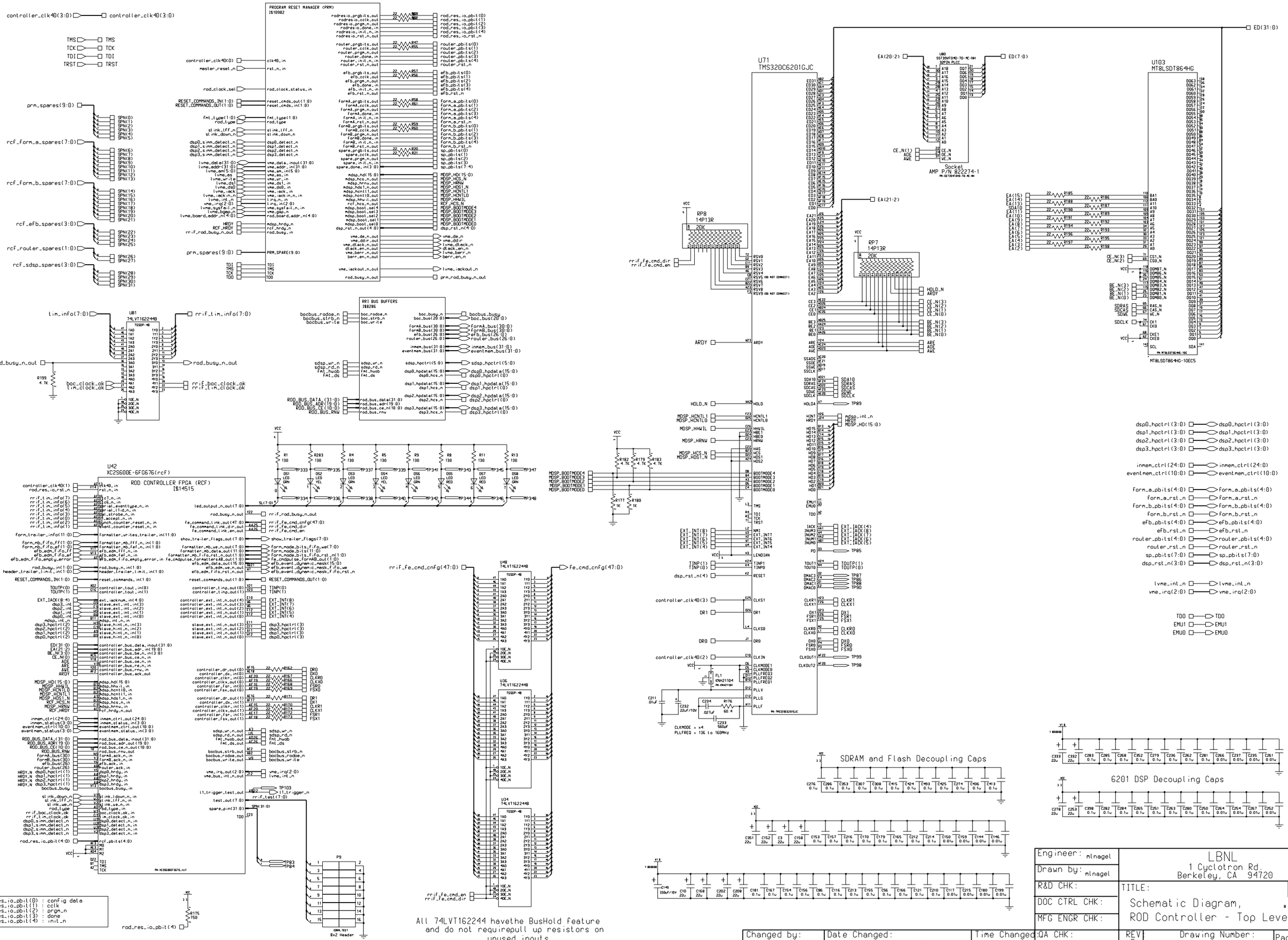


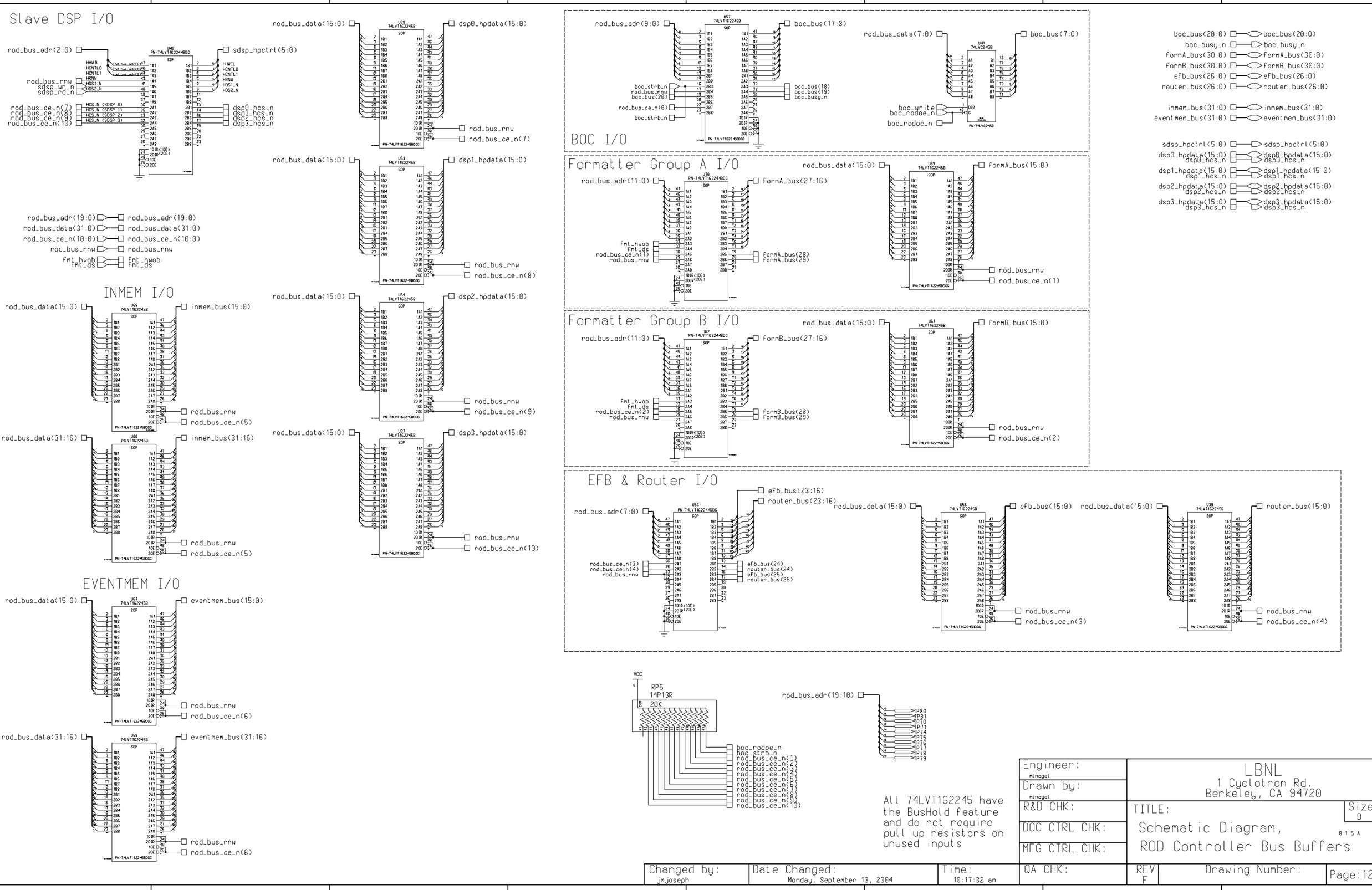


Changed by: jmjoseph	Date Changed: Monday, September 13, 2004	Time Changed: 10:15:43 am	QA CHK:	REV: F	Drawing Number:

Page: 10

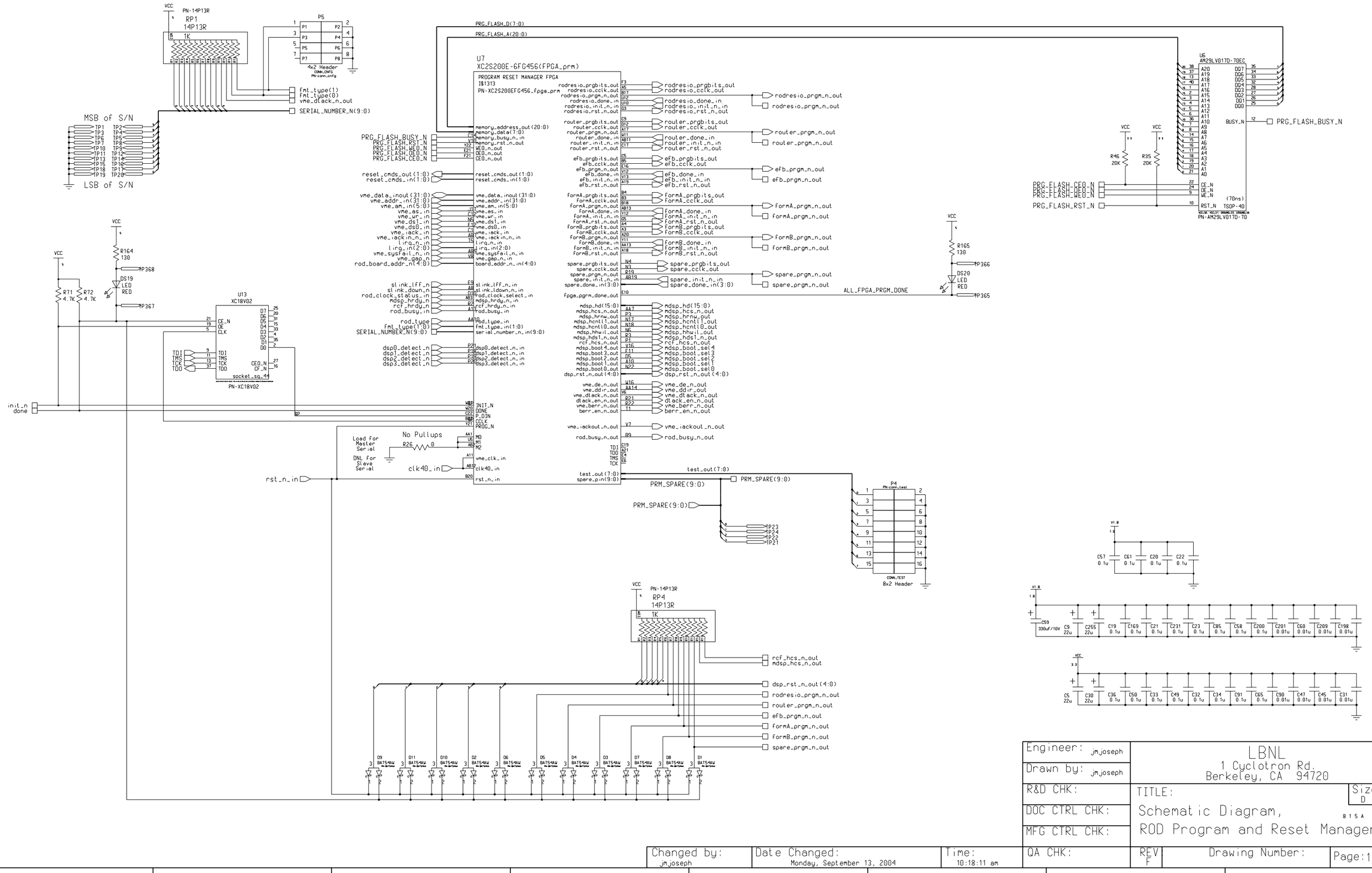
Engineer: JMJOSEPH	LBNL 1 Cyclotron Road Berkeley, CA 94720
Drawn by: JMJOSEPH	
R&D CHK:	TITLE: Schematic Diagram, ROD VME Interface
DOC CTRL CHK:	Size: D
MFG ENGR CHK:	4144A


PROGRAM RESET MANAGER (PRM)
IS10982
ROD CONTROLLER FPGA (RCF)
IS14515
U42
XC2S600E-6FG676(rcf)
U71
TMS320C6201GJC
U80
SST39VF040-70-4C-NH
32PIN PLCC
Socket
AMP P/N 822274-1
U103
MT48LSDT864HG
MT48LSDT864HG-10EC5
U81
74LVT162244B
RR1 BUS BUFFERS
IS8286
RP8
14P13R
20K
RP7
14P13R
20K
U48
74LVT162244B
U36
74LVT162244B
U34
74LVT162244B
P9
8x2 Header
SDRAM and Flash Decoupling Caps
6201 DSP Decoupling Caps
All 74LVT162244 havethe BusHold feature
and do not requirepull up resistors on
unused inputs
rod_res_io_pbit(0) : config date
rod_res_io_pbit(1) : cclk
rod_res_io_pbit(2) : prgm_n
rod_res_io_pbit(3) : done
rod_res_io_pbit(4) : init_n
Changed by: jmjoseph
Date Changed: Monday, September 13, 2004
Time Changed: 10:16:39 am
Engineer: mlnagel
Drawn by: mlnagel
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:
QA CHK:
LBNL
1 Cyclotron Rd.
Berkeley, CA 94720
TITLE: Schematic Diagram, ROD Controller - Top Level
Size: A2
REV .F
Drawing Number:
Page:11



Changed by: jmjoseph	Date Changed: Monday, September 13, 2004	Time: 10:17:32 am	QA CHK:	REV F

Engineer: mlnagel	LBNL 1 Cyclotron Rd. Berkeley, CA 94720
Drawn by: mlnagel	
R&D CHK:	TITLE: Schematic Diagram, ROD Controller Bus Buffers
DOC CTRL CHK:	Size: D
MFG CTRL CHK:	815A
Drawing Number:	Page:12



Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720		
Drawn by: jmjoseph			
R&D CHK:	TITLE: Schematic Diagram, ROD Program and Reset Manager	Size: D 8 1 5 A	
DOC CTRL CHK:			
MFG CTRL CHK:			
Changed by: jmjoseph	Date Changed: Monday, September 13, 2004	Time: 10:18:11 am	QA CHK:
REV F	Drawing Number:	Page:13	

Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720				
Drawn by: jmjoseph					
R&D CHK:	TITLE: Schematic Diagram, ROD Slave DSP Top	Size: A2 8 1 5 A			
DOC CTRL CHK:					
MFG CTRL CHK:					
Changed by: jmjoseph	Date Changed: Monday, September 13, 2004	Time: 10:18:42 am	QA CHK:	REV: F	Drawing Number: Page:14