ROD Operations Manual

APPENDIX B:
ROD VME Access Registers

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Revision History	
July 12, 2002	First Draft
August 12, 2002	Added Flash Memory Command Algorithms, VME Byte Order
September 22, 2005	Added ROD Busy Histogram Memory and Control
September 27, 2005	Added TMS320C6713 Memory Map Added ROD Busy Histogram Trigger Enable

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VME Chipset

The ROD uses the CY7C960A as a slave controller in I/O mode, and CY7C964 interface chips as bus transceivers.

VME Address Map

The VMEbus Address Decoding Block is implemented in the PRM FPGA and decodes the ROD memory map into Regions as required by the VMEBus Interface.

VME Address/ROD Region Decoder

The ROD uses 32 bits of address LA(31:0).

LA(31:24) are compared to the Geographical Address GA to select the active ROD board. The RODs occupy slots 5 to 12 and 14 to 21 and the geographical address of each board is as follows:

```
Slot 5  -> GA/LA[31:24] = "00000101" (05h)
Slot 6  -> GA/LA[31:24] = "00000110" (06h)
Slot 7  -> GA/LA[31:24] = "00000111" (07h)
Slot 8  -> GA/LA[31:24] = "00001000" (08h)
Slot 9  -> GA/LA[31:24] = "00001001" (09h)
Slot 10 -> GA/LA[31:24] = "00001010" (0Ah)
Slot 11 -> GA/LA[31:24] = "00001011" (0Bh)
Slot 12 -> GA/LA[31:24] = "00001100" (0Ch)
Slot 13 -> TIM
Slot 14 -> GA/LA[31:24] = "00001110" (0Eh)
Slot 15 -> GA/LA[31:24] = "00001111" (0Fh)
Slot 16 -> GA/LA[31:24] = "00010000" (10h)
Slot 17 -> GA/LA[31:24] = "00010001" (11h)
Slot 18 -> GA/LA[31:24] = "00010010" (12h)
Slot 19 -> GA/LA[31:24] = "00010011" (13h)
Slot 20 -> GA/LA[31:24] = "00010100" (14h)
Slot 21 -> GA/LA[31:24] = "00010101" (15h)
```

If the address match is true, then LA(23:20) is used to decode the function specific ROD Region Map, and the valid map is returned to the VMEBus Interface IC (CY7C960A).

ROD Memory Map to Region Map
REGION(2:0) = "000", ROD Master DSP Host Port - CS_N(1)
GA**0**XXXXX – HPI Control register
GA**2**XXXXX – HPI Address register

REGION(2:0) = "001", ROD Master DSP Host Port - CS_N(1)
GA**4**XXXXX – HPI Data register, address auto increment
GA**5**XXXXX – HPI Data register, address auto increment
GA**6**XXXXX - HPI Data register, no address auto increment
GA**7**XXXXX - HPI Data register, no address auto increment

REGION(2:0) = "100", Reserved – CS_N(0)
GA**8**XXXXX to GA**B**XXXXX - **Reserved**

REGION(2:0) = "010", FPGA Program Reset Manager - CS_N(2)
GA**C**XXXXX – PRM Registers

All other values for bits 23:20 result in no operation on the selected ROD.
REGION(2:0) = "101" to "111" – **Reserved**

Access to any reserved region will cause a VME bus time-out (BERR*).

ROD VME Data Transfer Format
The VME Interface document defines all data byte transfers as Big Endian.
The ROD transfers data as words only, does not support byte access.

ROD Master DSP Host Port
A detailed description of the Host Port can be found in the **TMS320C6000 Peripherals Reference Guide,** Literature Number: SPRU190D February 2001. Much of the text below is pasted directly from the above-mentioned document.

The Master DSP HPI Registers are located as follows on the ROD:

Description	Address	Access	Width
Master DSP: HPIC, Host Port Interface Control Register	{BA}000000	RW	32
		Bit Value	
Bits[31: 0]: HPIC		Value	

The HPIC register is normally the first register accessed to set configuration bits and initialize the interface. The HPIC is organized as a 32-bit register whose high half word and low half word contents are the same. On a host write, both half words must be identical. The lower half word is the write register, and the upper half word is the status register. No storage is allocated for the read-only reserved values. Only CPU writes to the lower half word affect HPIC values and HPI operation.

31-21	20	19	18	17	16
Reserved	FETCH	HRDY	HINT	DSPINT	HWOB

15-5	4	3	2	1	0
Reserved	FETCH	HRDY	HINT	DSPINT	HWOB

HWOB: Half Word Ordering Bit
If HWOB = 1, the first half word is least significant. If HWOB = 0, the first half word is most significant. HWOB affects both data and address transfers. Only the host can modify this bit. HWOB must be initialized before the first data or address register access.
DSPINT: The host processor-to-CPU/DMA interrupt.
HINT: DSP-to-Host Interrupt
The inverted value of this bit determines the state of the CPU HINT output.
HRDY: Ready Signal to Host
Not masked by HCS (as the HRDY pin is). If HRDY = 0, the internal bus is waiting for an HPI data access request to finish.
FETCH: Host Fetch Request
The value read by the host or CPU from this register field is always 0. The host writes a 1 to this bit to request a fetch into HPID of the word at the address pointed to by HPIA. The 1 is never actually written to this bit, however.

Description	Address	Access	Width
Master DSP: HPIA	{BA}200000	RW	32
Host Port Interface Address Register		Bit Value	
Bits[31: 0]: HPIA		Value	

The HPIA contains the address of the memory accessed by the HPI at which the current access occurs. This address is a 30-bit word address, so the two LSBs are unaffected by HPIA writes and are always read as 0. The

C62x/C67x HPIA register is only accessible by the host. It is not mapped to the DSP memory.

Description	Address	Access	Width
Master DSP: HPID++	{BA}400000	RW	32
Host Port Interface Data Register with Auto Increment		Bit Value	
Bits[31: 0]: HPID++		Value	

Description	Address	Access	Width
Master DSP: HPID	{BA}600000	RW	32
Host Port Interface Data Register no Auto Increment		Bit Value	
Bits[31: 0]: HPID		Value	

Host Access Sequences

The host begins HPI accesses by performing the following tasks in this order:
1) Initializing the HPIC register
2) Initializing the HPIA register
3) Writing data to or reading data from HPID register

Reading from or writing to HPID initiates an internal cycle that transfers the desired data between the HPID register and the DMA auxiliary channel in the C620x/C670x. For the 16-bit HPI, the PRM FPGA handles the D32 to D16 access. The host is able to access the 16 bit wide HPI with a single 32 bit wide cycle.

Initialization of HPIC and HPIA

Before any data access, the HPIC and HPIA must be initialized. On the C62x/C67x, only the host has access to the HPIA register. Before accessing data, the HWOB bit of the HPIC register and the HPIA must be initialized (in this order, because HWOB affects the HPIA access). The ROD requires that the HWOB bit be set to a value of '1'. After initializing HWOB, the host can write to HPIA.

HPID Read/Write Access in Fixed Address Mode

A read or write cycle to the HPID no Auto Increment Register will access a register on the ROD at the specific address set in the HPIA register.

HPID Read/Write Access in Auto Increment Mode

The auto increment feature results in efficient sequential host accesses. For both HPID read and write accesses, this removes the need for the host to load incremented addresses into HPIA. For read accesses, the data pointed to by the next address is fetched immediately after the completion of the current read. Because the intervals between successive reads are used to pre-fetch data, the latency for the next access is reduced. For the C62x/C67x pre-fetching also occurs after a host write of FETCH = 1 to the HPIC register. If the next HPI access is an HPID read, then the data is not re-fetched and the pre-fetched data is sent to the host. Otherwise, the HPI must wait for the pre-fetch to finish.

VME D32 to DSP D16 HPI Interface: Host Port To VME D32 Algorithm

The communication from the Host VME interface is specified as D32. The ROD Master DSP host port is a D16 component. To access the DSP as per the ROD requirements, an interface circuit shall be implemented in the FPGA PRM to allow D32 block transfers to and from the host.
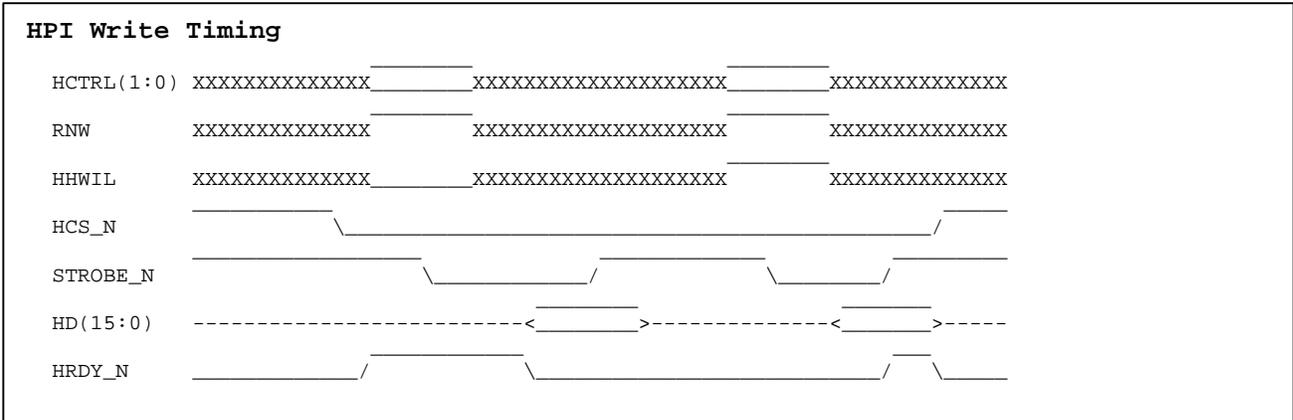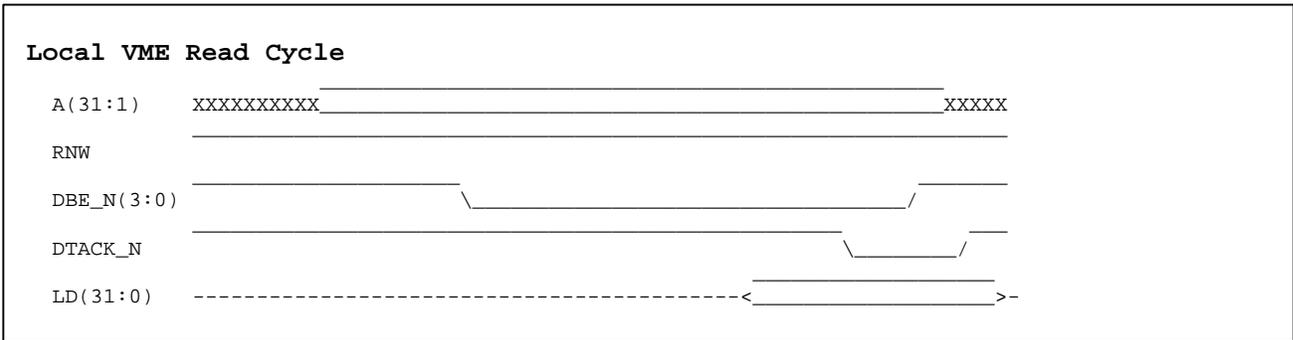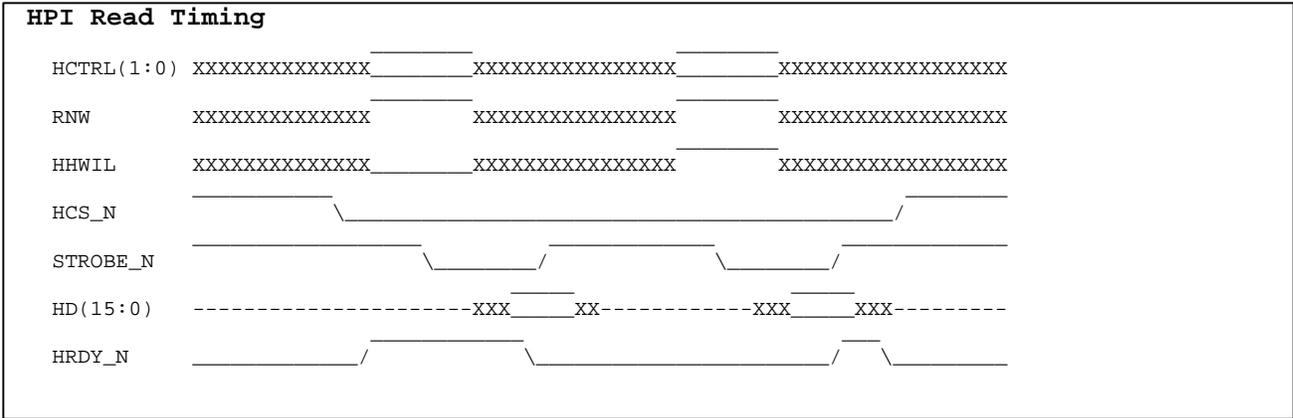
Write Algorithm

If RNW=0, and A(24:20)=DSP access, then DTACK_N will be set to a value of 1 to hold off completion of the VME cycle, D(31:0) will be latched into registers in the PRM when DBE_N(3:0) transitions to 0. HHWIL will be
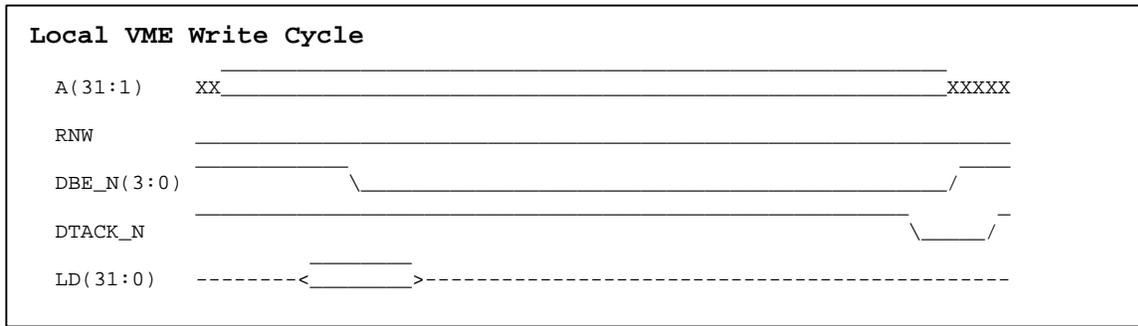
asserted low and D(15:0) will be placed on the HPI data bus, STROBE_N will transition to active, and stay low until HRDY_N transitions from high to low. D(31:16) will be placed on the HPI data bus (D(15:0)), HHWIL will be asserted high, and STROBE_N will transition to active to write the second half-word into the DSP. The state machine will clear STROBE_N, and will wait for HRDY_N to return low before clearing DTACK_N.

Read Algorithm

If RNW=1, and A(24:20)=DSP access, then DTACK_N will be set to a value of 1 to hold off completion of the VME cycle. HHWIL will be asserted low, and then STROBE_N will transition from high to low. When HRDY_N transitions from high to low, the data on the HPI data bus will be latched into the lower half word register in the PRM on the rising edge of STROBE_N. HHWIL will be set high, and STROBE_N will be asserted low again, and the second half-word will be latched into the PRM data register that maps to D(31:16) on the rising edge of STROBE_N. After HRDY_N transitions from high to low, D(31:0) will be placed on the LVME data bus and DTACK_N will be asserted low to complete the VME cycle.

```
HPI Read Timing

                           _____               _____
  HCTRL(1:0) XXXXXXXXXXXXXX_____XXXXXXXXXXXXXXXX_____XXXXXXXXXXXXXXXXX

                           _____               _____
  RNW        XXXXXXXXXXXXXX        XXXXXXXXXXXXXXXX        XXXXXXXXXXXXXXXXX

                                                  _____
  HHWIL      XXXXXXXXXXXXXX_____XXXXXXXXXXXXXXXX        XXXXXXXXXXXXXXXXX

             _____                                        _____
  HCS_N                   _____/

             _____       _____       _____
  STROBE_N                      _____/           _____/

                                     _____                   _____
  HD(15:0)   ---------------------XXX_____XX-----------XXX_____XXX---------

                                 _____                       ___
  HRDY_N     _____/           _____/   _____
```

```
Local VME Read Cycle

                     _____
  A(31:1)    XXXXXXXXXX_____XXXXX

             _____
  RNW

             _____                              _____
  DBE_N(3:0)                    _____/

             _____        ___
  DTACK_N                                               _____/

                                                   _____
  LD(31:0)   ----------------------------------------<_____>-
```

```
HPI Write Timing

                           _____                     _____
  HCTRL(1:0) XXXXXXXXXXXXXX_____XXXXXXXXXXXXXXXXXXXXXX_____XXXXXXXXXXXXX

                           _____                     _____
  RNW        XXXXXXXXXXXXXX        XXXXXXXXXXXXXXXXXXXXXX        XXXXXXXXXXXXX

                                                        _____
  HHWIL      XXXXXXXXXXXXXX_____XXXXXXXXXXXXXXXXXXXXXX        XXXXXXXXXXXXX

             _____                                             ____
  HCS_N                  _____/

             _____       _____       _____
  STROBE_N                    _____/         _____/

                                          _____             _____
  HD(15:0)   ------------------------<_____>-------------<_____>-----

                   _____                       ___
  HRDY_N     _____/           _____/   \_____
```

```
 _____
Local VME Write Cycle
                    _____
   A(31:1)    XX_____XXXXX

   RNW              _____
                    _____                                          ____
   DBE_N(3:0)  _____/
               _____  _
   DTACK_N     _____/
                      _____
   LD(31:0)    --------<_____>------------------------------------------------
```

Functional Procedure: Block Transfer Read from Slave DSP0 CE3 SDRAM to Host

Function	VME Register	Data Value	Notes
Write HWOB Value to Slave0 HPIC	MDSP HPIA 0x{BA}200000	0x00780000	These steps are performed by the Master DSP after a reset, and are not required.
	MDSP HPID 0x{BA}600000	0x00010000	
Write first address location of the block to the Slave HPIA	MDSP HPIA 0x{BA}200000	0x00780004	This location is the first address in CE3 Memory space
	MDSP HPID 0x{BA}600000	0x03000000	
Write Address of the Slave DSP HPID++ to the Master DSP HPIA address	MDSP HPIA 0x{BA}200000	0x00780008	Slave 0 HPID++ Register
Read from the Master DSP HPID	MDSP HPID 0x{BA}600000	Read Data	The Address value used for the Master DSP HPID register can increment from 0x600000 to 0x7FFFFF.

Functional Procedure: Block Transfer Write from the Host to Slave DSP0 CE3 SDRAM

Function	VME Register	Data Value	Notes
Write HWOB Value to Slave0 HPIC	MDSP HPIA 0x{BA}200000	0x00780000	These steps are performed by the Master DSP after a reset, and are not required.
	MDSP HPID 0x{BA}600000	0x00010000	
Write first address location of the block to the Slave HPIA	MDSP HPIA 0x{BA}200000	0x00780004	This location is the first address in CE3 Memory space
	MDSP HPID 0x{BA}600000	0x03000000	
Write Address of the Slave DSP HPID++ to the Master DSP HPIA address	MDSP HPIA 0x{BA}200000	0x00780008	Slave 0 HPID++ Register
Write to the Master DSP HPID	MDSP HPID 0x{BA}600000	Data	The Address value used for the Master DSP HPID register can increment from 0x600000 to 0x7FFFFF.

APPENDIX B: ROD VME Access Registers

The data format of the Master DSP is Little Endian, and the boot mode selected, 8-Bit ROM Boot, defines the DSP Memory Map as shown in table xx.

Address Range	Bytes	Description
ROD MASTER DSP (TMS320C6201) MEMORY MAP		
Address Range	Bytes	Description
00000000-0000FFFF	64K	Internal Program Memory
00010000-003FFFFF	4M-64K	Reserved (Not Used)
00400000-00FFFFFF	12M	Rod Controller (RRIF) Registers, Formatter Registers, EFB Registers, Router Registers, BOC Registers, SDSP (4x), Debug Memory FIFOs (CE0: Asynchronous Memory Configuration)
01000000-013FFFFF	4M	Not Used
01400000-017FFFFF	4M	MDSP Boot FLASH (CE1: Asynchronous Memory Configuration)
01800000-01FFFFFF	8M	Internal DSP Registers (Set by boot code)
02000000-02FFFFFF	16M	DSP SDRAM Memory (CE2)
03000000-03FFFFFF	16M	Unused (CE2) (Available with a larger SO-DIMM)
04000000-7FFFFFFF	2G-64M	Not Used
80000000-8000FFFF	64K	Internal Data RAM
80010000-FFFFFFFF	2G-64K	Reserved (Not Used)

APPENDIX B: ROD VME Access Registers

The data format of the Slave DSP is Little Endian, and the DSP Memory Map is defined in table xx.

ROD SLAVE DSP (TMS320C6713) MEMORY MAP		
Address Range	Bytes	Description
00000000–0002FFFF	192K	Internal RAM (L2)
00030000–0003FFFF	64K	Internal RAM/Cache
00040000–017FFFFF	24M–256K	Reserved
01800000–0183FFFF	256K	External Memory Interface (EMIF) Registers
01840000–0185FFFF	128K	L2 Registers
01860000–0187FFFF	128K	Reserved
01880000–018BFFFF	256K	HPI Registers
018C0000–018FFFFF	256K	McBSP 0 Registers
01900000–0193FFFF	256K	McBSP 1 Registers
01940000–0197FFFF	256K	Timer 0 Registers
01980000–019BFFFF	256K	Timer 1 Registers
019C0000–019C01FF	512	Interrupt Selector Registers
019C0200–019C0203	4	Device Configuration Registers
019C0204–019FFFFF	256K–516	Reserved
01A00000–01A3 FFFF	256K	EDMA RAM and EDMA Registers
01A40000–01AFFFFF	768K	Reserved
01B00000–01B03FFF	16K	GPIO Registers
01B04000–01B3FFFF	240K	Reserved
01B40000–01B43FFF	16K	I2C0 Registers
01B44000–01B47FFF	16K	I2C1 Registers
01B48000–01B4BFFF	16K	Reserved
01B4C000–01B4FFFF	16K	McASP0 Registers
01B50000–01B53FFF	16K	McASP1 Registers
01B54000–01B7BFFF	160K	Reserved
01B7C000–01B7DFFF	8K	PLL Registers
01B7E000–01BBFFFF	264K	Reserved
01BC0000–01BFFFFF	256K	Emulation Registers
01C00000–01FFFFFF	4M	Reserved
02000000–02000033	52	QDMA Registers
02000034–02FFFFFF	16M–52	Reserved
03000000–2FFFFFFF	720M	Reserved
30000000–33FFFFFF	64M	McBSP0 Data Port
34000000–37FFFFFF	64M	McBSP1 Data Port
38000000–3BFFFFFF	64M	Reserved
3C000000–3C0FFFFF	1M	McASP0 Data Port
3C100000–3C1FFFFF	1M	McASP1 Data Port
3C200000–7FFFFFFF	1G + 62M	Reserved
80000000–8FFFFFFF	256M	EMIF CE0†
90000000–9FFFFFFF	256M	EMIF CE1†
A0000000–AFFFFFFF	256M	EMIF CE2†
B0000000–BFFFFFFF	256M	EMIF CE3†
C0000000–FFFFFFFF	1G	Reserved

Table xx

† The number of EMIF address pins (EA[21:2]) limits the maximum addressable memory (SDRAM) to 128MB per CE space.

Program Reset Manager

Description		Address	Access	Width
PRM: FPGA Configuration Control Register		**{BA}C00000**	**RW**	**7**
All bits in the Register are Self-Clearing, unless noted otherwise.			**Bit Value**	
			1	**0**
Bit 0: Configure ROD Controller FPGA If this bit is set, the ROD Controller FPGA will be erased and programmed with a Configuration Bit Stream.			Configure Controller	Idle
Bit 1: Configure Formatter A&B If this bit is set, the ROD Formatter FPGA chips will be erased and programmed with a Configuration Bit Stream.			Configure Formatters	Idle
Bit 2: Configure Formatter A&B If this bit is set, the ROD Formatter FPGA chips will be erased and programmed with a Configuration Bit Stream.			Configure Formatters	Idle
Bit 3: Configure EFB If this bit is set, the ROD Event Fragment Builder FPGA will be erased and programmed with a Configuration Bit Stream.			Configure EFB	Idle
Bit 4: Configure Router If this bit is set, the ROD Router FPGA will be erased and programmed with a Configuration Bit Stream.			Configure Router	Idle
Bit 5: Configure All If this bit is set, all of FPGA chips on the ROD will be erased and programmed with a Configuration Bit Stream.			Configure All	Idle

Bit 6: Configure Override
    Bit 6 is used to override the configuration of the ROD. This function is used when the ROD will not exit Configuration Mode automatically. It allows the user to access all of the Flash memories on the ROD in the case that a configuration problem occurs or if the board is powered on for the first time with blank Flash Memories.
    THIS BIT IS NOT SELF-CLEARING
			Override Configure	Idle

Description		Address	Access	Width
PRM: FPGA Reset Control Register		**{BA}C00004**	**RW**	**7**
All bits in the Register are Self-Clearing, unless noted otherwise.			**Bit Value**	
			1	**0**
Bit 0: Reset ROD Controller FPGA If this bit is set, the ROD Controller FPGA will be reset.			Reset	Idle
Bit 1: Reset Formatter A If this bit is set, the Bank A Formatter FPGA chips will be reset.			Reset	Idle
Bit 2: Reset Formatter B If this bit is set, the Bank B Formatter FPGA chips will be reset.			Reset	Idle
Bit 3: Reset EFB If this bit is set, the Event Fragment Builder FPGA will be reset.			Reset	Idle
Bit 4: Reset Router If this bit is set, the Router FPGA will be reset.			Reset	Idle
Bit 5: Reset All If this bit is set, all of FPGA chips on the ROD will be reset.			Reset	Idle

Bit 6: Hold all FPGAs in Reset
    If this bit is set, all of FPGA chips on the ROD will be held in reset.
    THIS BIT IS NOT SELF-CLEARING
			Reset	Idle

Description		Address	Access	Width
PRM: DSP Reset Control Register		**{BA}C00008**	**RW**	**8**
Bits 1 to 6 in the Register are Self-Clearing			**Bit Value**	
			1	**0**
Bit 0: MDSP Boot Mode Select			HPI Boot	ROM Boot
Bit 1: Reset Master DSP If this bit is set, the Master DSP will be reset.			Reset	Idle
Bit 2: Reset Slave DSP0 If this bit is set, Slave DSP0 will be reset.			Reset	Idle
Bit 3: Reset Slave DSP1 If this bit is set, Slave DSP1 will be reset.			Reset	Idle
Bit 4: Reset Slave DSP2 If this bit is set, Slave DSP2 will be reset.			Reset	Idle
Bit 5: Reset Slave DSP3 If this bit is set, Slave DSP1 will be reset.			Reset	Idle
Bit 6: Reset ROD If this bit is set, all DSP and FPGA chips on the ROD will be reset.			Reset	Idle

Description	Address	Access	Width
PRM: Flash Control Register	{BA}C0000C	RW	3
All bits in the Register are Self-Clearing		Bit Value	
		1	0
Bit 0: Read Flash Direct VME This bit is set to perform a read from the Flash Memory. The data from one read cycle will be stored in the Flash Data Register until the next read operation is performed. The address location to be read must first be loaded into the FLASH Address Register. The data can be read from the FLASH Data Read Register when the cycle is complete.		Read	NOP
Bit 1: Write Flash Direct VME This bit is set to perform a write from the Flash Memory. The address location and data to be written must first be loaded into the FLASH Address and Write Data Register. This bit is used when erasing sectors of the Flash Memory. This write mode allows the user complete control of the write cycle because the PRM does not add any of the unlock commands when this bit is set.		Write	NOP
Bit 2: Write Flash PRM Control This bit is set to perform a write to the Flash Memory with the data stored in the Flash Data Register. This write allows the PRM to control the unlock algorithm of the Flash. This operation requires the correct destination address and data are written to their respective locations before it is set. The address location and data to be written must first be loaded into the FLASH Address and Write Data Register.		Write	NOP

Description	Address	Access	Width
PRM: Flash Address and Write Data Register	{BA}C00010	RW	32
This register is used to transfer the FLASH Address location and write data with one VME access. The Address data is located in bits LD(23:0), and the Write Data is located in bits LD(31:24). A read cycle only requires a valid address; the PRM ignores the data field in this case.		Bit Value	
Bits[31:24]: FLASH Memory Write Data		Value	
Bits[23: 0]: FLASH Memory Address Data		Value	

Address Location Map Table: RevE and RevF ROD FLASH Memory

FLASH 0	
Begin	End
0xE00000	0xFFFFFF

Address Location Map Table: RevE and RevF ROD FPGA Configuration Data

ROD Controller		Formatters		EFB		Router	
Begin	End	Begin	End	Begin	End	Begin	End
E00000	E78E63	E80000	EF8E6B	F00000	F52327	F80000	FD2327

PRM: ROD Miscellaneous Status Register		{BA}C00014	R	26
			Bit Value	
			1	0
Bit 0: ROD Clock Select Status			Internal	BOC
Bit 1: ROD Clock DLL Locked			DLL Locked	Fail
Bit 2: VME Clock DLL Locked			DLL Locked	Fail
Bit 3: ROD Busy			ROD Busy	OK
Bit 4: ROD Type In			Pixel	SCT
Bit 5: Formatter Type In(0) (Pixel Only)			Value	Mode
			00	40MHz
			01	80MHz
Bit 6: Formatter Type In(1) (Pixel Only)			10	160MHz
			11	40MHz (HW)
Bit 7: Slink LFF (Latching, Self Clearing)			Error	OK
Bit 8: Slink LDOWN			Error	OK
Bit 9: DSP0 Detect In			DSP0 Present	DSP0 Out
Bit 10: DSP1 Detect In			DSP1 Present	DSP1 Out
Bit 11: DSP2 Detect In			DSP2 Present	DSP2 Out
Bit 12: DSP3 Detect In			DSP3 Present	DSP3 Out
Bit 13: MDSP HRDY_N			HPI Busy	HPI Ready
Bit 14: NOT USED				
Bit 15: Configuration Done				
Bits[19:16]: IRQ ID				
Bits[25:20]: VME AM Code				

Description		Address	Access	Width
PRM: VME Time Out Value Register		{BA}C00018	RW	32
This register allows the user to set the VME timeout period for the ROD. After reset, the value is 1.4ms (0x1CB90). During a VME access to the MDSP, if HRDYn does not acknowledge the transaction within the VME timeout limit, the ROD will issue a BERRn and the VME slave state machine will return to the idle state.			Bit Value	
Bits[31:0]: VME Time out Value			Value	

Description		Address	Access	Width
PRM: ROD Busy Histogram Control Register		{BA}C0001C	RW	1
This register is used to enable or disable the ROD Busy Histogram engine. After reset, histogramming is disabled. For triggered operation, set bit 1 before enabling the Histogram engine.			Bit Value	
Bit 0: ROD Busy Histogram Control			Enable	Disable
Bit 1: ROD Busy Histogram Triggered Start Enabled			Trigger	Auto

Description		Address	Access	Width
PRM: FPGA Configuration Status Register		{BA}C00020	R	6
			Bit Value	
			1	0
Bit 0: ROD Controller FPGA Configuration Done			Done	Fail
Bit 1: Formatter A Configuration Done			Done	Fail
Bit 2: Formatter B Configuration Done			Done	Fail
Bit 3: EFB Configuration Done			Done	Fail
Bit 4: Router Configuration Done			Done	Fail
Bit 5: Configuration Active If this bit is set, the PRM is in Configuration mode. While this bit is true, the VME is not able to access the FLASH Memory.			Configure Mode	Normal

Description		Address	Access	Width
PRM: FPGA Reset Status Register		{BA}C00024	R	6
			Bit Value	
			1	0
Bit 0: ROD Controller FPGA Reset Control Signal State			OK	Reset
Bit 1: Formatter A Reset Control Signal State			OK	Reset
Bit 2: Formatter B Reset Control Signal State			OK	Reset
Bit 3: EFB Reset Control Signal State			OK	Reset
Bit 4: Router Reset Control Signal State			OK	Reset

Description	Address	Access	Width
PRM: DSP Reset Status Register	{BA}C00028	**R**	**6**
All bits in the Register are Self-Clearing	Bit Value		
		1	0
Bit 0: Not Used		OK	Reset
Bit 1: Master DSP Reset Control Signal State		OK	Reset
Bit 2: Slave DSP0 Reset Control Signal State		OK	Reset
Bit 3: Slave DSP1 Reset Control Signal State		OK	Reset
Bit 4: Slave DSP2 Reset Control Signal State		OK	Reset
Bit 5: Slave DSP3 Reset Control Signal State		OK	Reset

Description	Address	Access	Width
PRM: FPGA INIT_N Status Register	{BA}C0002C	**R**	**6**
Indicates the state of the FPGA INIT bit. If the bit is true, and the DONE is true, then the FPGA chips are operating.	Bit Value		
		1	0
Bit 0: ROD Controller FPGA INIT_N Control Signal State		OK	Clear
Bit 1: Formatter A INIT_N Control Signal State		OK	Clear
Bit 2: Formatter B INIT_N Control Signal State		OK	Clear
Bit 3: EFB INIT_N Control Signal State		OK	Clear
Bit 4: Router INIT_N Control Signal State		OK	Clear

Description	Address	Access	Width
PRM: Flash Status Register	{BA}C00030	**R**	**3**
All bits in the Register are Self-Clearing	Bit Value		
		1	0
Bit 0: Read Flash Direct VME Status		Read	NOP
Bit 1: Write Flash Direct VME Status		Write	NOP
Bit 2: Write Flash PRM Control Status		Write	NOP

Description	Address	Access	Width
PRM: FPGA Configuration Halt Status Register	{BA}C00034	**R**	**6**
Indicates the state of the FPGA configuration. If the bit is true, the FPGA configuration failed.	Bit Value		
		1	0
Bit 0: ROD Controller FPGA Configuration Halt Signal State		Fail	OK
Bit 1: Formatter A Configuration Halt Signal State		Fail	OK
Bit 2: Formatter B Configuration Halt Signal State		Fail	OK
Bit 3: EFB Configuration Halt Signal State		Fail	OK
Bit 4: Router Configuration Halt Signal State		Fail	OK

Description	Address	Access	Width
PRM: ROD Serial Number	{BA}C00038	**R**	**32**
	Bit Value		
Bits[9: 0]: Serial Number	Value		
Bits[15:12]: FPGA Code Version	Value		
Bits[23:16]: ROD Board Revision	Value		
Bits[31:24]: ROD ID	ADh		

Description	Address	Access	Width
PRM: Flash Data Read Register	{BA}C0003C	**R**	**8**
	Bit Value		
Bits[7:0]: FLASH Memory READ Data	Value		

Description	Address	Access	Width
PRM: ROD Source ID	{BA}C00040	**R**	**32**
	Bit Value		
Bits[7: 0]: Serial Number	Value		
Bits[15: 8]: Sub-detector ID	Value		
Bits[23:16]: Module Type	00h		
Bits[31:24]: Reserved	00h		

Description	Address	Access	Width
PRM: ROD Manufacturer ID	{BA}C00044	R	24
		Bit Value	
Bits[23:0]: LBNL ID		Value	

Description	Address	Access	Width
PRM: ROD Board ID	{BA}C00048	R	32
		Bit Value	
Bits[31:0]: ROD Board ID		Value	

Description	Address	Access	Width
PRM: ROD Revision ID	{BA}C0004C	R	32
		Bit Value	
Bits[3: 0]: NOT USED		0x0	
Bits[7: 4]: ROD Revision ID		Value	
Bits[17: 8]: ROD Serial Number		Value	
Bits[31:24]: Code Version		Value	

Description	Address	Access	Width
PRM: Diagnostic Register	{BA}C00050	R	32
		Bit Value	
Bits[31:0]: Diagnostic Bits		Value	

Description	Address	Access	Width
PRM: Diagnostic Register	{BA}C00054	R	32
		Bit Value	
Bits[31:0]: Diagnostic Bits		Value	

Description	Address	Access	Width
PRM: Diagnostic Register	{BA}C00058	R	32
		Bit Value	
Bits[31:0]: Diagnostic Bits		Value	

Description	Address	Access	Width
PRM: Current ROD Busy Histogram Address	{BA}C0005C	R	16
Bits [9:0] indicate the data location, bits [15:10] indicate the number of times the address counter has wrapped around 0.		Bit Value	
Bits[15:0]: ROD Busy Histogram Address Status		Value	

Description	Address	Access	Width
PRM: 1024x32 ROD Busy Histogram Memory	{BA}C01000	R	32
Address Range 0xC01000 to 0xC01FFC (4kB memory space). Fast Access memory block			

MDSP Boot ROM Write/Control Information

Part Number:
SST39VF040-90-4C-NH, 512Kx8 Flash Memory, 90ns, 100K min cycle, 32-pin PLCC

Device Operation
Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Read
The Read operation of the SST39VF040 device is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high.
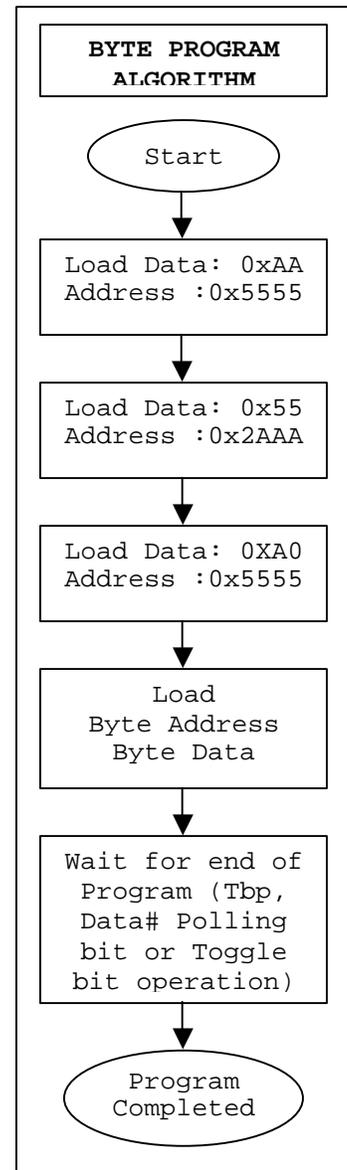
Write Operation Status Detection
The SST39VF040 device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Pro-gram or Erase operation. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result (i.e., valid data may appear to conflict with either DQ7 or DQ6). In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.
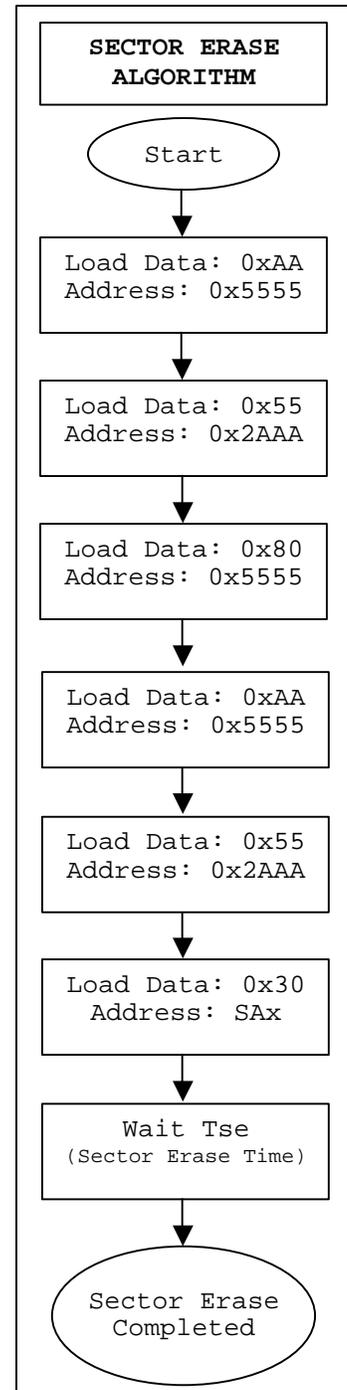
Byte-Program Operation

The SST39VF040 are programmed on a byte-by-byte basis. Before programming, the sector where the byte exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 20 µs. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

```
┌─────────────────────────┐
│   BYTE PROGRAM          │
│   ALGORITHM             │
├─────────────────────────┤
│        ( Start )        │
│           │             │
│  ┌──────────────────┐   │
│  │ Load Data: 0xAA  │   │
│  │ Address :0x5555  │   │
│  └──────────────────┘   │
│           │             │
│  ┌──────────────────┐   │
│  │ Load Data: 0x55  │   │
│  │ Address :0x2AAA  │   │
│  └──────────────────┘   │
│           │             │
│  ┌──────────────────┐   │
│  │ Load Data: 0XA0  │   │
│  │ Address :0x5555  │   │
│  └──────────────────┘   │
│           │             │
│  ┌──────────────────┐   │
│  │      Load        │   │
│  │  Byte Address    │   │
│  │   Byte Data      │   │
│  └──────────────────┘   │
│           │             │
│  ┌──────────────────┐   │
│  │ Wait for end of  │   │
│  │ Program (Tbp,    │   │
│  │ Data# Polling    │   │
│  │ bit or Toggle    │   │
│  │ bit operation)   │   │
│  └──────────────────┘   │
│           │             │
│      ( Program          │
│        Completed )      │
└─────────────────────────┘
```
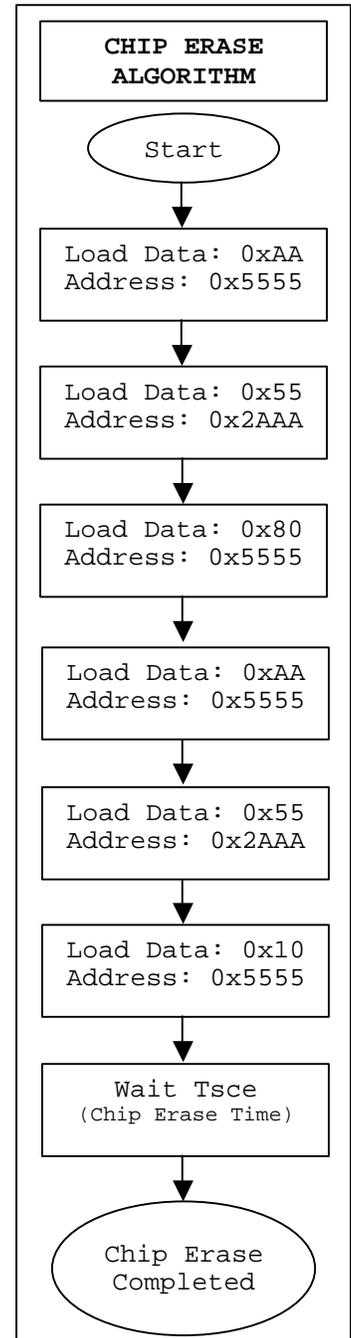
Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. Any commands written during the Sector-Erase operation will be ignored.

```
┌─────────────────────────┐
│    SECTOR ERASE         │
│     ALGORITHM           │
└─────────────────────────┘

        ( Start )
            │
            ▼
┌─────────────────────────┐
│ Load Data: 0xAA         │
│ Address: 0x5555         │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│ Load Data: 0x55         │
│ Address: 0x2AAA         │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│ Load Data: 0x80         │
│ Address: 0x5555         │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│ Load Data: 0xAA         │
│ Address: 0x5555         │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│ Load Data: 0x55         │
│ Address: 0x2AAA         │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│ Load Data: 0x30         │
│  Address: SAx           │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│      Wait Tse           │
│ (Sector Erase Time)     │
└─────────────────────────┘
            │
            ▼
      ( Sector Erase
         Completed )
```

Chip-Erase Operation

The SST39VF040 device provides a Chip-Erase operation, which allows the user to erase the entire memory array to the '1's state. This is useful when the entire device must be quickly erased. The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. Any commands written during the Chip-Erase operation will be ignored.

```
┌─────────────────────────┐
│  ┌───────────────────┐  │
│  │   CHIP ERASE      │  │
│  │   ALGORITHM       │  │
│  └───────────────────┘  │
│                         │
│      (  Start  )        │
│          │              │
│          ▼              │
│  ┌───────────────────┐  │
│  │ Load Data: 0xAA   │  │
│  │ Address: 0x5555   │  │
│  └───────────────────┘  │
│          │              │
│          ▼              │
│  ┌───────────────────┐  │
│  │ Load Data: 0x55   │  │
│  │ Address: 0x2AAA   │  │
│  └───────────────────┘  │
│          │              │
│          ▼              │
│  ┌───────────────────┐  │
│  │ Load Data: 0x80   │  │
│  │ Address: 0x5555   │  │
│  └───────────────────┘  │
│          │              │
│          ▼              │
│  ┌───────────────────┐  │
│  │ Load Data: 0xAA   │  │
│  │ Address: 0x5555   │  │
│  └───────────────────┘  │
│          │              │
│          ▼              │
│  ┌───────────────────┐  │
│  │ Load Data: 0x55   │  │
│  │ Address: 0x2AAA   │  │
│  └───────────────────┘  │
│          │              │
│          ▼              │
│  ┌───────────────────┐  │
│  │ Load Data: 0x10   │  │
│  │ Address: 0x5555   │  │
│  └───────────────────┘  │
│          │              │
│          ▼              │
│  ┌───────────────────┐  │
│  │    Wait Tsce      │  │
│  │ (Chip Erase Time) │  │
│  └───────────────────┘  │
│          │              │
│          ▼              │
│    (  Chip Erase   )    │
│    (  Completed    )    │
└─────────────────────────┘
```

Data# Polling (DQ7)

When the SST39VF040 is in the internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce true data. Note that even though DQ7 may have valid data immediately following completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1μs. During internal Erase operation, any attempt to read DQ7 will produce a "0". Once the internal Erase operation is completed, DQ7 will produce a "1". The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse.

Toggle Bit (DQ6)

During the internal Program or Erase operation, any consecutive attempts to read DQ6 will produce alternating '0's and '1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse.
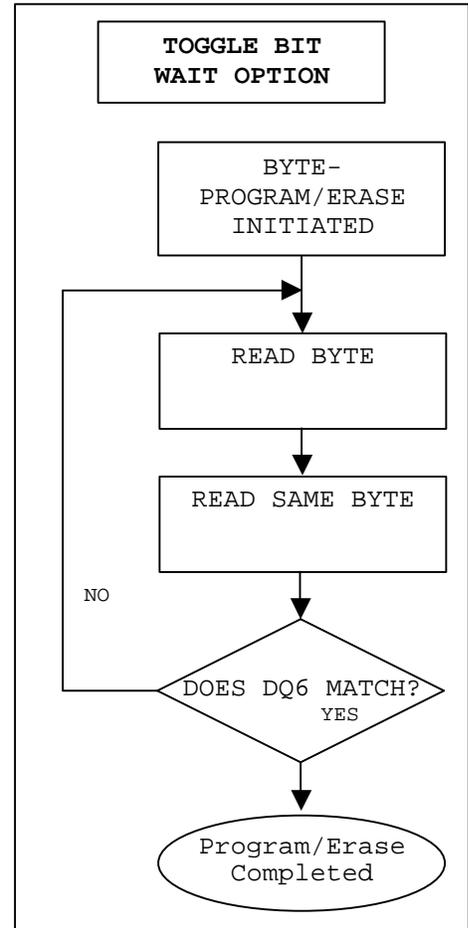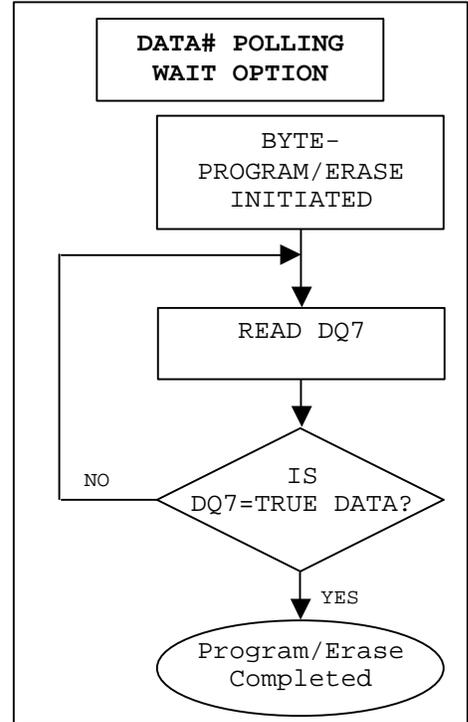
Software Data Protection (SDP)
The SST39040 provide the JEDEC approved Software Data Protection scheme for all data alteration operation, i.e., Pro-gram and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down.
Any Erase operation requires the inclusion of six-byte load sequence. These devices are shipped with the Software Data Protection permanently enabled. During SDP command sequence, invalid commands will abort the device to read mode, within
TRC.

Product Identification
The Product Identification mode identifies the devices as the SST39VF040 and manufacturer as SST. This mode may be accessed by software operations. Users may use the Software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket.
Manufacturer's ID: 0000H BFH
Device ID: SST39LF/VF040 0001H D7H

Product Identification Mode Exit/Reset
In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read operation. Please note that the Software ID Exit command is ignored during an internal Program or Erase operation.

TABLE 1: FLASH SOFTWARE COMMAND SEQUENCE

Flash Software Command Sequence												
Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	ADDR(1)	DATA	ADDR(1)	DATA	ADDR(1)	DATA	ADDR(1)	DATA	ADDR(1)	DATA	ADDR(1)	DATA
Byte-Program	0x5555	0xAA	0X2AAA	0X55	0X5555	0XA0	BA(2)	DATA				
Sector Erase	0x5555	0xAA	0X2AAA	0X55	0X5555	0X80	0x5555	0xAA	0X2AAA	0X55	SAx(3)	0X30
Chip Erase	0x5555	0xAA	0X2AAA	0X55	0X5555	0X80	0x5555	0xAA	0X2AAA	0X55	0X5555	0X10
Software ID Entry (4,5)	0x5555	0xAA	0X2AAA	0X55	0X5555	0X90						
Software ID Exit (6)	0xXX	0XF0										
Software ID Exit (6)	0x5555	0xAA	0X2AAA	0X55	0X5555	0XF0						

1. Address format A14-A0 (Hex),
   Addresses AMS-A15 can be VIL or VIH, but no other value, for the Command sequence.
   AMS = Most significant address
   AMS = A15 for SST39LF/VF512, A16 for SST39LF/VF010, A17 for SST39LF/VF020, and A18 for SST39LF/VF040
2. BA = Program Byte address
3. SAx for Sector-Erase; uses AMS-A12 address lines
4. The device does not remain in Software Product ID mode if powered down.
5. With AMS-A1 = 0; SST Manufacturer's ID = BFH, is read with A0 = 0,
   SST39LF/VF040 Device ID = D7H, is read with A0 = 1
6. Both Software ID Exit operations are equivalent.

APPENDIX B: ROD VME Access Registers

FPGA Configuration Write/Control Information

Part Number:
AMD29LV017D, 2048Kx8 Flash Memory, 90ns, 10K min cycle, 52-pin TTSOP

Device Operation
Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Read
The Read operation of the AMD29LV017D device is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high.