

# ROD Operations Manual

## APPENDIX A:

### ROD and BOC FPGA Register Definitions

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# APPENDIX A: ROD and BOC FPGA Register Definitions

## 1 Supported FPGA Versions

FPGA Versions	
ROD Controller FPGA (RCF)	V35F
Formatter FPGA (FMT) [S = SCT / P = Pixel]	S34F/P3CF
Event Fragment Builder FPGA (EFB)	V2EF
Router FPGA (RTR)	V29F

## 2 ROD Memory Location Definitions

Description	Address Range	
<b>Formatter FPGA 0 Registers: Links 0 to 11</b> Configuration, Status, Readout Timeout Limit, Data Overflow Limit, Header Trailer Limit, and ROD Busy Limit	00400000	00400090
<b>Formatter FPGA 1 Registers: Links 12 to 23</b> Configuration, Status, Readout Timeout Limit, Data Overflow Limit, Header Trailer Limit, and ROD Busy Limit	00400400	00400490
<b>Formatter FPGA 2 Registers: Links 24 to 35</b> Configuration, Status, Readout Timeout Limit, Data Overflow Limit, Header Trailer Limit, and ROD Busy Limit	00400800	00400890
<b>Formatter FPGA 3 Registers: Links 36 to 47</b> Configuration, Status, Readout Timeout Limit, Data Overflow Limit, Header Trailer Limit, and ROD Busy Limit	00400C00	00400C90
<b>Formatter FPGA 4 Registers: Links 48 to 59</b> Configuration, Status, Readout Timeout Limit, Data Overflow Limit, Header Trailer Limit, and ROD Busy Limit	00401000	00401090
<b>Formatter FPGA 5 Registers: Links 60 to 71</b> Configuration, Status, Readout Timeout Limit, Data Overflow Limit, Header Trailer Limit, and ROD Busy Limit	00401400	00401490
<b>Formatter FPGA 6 Registers: Links 72 to 83</b> Configuration, Status, Readout Timeout Limit, Data Overflow Limit, Header Trailer Limit, and ROD Busy Limit	00401800	00401890
<b>Formatter FPGA 7 Registers: Links 84 to 95</b> Configuration, Status, Readout Timeout Limit, Data Overflow Limit, Header Trailer Limit, and ROD Busy Limit	00401C00	00401C90
<b>Event Fragment Builder FPGA Registers</b> Error Mask, Format Version, Source ID, Play Empty Events, Mask BCID Error Check, Diagnostic, Status, Play One Event, FIFO Status Flags, Reset EVENTMEM, W: EVENTMEM A, EVENTMEM B, EVENTMEM C	00402000	004022FC
<b>Router FPGA Registers</b> S-Link Control and Status, Event Trapping Control and Status	00402400	004025FC
<b>ROD Controller FPGA Registers</b> Function Control, Status, ROD Mode, Diagnostic, Calibration Commands, FE Command Mask, Counter Values, Interrupts, and FE Occupancy Count Control	00404400	004044FC
<b>Front End Chip Occupancy Counter Registers</b>	00404500	0040452C
<b>FE Command Mask Look-up Table</b> 8 sets of Masks, 64 Locations	00404600	004046FC
<b>EFB Dynamic Mask Registers</b> Default and Corrective ROD types	00404700	00404780
<b>Formatter Dynamic Mode Bit Look-up Table</b> 8 sets of Masks, 256 Locations	00404800	00404BFC
<b>Diagnostic Memory FIFO Registers</b> R/W: INMEM A, INMEM B R: EVENTMEM A, EVENTMEM B, EVENTMEM C	00406000	00406150
<b>BOC Setup Registers</b>	00408000	00408FFC
<b>Slave DSP0 HPI Registers</b> HPIC, HPIA, HPID++, and HPID	00780000	0078000C
<b>Slave DSP1 HPI Registers</b> HPIC, HPIA, HPID++, and HPID	007A0000	007A000C
<b>Slave DSP2 HPI Registers</b> HPIC, HPIA, HPID++, and HPID	007C0000	007C000C
<b>Slave DSP3 HPI Registers</b> HPIC, HPIA, HPID++, and HPID	007E0000	007E000C

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## 3 ROD Formatter FPGA Registers

### 3.1 Link Configuration Registers

Description	REG ID	Address	Access	Width
<b>Link Enable Register: FMT_LINK_EN(fmt)</b> fmt = formatter number			RW	12
<b>Formatter Chip 0</b>	0	00400000		
<b>Formatter Chip 1</b>	1	00400400		
<b>Formatter Chip 2</b>	2	00400800		
<b>Formatter Chip 3</b>	3	00400C00		
<b>Formatter Chip 4</b>	4	00401000		
<b>Formatter Chip 5</b>	5	00401400		
<b>Formatter Chip 6</b>	6	00401800		
<b>Formatter Chip 7</b>	7	00401C00		
Each bit enables the serial data decoder and data FIFO for a specific link or module input to the Formatter. If the link or module is off, the internal data FIFO will be turned off. On the Pixel ROD, the unused bits are masked. The default register value is 0.			<b>Bit Value</b>	
			1	0
<b>Bit 0:</b> Enable SCT Link 0 (40 MHz) / Pixel Module 0 (40/80/160 MHz)			Enable	Off
<b>Bit 1:</b> Enable SCT Link 1 (40 MHz) / Pixel Module 1 (40/80 MHz only)			Enable	Off
<b>Bit 2:</b> Enable SCT Link 2 (40 MHz) / Pixel Module 2 (40 MHz only)			Enable	Off
<b>Bit 3:</b> Enable SCT Link 3 (40 MHz) / Pixel Module 3 (40 MHz only)			Enable	Off
<b>Bit 4:</b> Enable SCT Link 4			Enable	Off
<b>Bit 5:</b> Enable SCT Link 5			Enable	Off
<b>Bit 6:</b> Enable SCT Link 6			Enable	Off
<b>Bit 7:</b> Enable SCT Link 7			Enable	Off
<b>Bit 8:</b> Enable SCT Link 8			Enable	Off
<b>Bit 9:</b> Enable SCT Link 9			Enable	Off
<b>Bit 10:</b> Enable SCT Link 10			Enable	Off
<b>Bit 11:</b> Enable SCT Link 11			Enable	Off

Description	REG ID	Address	Access	Width
<b>Expanded Mode Register: FMT_EXP_MODE_EN(fmt) **SCT only**</b> fmt = formatter number			RW	12
<b>Formatter Chip 0</b>	8	00400004		
<b>Formatter Chip 1</b>	9	00400404		
<b>Formatter Chip 2</b>	A	00400804		
<b>Formatter Chip 3</b>	B	00400C04		
<b>Formatter Chip 4</b>	C	00401004		
<b>Formatter Chip 5</b>	D	00401404		
<b>Formatter Chip 6</b>	E	00401804		
<b>Formatter Chip 7</b>	F	00401C04		
<b>Expanded SCT Data Mode</b> If this bit is set to value 1, the serial input data will be parsed in Expanded Data format. If this bit is set to value 0, the serial input data will be parsed in Condensed Data format. The default register value is 0.			<b>Bit Value</b>	
<b>The SCT data formats are as follows:</b> Condensed 1 hit condensed - 1FFFFCCCCCxfx0 2 hits condensed - 1FFFFCCCCCsfx1  Expanded 1st hit cluster - 1FFFFCCCCC0DDD 1 hit cluster - 1xxxxxxx0xxx1DDD 2 hit cluster - 1xxxxxxx1DDD1DDD  x = do not care (The ROD fills these with 0's) C = cluster base address D = 3 bit hit data F = FE number f = error in condensed mode data, 1st hit s = error in condensed mode data, 2nd hit			1	0
<b>Bit 0:</b> Link 0			Expand	Condense
<b>Bit 1:</b> Link 1			Expand	Condense
<b>Bit 2:</b> Link 2			Expand	Condense
<b>Bit 3:</b> Link 3			Expand	Condense
<b>Bit 4:</b> Link 4			Expand	Condense
<b>Bit 5:</b> Link 5			Expand	Condense
<b>Bit 6:</b> Link 6			Expand	Condense
<b>Bit 7:</b> Link 7			Expand	Condense
<b>Bit 8:</b> Link 8			Expand	Condense
<b>Bit 9:</b> Link 9			Expand	Condense
<b>Bit 10:</b> Link 10			Expand	Condense
<b>Bit 11:</b> Link 11			Expand	Condense

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>Configuration Mode Register: FMT_CONFIG_MODE_EN(fmt)</b> fmt = formatter number				
<b>Formatter Chip 0</b>	10	00400008	RW	12
<b>Formatter Chip 1</b>	11	00400408		
<b>Formatter Chip 2</b>	12	00400808		
<b>Formatter Chip 3</b>	13	00400C08		
<b>Formatter Chip 4</b>	14	00401008		
<b>Formatter Chip 5</b>	15	00401408		
<b>Formatter Chip 6</b>	16	00401808		
<b>Formatter Chip 7</b>	17	00401C08		
<b>Configuration Mode (Raw Data Format)</b> If this bit is set to value 1, the Formatter will parse the serial input stream in raw format. If this bit is set to value 0, other registers determine the decoding format. The default register value is 0.  <b>The SCT raw data format is as follows:</b> Data Word 011nnnxxDDDDDDDD (n=(number of bits)+1, D=data) <b>The Pixel raw data format is as follows:</b> Link Header 001H11001101DDDDDDDDDDDDDDDDDDDDDDDDDDDD >> (D=data, H=Header Error) Data Word 0110DDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDD >> (D=data)			<b>Bit Value</b>	
			1	0
<b>Bit 0:</b> Link 0			Raw	OFF
<b>Bit 1:</b> Link 1			Raw	OFF
<b>Bit 2:</b> Link 2			Raw	OFF
<b>Bit 3:</b> Link 3			Raw	OFF
<b>Bit 4:</b> Link 4			Raw	OFF
<b>Bit 5:</b> Link 5			Raw	OFF
<b>Bit 6:</b> Link 6			Raw	OFF
<b>Bit 7:</b> Link 7			Raw	OFF
<b>Bit 8:</b> Link 8			Raw	OFF
<b>Bit 9:</b> Link 9			Raw	OFF
<b>Bit 10:</b> Link 10			Raw	OFF
<b>Bit 11:</b> Link 11			Raw	OFF

Description	REG ID	Address	Access	Width
<b>Edge Detect Mode Register: FMT_EDGE_MODE_EN(fmt)</b> fmt = formatter number				
<b>Formatter Chip 0</b>	18	0040000C	RW	12
<b>Formatter Chip 1</b>	19	0040040C		
<b>Formatter Chip 2</b>	1A	0040080C		
<b>Formatter Chip 3</b>	1B	00400C0C		
<b>Formatter Chip 4</b>	1C	0040100C		
<b>Formatter Chip 5</b>	1D	0040140C		
<b>Formatter Chip 6</b>	1E	0040180C		
<b>Formatter Chip 7</b>	1F	00401C0C		
<b>Edge Detect Mode ** SCT ONLY **</b> Valid in Condensed Data Mode only. If set, the Formatter will check hit data for Edge Mode or Level Mode format. If an invalid hit pattern is detected, an error flag will be inserted into the condensed hit data word and reported by the EFB. After a reset, this register defaults to all links in Level Detect Mode (all bits 0).  <b>Edge Detect Hit Pattern : 01X</b> <b>Level Detect Hit Pattern: X1X</b>			<b>Bit Value</b>	
			1	0
<b>Bit 0:</b> Link 0			Edge	Level
<b>Bit 1:</b> Link 1			Edge	Level
<b>Bit 2:</b> Link 2			Edge	Level
<b>Bit 3:</b> Link 3			Edge	Level
<b>Bit 4:</b> Link 4			Edge	Level
<b>Bit 5:</b> Link 5			Edge	Level
<b>Bit 6:</b> Link 6			Edge	Level
<b>Bit 7:</b> Link 7			Edge	Level
<b>Bit 8:</b> Link 8			Edge	Level
<b>Bit 9:</b> Link 9			Edge	Level
<b>Bit 10:</b> Link 10			Edge	Level
<b>Bit 11:</b> Link 11			Edge	Level

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## 3.2 Error Limit Setup Registers

Description	REG ID	Address	Access	Width
<b>Time Out Limit Register: FMT_READOUT_TIMEOUT(fmt)</b>				
Formatter Chip 0	20	00400010	RW	8 (SCT) 32 (PXL)
Formatter Chip 1	21	00400410		
Formatter Chip 2	22	00400810		
Formatter Chip 3	23	00400C10		
Formatter Chip 4	24	00401010		
Formatter Chip 5	25	00401410		
Formatter Chip 6	26	00401810		
Formatter Chip 7	27	00401C10		
<b>Token to Readout Timeout Limit Reg:</b> The Token to Readout Limit is a user configurable value that is used to determine the time that the ROD allows for a module to transmit event data following a L1 Trigger. If a module does not respond with data before the counter in the Formatter reaches the timeout limit, a time out error event is inserted into the event fragment and the token is passed to the next link. SCT: 800ns increments: The default value at reset is 0xFFh (204.8 us). PXL: 25ns increments: The default value at reset is 0x800h (51.2 us).			Bit Value	Value

Description	REG ID	Address	Access	Width
<b>Data Overflow Limit Register: FMT_DATA_OVERFLOW_LIMIT(fmt)</b>				
Formatter Chip 0	28	00400014	RW	12
Formatter Chip 1	29	00400414		
Formatter Chip 2	2A	00400814		
Formatter Chip 3	2B	00400C14		
Formatter Chip 4	2C	00401014		
Formatter Chip 5	2D	00401414		
Formatter Chip 6	2E	00401814		
Formatter Chip 7	2F	00401C14		
<b>Data Overflow Limit Value:</b> This value set the maximum number of words played out of the Output FIFO before the ROD determines that a link has received too much data for 1 Event. At reset, the default value is set to 0x200h.			Bit Value	Value

Description	REG ID	Address	Access	Width
<b>Header Trailer Limit Reg: FMT_HEADER_TRAILER_LIMIT(fmt)</b>				
Formatter Chip 0	30	00400018	RW	9 (SCT) 11 (PXL)
Formatter Chip 1	31	00400418		
Formatter Chip 2	32	00400818		
Formatter Chip 3	33	00400C18		
Formatter Chip 4	34	00401018		
Formatter Chip 5	35	00401418		
Formatter Chip 6	36	00401818		
Formatter Chip 7	37	00401C18		
<b>Header Trailer Limit (HTL):</b> This value in the HTL register sets the link FIFO Almost Full word count threshold. When HTL is true, the Formatter only writes Headers and Trailers to the Link FIFO and drops all hit data. At reset, the default value for the SCT Formatter is set to 0x1C0h and for the Pixel Formatter the default value is set to 0x700.			Bit Value	Value

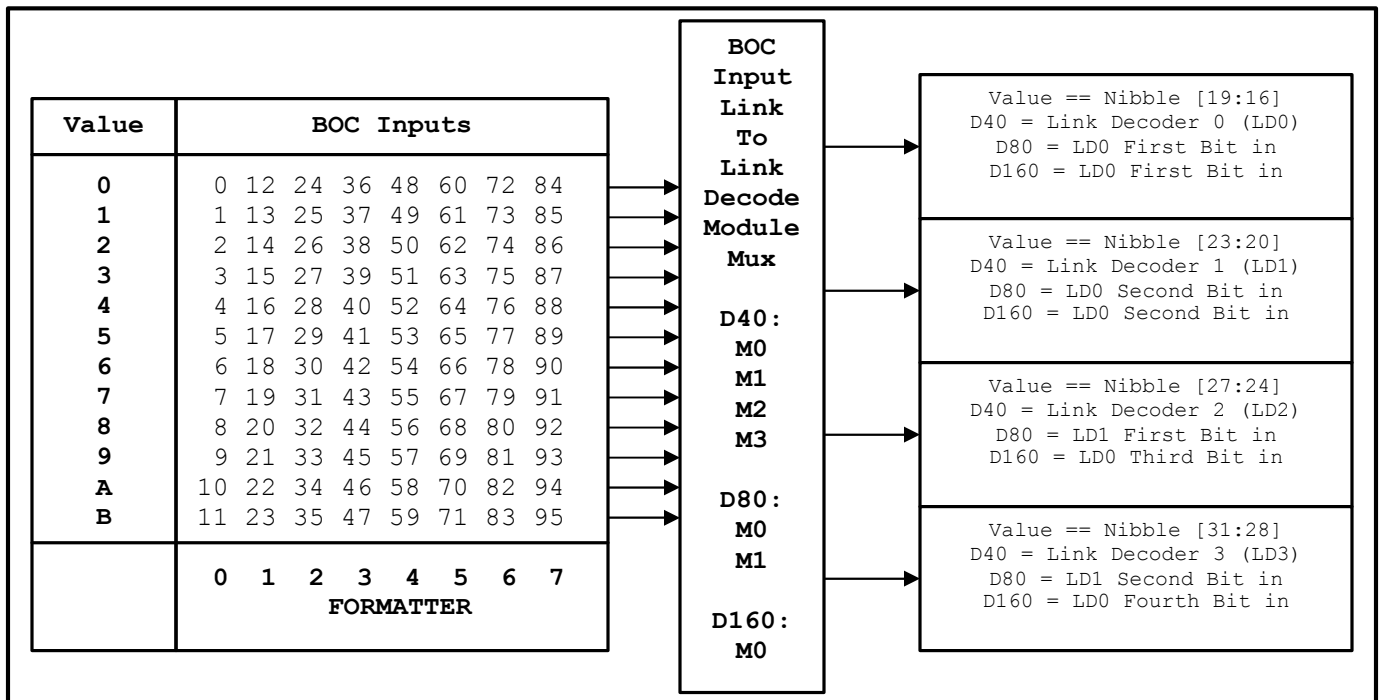
Description	REG ID	Address	Access	Width
<b>ROD Busy Limit Register: FMT_ROD_BUSY_LIMIT(fmt)</b>				
Formatter Chip 0	38	0040001C	RW	9 (SCT) 11 (PXL)
Formatter Chip 1	39	0040041C		
Formatter Chip 2	3A	0040081C		
Formatter Chip 3	3B	00400C1C		
Formatter Chip 4	3C	0040101C		
Formatter Chip 5	3D	0040141C		
Formatter Chip 6	3E	0040181C		
Formatter Chip 7	3F	00401C1C		
<b>ROD Busy Limit (RBL):</b> The value in the RBL register sets the input link FIFO word count threshold, that, when exceeded, will assert and send ROD BUSY to the trigger system. Because the threshold is configurable, a link that has exceeded ROD BUSY limit may still have a room for more data, but recovery from ROD Busy limit usually requires reset of the link in error. At reset, the default RBL value for the SCT Formatter is 0x1F0h and for the Pixel Formatter the default value is 0x780h.			Bit Value	Value

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## 3.3 Pixel Trigger Number of Accepts Register

Description	REG ID	Address	Access	Width
<b>Pixel Formatter: Number of L1 Accepts</b> FMT_PXL_LINK_L1A_CNT(fmt)		00400020	RW	16
Formatter Chip 0	40	00400020		
Formatter Chip 1	41	00400420		
Formatter Chip 2	42	00400820		
Formatter Chip 3	43	00400C20		
Formatter Chip 4	44	00401020		
Formatter Chip 5	45	00401420		
Formatter Chip 6	46	00401820		
Formatter Chip 7	47	00401C20		
The Pixel MCC chip can issue up to 16 L1 Triggers to the FE chips for each L1 trigger sent by the ROD. This register sets a counter value in the Formatter readout state machine that allows all of the data from a multi trigger event to be played out with one trigger.			<b>Bit Value</b>	
Bits[ 3: 0]: Input Module 0			Value	
Bits[ 7: 4]: Input Module 1			Value	
Bits[11: 8]: Input Module 2			Value	
Bits[15:12]: Input Module 3			Value	

Description	REG ID	Address	Access	Width
<b>Pixel Formatter: Software Decode Type Select</b> FMT_PXL_BANDWIDTH(fmt) - Link Input Map		00400024	RW	16
Formatter Chip 0	48	00400024		
Formatter Chip 1	49	00400424		
Formatter Chip 2	4A	00400824		
Formatter Chip 3	4B	00400C24		
Formatter Chip 4	4C	00401024		
Formatter Chip 5	4D	00401424		
Formatter Chip 6	4E	00401824		
Formatter Chip 7	4F	00401C24		
If the Decode Select Jumpers are not installed, then the value in bits 0 and 1 of this register selects the input decode type. Pixel Decoder Type == "00" - Single Link 40MHz Decoder (default) "01" - Dual Link 80MHz input "10" - Quad Link 160MHz input See diagram below for information on Link Map values. The Formatter does not protect against incorrect link map values.			<b>Bit Value</b>	
Bits[ 1: 0]: Decode Select Value			Value	
Bits[19:16]: Module 0 - Data Input 0 Link Map (0 to 11) / DTO 2 Rising Edge			Value	
Bits[23:20]: Module 1 - Data Input 1 Link Map (0 to 11) / DTO 2 Falling Edge			Value	
Bits[27:24]: Module 2 - Data Input 2 Link Map (0 to 11) / DTO Rising Edge			Value	
Bits[31:28]: Module 3 - Data Input 3 Link Map (0 to 11) / DTO Falling Edge			Value	





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### 3.4 Diagnostic Control Register

Description	REG ID	Address	Access	Width
<b>Formatter L1A Counter Register:</b>				
Formatter Chip 0		00400030	R	24
Formatter Chip 1		00400430		
Formatter Chip 2		00400830		
Formatter Chip 3		00400C30		
Formatter Chip 4		00401030		
Formatter Chip 5		00401430		
Formatter Chip 6		00401830		
Formatter Chip 7		00401C30		
This register keeps track of all L1A triggers that are sent to the Formatter. It is cleared when the Formatter receives an ECR command			Bit Value	
Bits [23:0] : L1A Count			Value	
			L1A Count	

Description	REG ID	Address	Access	Width
<b>Formatter BCR and ECR Counter Register:</b>				
Formatter Chip 0		00400034	R	32
Formatter Chip 1		00400434		
Formatter Chip 2		00400834		
Formatter Chip 3		00400C34		
Formatter Chip 4		00401034		
Formatter Chip 5		00401434		
Formatter Chip 6		00401834		
Formatter Chip 7		00401C34		
This register keeps track of all ECR and BCR commands triggers that are sent to the Formatter. It is cleared when the Formatter is reset.			Bit Value	
Bits [31:16] : BCR Count			Value	
			BCR Count	
Bits [15: 0] : ECR Count			Value	
			ECR Count	

Description	REG ID	Address	Access	Width
<b>Link Data Test Output Mux Register:</b> FMT LINK DATA TEST MUX (fmt)				
Formatter Chip 0	70	00400038	RW	4
Formatter Chip 1	71	00400438		
Formatter Chip 2	72	00400838		
Formatter Chip 3	73	00400C38		
Formatter Chip 4	74	00401038		
Formatter Chip 5	75	00401438		
Formatter Chip 6	76	00401838		
Formatter Chip 7	77	00401C38		
Link Data Test Output Mux: This value selects the input link to send to the EFB output mux that drives the front panel LEMO. The decoding is as follows: 0x0h = Link0, 0x1h = Link1, ... 0xBh = Link11, 0xFh = ROD Busy Monitor			Bit Value	
			Value	

Description	REG ID	Address	Access	Width
<b>Mode Bits Diagnostic, Read Enable: FMT MB DIAG REN (fmt)</b>			RW	8
Formatter Chip 0	78	0040003C		
Formatter Chip 1	79	0040043C		
Formatter Chip 2	7A	0040083C		
Formatter Chip 3	7B	00400C3C		
Formatter Chip 4	7C	0040103C		
Formatter Chip 5	7D	0040143C		
Formatter Chip 6	7E	0040183C		
Formatter Chip 7	7F	00401C3C		
Mode Bits Diagnostic REN: This bit enables the readout of Mode Bits to check that they are being sent to the Formatters correctly. This register is only to be used as board diagnostics.			Bit Value	
Bit 0: Mode Bit FIFO Read Enable			1	0
Bit 1: Enable Link FIFO read command			RD	Idle
Bit 2: Enable Link FIFO write command			RD	Idle
Bit 3: Not Used			WR	Idle
Bits [7:4]: Link FIFO Select			Value	

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### 3.5 Link FIFO Occupancy Count Registers

The value in the Data FIFO Occupancy Count Register indicates the number of data words (headers/hits/trailers) that are currently stored for a specific link or module. The counter increments by 1 for each word stored and decrements by one for each word transmitted on the ROD data path. The number of words in the link/module FIFO is not equal to the number of hits received from the FE modules.

Description	REG ID	Address	Access	Width
Link 0 / Module 0 Data FIFO Occupancy Count Register: FMT_LINK_OCC_COUNT(fmt,lnk)			R	[S]/[P] 9 / 11
Formatter Chip 0	80	00400040		
Formatter Chip 1	8C	00400440		
Formatter Chip 2	98	00400840		
Formatter Chip 3	A4	00400C40		
Formatter Chip 4	B0	00401040		
Formatter Chip 5	BC	00401440		
Formatter Chip 6	C8	00401840		
Formatter Chip 7	D4	00401C40		

Description	REG ID	Address	Access	Width
Link 1 / Module 1 Data FIFO Occupancy Count Register: FMT_LINK_OCC_COUNT(fmt,lnk)			R	[S]/[P] 9 / 11
Formatter Chip 0	81	00400044		
Formatter Chip 1	8D	00400444		
Formatter Chip 2	99	00400844		
Formatter Chip 3	A5	00400C44		
Formatter Chip 4	B1	00401044		
Formatter Chip 5	BD	00401444		
Formatter Chip 6	C9	00401844		
Formatter Chip 7	D5	00401C44		

Description	REG ID	Address	Access	Width
Link 2 / Module 2 Data FIFO Occupancy Count Register: FMT_LINK_OCC_COUNT(fmt,lnk)			R	[S]/[P] 9 / 11
Formatter Chip 0	82	00400048		
Formatter Chip 1	8E	00400448		
Formatter Chip 2	9A	00400848		
Formatter Chip 3	A6	00400C48		
Formatter Chip 4	B2	00401048		
Formatter Chip 5	BE	00401448		
Formatter Chip 6	CA	00401848		
Formatter Chip 7	D6	00401C48		

Description	REG ID	Address	Access	Width
Link 3 / Module 3 Data FIFO Occupancy Count Register: FMT_LINK_OCC_COUNT(fmt,lnk)			R	[S]/[P] 9 / 11
Formatter Chip 0	83	0040004C		
Formatter Chip 1	8F	0040044C		
Formatter Chip 2	9B	0040084C		
Formatter Chip 3	A7	00400C4C		
Formatter Chip 4	B3	0040104C		
Formatter Chip 5	BF	0040144C		
Formatter Chip 6	CB	0040184C		
Formatter Chip 7	D7	00401C4C		

Description	REG ID	Address	Access	Width
Link 4 Data FIFO Occupancy Count Register: FMT_LINK_OCC_COUNT(fmt,lnk)			R	[S]/[P] 9 / 11
Formatter Chip 0	84	00400050		
Formatter Chip 1	90	00400450		
Formatter Chip 2	9C	00400850		
Formatter Chip 3	A8	00400C50		
Formatter Chip 4	B4	00401050		
Formatter Chip 5	C0	00401450		
Formatter Chip 6	CC	00401850		
Formatter Chip 7	D8	00401C50		

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Link 5 Data FIFO Occupancy Count Register: FMT_LINK_OCC_COUNT(fmt,lnk)			R	9
Formatter Chip 0	85	00400054		
Formatter Chip 1	91	00400454		
Formatter Chip 2	9D	00400854		
Formatter Chip 3	A9	00400C54		
Formatter Chip 4	B5	00401054		
Formatter Chip 5	C1	00401454		
Formatter Chip 6	CD	00401854		
Formatter Chip 7	D9	00401C54		

Description	REG ID	Address	Access	Width
Link 6 Data FIFO Occupancy Count Register: FMT_LINK_OCC_COUNT(fmt,lnk)			R	9
Formatter Chip 0	86	00400058		
Formatter Chip 1	92	00400458		
Formatter Chip 2	9E	00400858		
Formatter Chip 3	AA	00400C58		
Formatter Chip 4	B6	00401058		
Formatter Chip 5	C2	00401458		
Formatter Chip 6	CE	00401858		
Formatter Chip 7	DA	00401C58		

Description	REG ID	Address	Access	Width
Link 7 Data FIFO Occupancy Count Register: FMT_LINK_OCC_COUNT(fmt,lnk)			R	9
Formatter Chip 0	87	0040005C		
Formatter Chip 1	93	0040045C		
Formatter Chip 2	9F	0040085C		
Formatter Chip 3	AB	00400C5C		
Formatter Chip 4	B7	0040105C		
Formatter Chip 5	C3	0040145C		
Formatter Chip 6	CF	0040185C		
Formatter Chip 7	DB	00401C5C		

Description	REG ID	Address	Access	Width
Link 8 Data FIFO Occupancy Count Register: FMT_LINK_OCC_COUNT(fmt,lnk)			R	9
Formatter Chip 0	88	00400060		
Formatter Chip 1	94	00400460		
Formatter Chip 2	A0	00400860		
Formatter Chip 3	AC	00400C60		
Formatter Chip 4	B8	00401060		
Formatter Chip 5	C4	00401460		
Formatter Chip 6	D0	00401860		
Formatter Chip 7	DC	00401C60		

Description	REG ID	Address	Access	Width
Link 9 Data FIFO Occupancy Count Register: FMT_LINK_OCC_COUNT(fmt,lnk)			R	9
Formatter Chip 0	89	00400064		
Formatter Chip 1	95	00400464		
Formatter Chip 2	A1	00400864		
Formatter Chip 3	AD	00400C64		
Formatter Chip 4	B9	00401064		
Formatter Chip 5	C5	00401464		
Formatter Chip 6	D1	00401864		
Formatter Chip 7	DD	00401C64		

Description	REG ID	Address	Access	Width
Link 10 Data FIFO Occupancy Count Register: FMT_LINK_OCC_COUNT(fmt,lnk)			R	9
Formatter Chip 0	8A	00400068		
Formatter Chip 1	96	00400468		
Formatter Chip 2	A2	00400868		
Formatter Chip 3	AE	00400C68		
Formatter Chip 4	BA	00401068		
Formatter Chip 5	C6	00401468		
Formatter Chip 6	D2	00401868		
Formatter Chip 7	DE	00401C68		

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>Link 11 Data FIFO Occupancy Count Register:</b> <b>FMT_LINK_OCC_COUNT (fmt,lnk)</b>			R	9
Formatter Chip 0	8B	0040006C		
Formatter Chip 1	97	0040046C		
Formatter Chip 2	A3	0040086C		
Formatter Chip 3	AF	00400C6C		
Formatter Chip 4	BB	0040106C		
Formatter Chip 5	C7	0040146C		
Formatter Chip 6	D3	0040186C		
Formatter Chip 7	DF	00401C6C		

### 3.6 Error Status Registers

Description	REG ID	Address	Access	Width
<b>Time Out Error Register: FMT_TIMEOUT_ERROR (fmt)</b>			R	12
Formatter Chip 0	E0	00400070		
Formatter Chip 1	E1	00400470		
Formatter Chip 2	E2	00400870		
Formatter Chip 3	E3	00400C70		
Formatter Chip 4	E4	00401070		
Formatter Chip 5	E5	00401470		
Formatter Chip 6	E6	00401870		
Formatter Chip 7	E7	00401C70		
Time Out Error Status Bit to indicate that the link has received the token but no data has arrived from the module within the time limit set by the Token to Readout Timeout Limit Register. When a time out occurs on a link, the status is latched into this register. This register is cleared when it is read by the host			Bit Value	
			1	0
<b>Bits[11:0] : Links/Modules[11:0]</b>			Error	OK

Description	REG ID	Address	Access	Width
<b>Data Overflow Error Register:</b> <b>FMT_DATA_OVERFLOW_ERROR (fmt)</b>			R	12
Formatter Chip 0	E8	00400074		
Formatter Chip 1	E9	00400474		
Formatter Chip 2	EA	00400874		
Formatter Chip 3	EB	00400C74		
Formatter Chip 4	EC	00401074		
Formatter Chip 5	ED	00401474		
Formatter Chip 6	EE	00401874		
Formatter Chip 7	EF	00401C74		
Data Overflow Error Status Bit to indicate that too much data has gone into the FIFO for 1 Event. When a data overflow error occurs on a link, the status is latched into this register. This register is cleared when the host reads it.			Bit Value	
			1	0
<b>Bits[11:0] : Links [11:0]</b>			Error	OK

Description	REG ID	Address	Access	Width
<b>Header Trailer Error Register:</b> <b>FMT_HEADER_TRAILER_ERR (fmt)</b>			R	12
Formatter Chip 0	F0	00400078		
Formatter Chip 1	F1	00400478		
Formatter Chip 2	F2	00400878		
Formatter Chip 3	F3	00400C78		
Formatter Chip 4	F4	00401078		
Formatter Chip 5	F5	00401478		
Formatter Chip 6	F6	00401878		
Formatter Chip 7	F7	00401C78		
Header/Trailer Limit Status Status of the Header/Trailer Limit bit for this link. Indicates that the link is almost full and the Link Formatter is only writing Header/Trailer words to the Link FIFO. When a header trailer (FIFO almost full) error occurs on a link, the status is latched into this register. This register is cleared when the host reads it.			Bit Value	
			1	0
<b>Bits[11:0] : Links [11:0]</b>			Error	OK

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>ROD Busy Error Register: FMT ROD BUSY ERR(fmt)</b>				
Formatter Chip 0	F8	0040007C	R	12
Formatter Chip 1	F9	0040047C		
Formatter Chip 2	FA	0040087C		
Formatter Chip 3	FB	00400C7C		
Formatter Chip 4	FC	0040107C		
Formatter Chip 5	FD	0040147C		
Formatter Chip 6	FE	0040187C		
Formatter Chip 7	FF	00401C7C		
ROD Busy Limit Status Status of the ROD Busy Limit bit for this link. Indicates that the FIFO for this is full and data is still arriving from the FE Module. This is a fatal error. Resetting the Formatter is the only way to recover from a ROD Busy Limit Error. This register is cleared when the host reads it.			Bit Value	
			1	0
<b>Bits[11:0] : Links [11:0]</b>			Error	OK

### 3.7 Diagnostic Status Registers

Description	REG ID	Address	Access	Width
<b>Normal or Raw Data Format Status Bit: FMT DATA FMT STATUS(fmt)</b>			R	12
Formatter Chip 0	100	00400080		
Formatter Chip 1	101	00400480		
Formatter Chip 2	102	00400880		
Formatter Chip 3	103	00400C80		
Formatter Chip 4	104	00401080		
Formatter Chip 5	105	00401480		
Formatter Chip 6	106	00401880		
Formatter Chip 7	107	00401C80		
Data Parsing Mode Status If this bit is set, the Formatter is parsing data in "Normal" Mode (Condensed, or Expanded Data Formats). If this bit is cleared, the Formatter is parsing data in "Raw" format. The status is latched into this register if the link goes into "raw data" mode, and is cleared when the host reads it.			Bit Value	
			1	0
<b>Bits[11:0] : Links [11:0]</b>			Normal	Raw

Description	REG ID	Address	Access	Width
<b>Formatter Status Register: FMT STATUS(fmt)</b>				
Formatter Chip 0	108	00400084	R	32
Formatter Chip 1	109	00400484		
Formatter Chip 2	10A	00400884		
Formatter Chip 3	10B	00400C84		
Formatter Chip 4	10C	00401084		
Formatter Chip 5	10D	00401484		
Formatter Chip 6	10E	00401884		
Formatter Chip 7	10F	00401C84		
			Bit Value	
			1	0
<b>Bits[ 4:0] : Trigger Count - Number of pending triggers in the Master Form.</b>			Count	
<b>Bit 5 : Link Mode Bits FIFO Reset State</b>			Active	Reset
<b>Bit 6 : Link Mode Bits FIFO Empty Flag: Mode Bits FIFO is empty</b>			Empty	OK
<b>Bit 7 : Link Mode Bits FIFO Full Flag: Mode Bits FIFO is full</b>			Full	OK
<b>Bits[11:8] : Active Link Status</b>			Link Number	
<b>Bit 12 : Chip Has Token Status</b>			Token	Idle
<b>Bit 13 : Hold Output</b>			Hold	OK
<b>Bit 14 : Master/Slave Status</b>			Master	Slave
<b>Bit 15 : Formatter DLL Locked</b>			Locked	Error
<b>Bits[26:16]: Extended Trigger Count</b>			Count	
<b>Bit 27 : Trigger Overflow</b>			Overflow	OK

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>Formatter Version Register: FMT_VERSION(fmt)</b>				
Formatter Chip 0	110	00400088	R	18
Formatter Chip 1	111	00400488		
Formatter Chip 2	112	00400888		
Formatter Chip 3	113	00400C88		
Formatter Chip 4	114	00401088		
Formatter Chip 5	115	00401488		
Formatter Chip 6	116	00401888		
Formatter Chip 7	117	00401C88		
			<b>Bit Value</b>	
			1	0
<b>Bits[ 7: 0] : Code Version</b>			Value	
<b>Bits[12: 8] : Board Revision</b>			0x0Ch	
<b>Bits[14:13] : Pixel Decoder Type == "00" - Single Link 40MHz Decoder "01" - Dual Link 80MHz input "10" - Quad Link 160MHz input</b>			Value	
<b>Bit[15] : Formatter Type</b>			Pixel	SCT
<b>Bits[17:16] : Formatter Number == "00" - Formatter 0 "01" - Formatter 1 "10" - Formatter 2 "11" - Formatter 3</b>			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width																																																					
<b>ModeBits Status - Links 0 to 11: FMT_MODEBIT_STAT(fmt)</b>																																																									
Formatter Chip 0	118	0040008C	R	32																																																					
Formatter Chip 1	119	0040048C																																																							
Formatter Chip 2	11A	0040088C																																																							
Formatter Chip 3	11B	00400C8C																																																							
Formatter Chip 4	11C	0040108C																																																							
Formatter Chip 5	11D	0040148C																																																							
Formatter Chip 6	11E	0040188C																																																							
Formatter Chip 7	11F	00401C8C																																																							
Current Read Out Mode Bits, Links 0 to 5 This value is the last set of mode bits used by this link. It is used as a diagnostic tool, and is used primarily when the ROD is processing events one at a time.			<b>Bit Value</b>																																																						
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 5%;">MB1</th> <th style="width: 5%;">MB0</th> <th style="width: 90%;">Formatter Read Out Mode Bits Definitions</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>Play 1st event from Link FIFO. Normal data flow from Formatter to EFB.</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>Mask this link for 1 event. In this mode, the formatter will dump one event from the link FIFO.</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>Skip read out of this link for 1 event for re-synchronization.</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>Read out 1<sup>st</sup> event from FIFO and dump it on the floor, play the 2nd event to the EFB.</td> </tr> </tbody> </table>			MB1	MB0	Formatter Read Out Mode Bits Definitions	0	0	Play 1st event from Link FIFO. Normal data flow from Formatter to EFB.	0	1	Mask this link for 1 event. In this mode, the formatter will dump one event from the link FIFO.	1	0	Skip read out of this link for 1 event for re-synchronization.	1	1	Read out 1 <sup>st</sup> event from FIFO and dump it on the floor, play the 2nd event to the EFB.																																								
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<b>Bits[ 1: 0] : SCT Link 0 / PXL Module 0</b>			(MB1:MB0)																																																						
<b>Bits[ 3: 2] : SCT Link 1 / PXL Module 1</b>			(MB1:MB0)																																																						
<b>Bits[ 5: 4] : SCT Link 2 / PXL Module 2</b>			(MB1:MB0)																																																						
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<b>Bits[ 9: 8] : SCT Link 4</b>			(MB1:MB0)																																																						
<b>Bits[11:10] : SCT Link 5</b>			(MB1:MB0)																																																						
<b>Bits[13:12] : SCT Link 6</b>			(MB1:MB0)																																																						
<b>Bits[15:14] : SCT Link 7</b>			(MB1:MB0)																																																						
<b>Bits[17:16] : SCT Link 8</b>			(MB1:MB0)																																																						
<b>Bits[19:18] : SCT Link 9</b>			(MB1:MB0)																																																						
<b>Bits[21:20] : SCT Link 10</b>			(MB1:MB0)																																																						
<b>Bits[23:22] : SCT Link 11</b>			(MB1:MB0)																																																						
<b>Bits[31:28] : Diagnostics - Readout FIFO Controller Status</b>			Value																																																						
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Read Out Mode	Description	Value																																																							
reset	Reset	0x1h																																																							
idle	Wait for Mode from RCF	0x2h																																																							
fmb	Fetch current Mode Bits	0x3h																																																							
wfmb	Wait for current Mode Bits																																																								
wft	Wait for token	0x4h																																																							
rolf	Read out link FIFO	0x5h																																																							
wfd	Wait for data	0x6h																																																							
wfd td	Trailer detected in wait for data																																																								
doe	Dump one event from the link FIFO	0x7h																																																							
wfd doe	Wait for data, while dump one event																																																								
doe ret	Return to DOE																																																								
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## APPENDIX A: ROD and BOC FPGA Register Definitions

### 3.8 Formatter Link Counters and Link Counter Control

Description	REG ID	Address	Access	Width
<b>Formatter Input Counter Control: FMT_CNT_COUNTER(fmt)</b>				
Formatter Chip 0		00400090	R	32
Formatter Chip 1		00400490		
Formatter Chip 2		00400890		
Formatter Chip 3		00400C90		
Formatter Chip 4		00401090		
Formatter Chip 5		00401490		
Formatter Chip 6		00401890		
Formatter Chip 7		00401C90		
This bit enables the link counters in each formatter. During this bit being reset, the global counter set value (FMT_GLB_COUNTER[15:0]) can be written and is transferred into the global counter recent value register part (FMT_GLB_COUNTER[31:16]), while the stream counters (FMT_STREAM_XY) are reset to zero. While the bit is set, the global counter recent value is counted down to zero and while not being zero, the stream counters are added up.			<b>Bit Value</b>	
			1	0
<b>Bit[0]</b> : Enable Counters			Counting	Reset

Description	REG ID	Address	Access	Width
<b>Formatter Global Input Counter: FMT_GLB_COUNTER(fmt)</b>				
Formatter Chip 0		00400094	R	32
Formatter Chip 1		00400494		
Formatter Chip 2		00400894		
Formatter Chip 3		00400C94		
Formatter Chip 4		00401094		
Formatter Chip 5		00401494		
Formatter Chip 6		00401894		
Formatter Chip 7		00401C94		
			<b>Bit Value</b>	
			1	0
<b>Bits[15: 0]</b> : Global Counter Set Value - During FMT_CNT_COUNTER Bit[0]=0 (Reset of the Counters) this value is transferred into Bits[31:16]			Value	
<b>Bits[31:16]</b> : Global Counter Recent Value - While this value is higher than 0 and the FMT_CNT_COUNTER Bit[0] is equal 1, this value decreased by one every clock cycle			Value	

Description	REG ID	Address	Access	Width
<b>Formatter Global Input Counter: FMT_STREAM_01(fmt)</b>				
Formatter Chip 0		00400098	R	32
Formatter Chip 1		00400498		
Formatter Chip 2		00400898		
Formatter Chip 3		00400C98		
Formatter Chip 4		00401098		
Formatter Chip 5		00401498		
Formatter Chip 6		00401898		
Formatter Chip 7		00401C98		
			<b>Bit Value</b>	
			1	0
<b>Bits[15: 0]</b> : Stream counter value for input stream 0 of the formatter This value adds up incoming data bits while FMT_CNT_COUNTER[0] is equal 1 and FMT_GLB_COUNTER[31:16] value is not zero			Value	
<b>Bits[31:16]</b> : Stream counter value for input stream 1 of the formatter This value adds up incoming data bits while FMT_CNT_COUNTER[0] is equal 1 and FMT_GLB_COUNTER[31:16] value is not zero			Value	



## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>Formatter Global Input Counter: FMT_STREAM_23(fmt)</b>				
Formatter Chip 0		0040009C	R	32
Formatter Chip 1		0040049C		
Formatter Chip 2		0040089C		
Formatter Chip 3		00400C9C		
Formatter Chip 4		0040109C		
Formatter Chip 5		0040149C		
Formatter Chip 6		0040189C		
Formatter Chip 7		00401C9C		
			<b>Bit Value</b>	
			1	0
<b>Bits[15: 0]</b> : Stream counter value for input stream 2 of the formatter This value adds up incoming data bits while FMT_CNT_COUNTER[0] is equal 1 and FMT_GLB_COUNTER[31:16] value is not zero			Value	
<b>Bits[31:16]</b> : Stream counter value for input stream 3 of the formatter This value adds up incoming data bits while FMT_CNT_COUNTER[0] is equal 1 and FMT_GLB_COUNTER[31:16] value is not zero			Value	

**NOTE: The PIXEL Data Stream Simulator starts at 0xA0 in the Formatter. Check for the register description later in the manual (near the SCT simulator).**

Description	REG ID	Address	Access	Width
<b>Formatter Global Input Counter: FMT_STREAM_45(fmt)</b>				
Formatter Chip 0		004000A0	R	32
Formatter Chip 1		004004A0		
Formatter Chip 2		004008A0		
Formatter Chip 3		00400CA0		
Formatter Chip 4		004010A0		
Formatter Chip 5		004014A0		
Formatter Chip 6		004018A0		
Formatter Chip 7		00401CA0		
<b>Only exists in SCT formatters</b>			<b>Bit Value</b>	
			1	0
<b>Bits[15: 0]</b> : Stream counter value for input stream 4 of the formatter This value adds up incoming data bits while FMT_CNT_COUNTER[0] is equal 1 and FMT_GLB_COUNTER[31:16] value is not zero			Value	
<b>Bits[31:16]</b> : Stream counter value for input stream 5 of the formatter This value adds up incoming data bits while FMT_CNT_COUNTER[0] is equal 1 and FMT_GLB_COUNTER[31:16] value is not zero			Value	

Description	REG ID	Address	Access	Width
<b>Formatter Global Input Counter: FMT_STREAM_67(fmt)</b>				
Formatter Chip 0		004000A4	R	32
Formatter Chip 1		004004A4		
Formatter Chip 2		004008A4		
Formatter Chip 3		00400CA4		
Formatter Chip 4		004010A4		
Formatter Chip 5		004014A4		
Formatter Chip 6		004018A4		
Formatter Chip 7		00401CA4		
<b>Only exists in SCT formatters</b>			<b>Bit Value</b>	
			1	0
<b>Bits[15: 0]</b> : Stream counter value for input stream 6 of the formatter This value adds up incoming data bits while FMT_CNT_COUNTER[0] is equal 1 and FMT_GLB_COUNTER[31:16] value is not zero			Value	
<b>Bits[31:16]</b> : Stream counter value for input stream 7 of the formatter This value adds up incoming data bits while FMT_CNT_COUNTER[0] is equal 1 and FMT_GLB_COUNTER[31:16] value is not zero			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>Formatter Global Input Counter: FMT_STREAM_89(fmt)</b>				
Formatter Chip 0		004000A8	R	32
Formatter Chip 1		004004A8		
Formatter Chip 2		004008A8		
Formatter Chip 3		00400CA8		
Formatter Chip 4		004010A8		
Formatter Chip 5		004014A8		
Formatter Chip 6		004018A8		
Formatter Chip 7		00401CA8		
Only exists in SCT formatters			<b>Bit Value</b>	
			1	0
<b>Bits[15: 0]</b> : Stream counter value for input stream 8 of the formatter This value adds up incoming data bits while FMT_CNT_COUNTER[0] is equal 1 and FMT_GLB_COUNTER[31:16] value is not zero			Value	
<b>Bits[31:16]</b> : Stream counter value for input stream 9 of the formatter This value adds up incoming data bits while FMT_CNT_COUNTER[0] is equal 1 and FMT_GLB_COUNTER[31:16] value is not zero			Value	

Description	REG ID	Address	Access	Width
<b>Formatter Global Input Counter: FMT_STREAM_AB(fmt)</b>				
Formatter Chip 0		004000AC	R	32
Formatter Chip 1		004004AC		
Formatter Chip 2		004008AC		
Formatter Chip 3		00400CAC		
Formatter Chip 4		004010AC		
Formatter Chip 5		004014AC		
Formatter Chip 6		004018AC		
Formatter Chip 7		00401CAC		
Only exists in SCT formatters			<b>Bit Value</b>	
			1	0
<b>Bits[15: 0]</b> : Stream counter value for input stream 10 of the formatter This value adds up incoming data bits while FMT_CNT_COUNTER[0] is equal 1 and FMT_GLB_COUNTER[31:16] value is not zero			Value	
<b>Bits[31:16]</b> : Stream counter value for input stream 11 of the formatter This value adds up incoming data bits while FMT_CNT_COUNTER[0] is equal 1 and FMT_GLB_COUNTER[31:16] value is not zero			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

### 3.9 Formatter Data Stream Simulators: Pixel and SCT

#### PIXEL SPECIFIC:

Description	REG ID	Address	Access	Width
<b>Formatter Data Stream Simulator Control:</b> <b>FMT SIM CTRL 1(fmt) **** PXL VERSION ****</b>			RW	32
Formatter Chip 0		004000A0		
Formatter Chip 1		004004A0		
Formatter Chip 2		004008A0		
Formatter Chip 3		00400CA0		
Formatter Chip 4		004010A0		
Formatter Chip 5		004014A0		
Formatter Chip 6		004018A0		
Formatter Chip 7		00401CA0		
			<b>Bit Value</b>	
			1	0
<b>Bit[0]</b> : Activate Simulator			ON	OFF
<b>Bits[ 2: 1]</b> : Data Decoder Mode			"00" = 40 Mbit/s "01" = 80 Mbit/s "10" = 160 Mbit/s	
<b>Bit[3]</b> : Simulator Mode			Multiple	Single
<b>Bits[ 7: 4]</b> : Number of sequential L1A triggers in each event			Value	
<b>Bit[8]</b> : Not Used			x	x
<b>Bits[12: 9]</b> : Number of MCC Skipped Events in each event (See note in Users Manual v1.64 or later)			Value	
<b>Bits[15:13]</b> : Header Pattern to transmit	Normal header: '11101' Bit-flip header: '11100' Bit-flip header: '11111' Bit-flip header: '11001' Bit-flip header: '10101' Bit-flip header: '01101' Bit-flip header: '111101'		'000' '001' '010' '011' '100' '101' '110'	
<b>Bits[23:16]</b> : 8-bit MCC flags			Value	
<b>Bits[31:24]</b> : 8-bit FE flags			Value	

Description	REG ID	Address	Access	Width
<b>Formatter Data Stream Simulator Control:</b> <b>FMT SIM CTRL 2(fmt) **** PXL VERSION ****</b>			RW	32
Formatter Chip 0		004000A4		
Formatter Chip 1		004004A4		
Formatter Chip 2		004008A4		
Formatter Chip 3		00400CA4		
Formatter Chip 4		004010A4		
Formatter Chip 5		004014A4		
Formatter Chip 6		004018A4		
Formatter Chip 7		00401CA4		
			<b>Bit Value</b>	
			1	0
<b>Bits[ 2: 0]</b> : Bit Flip Patterns	No bit flip Bit flip all Periodic bit flip (see reg bits 23-3)		'000' '001' '010'	
<b>Bits[23: 3]</b> : Bit flip settings (get description from Jens)			Value	
<b>Bits[31:24]</b> : Number of hits to generate for each event. Hits will be inserted into the mid BC of all sequential L1A events			Value	

Description	REG ID	Address	Access	Width
<b>Formatter Global PXL Resync Counter: xxx(fmt)</b>			R	32
Formatter Chip 0, MOD 0		004000B0		
Formatter Chip 1, MOD 0		004004B0		
Formatter Chip 2, MOD 0		004008B0		
Formatter Chip 3, MOD 0		00400CB0		
Formatter Chip 4, MOD 0		004010B0		
Formatter Chip 5, MOD 0		004014B0		
Formatter Chip 6, MOD 0		004018B0		
Formatter Chip 7, MOD 0		00401CB0		
Pixel formatters ONLY			<b>Bit Value</b>	
			1	0
<b>Bits[31: 0]</b> : Counts the number of times the Formatter forces the FE Module data into synchronization following MCC skipped event flags			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Formatter Global PXL Resync Counter: xxx(fmt)			R	32
Formatter Chip 0, MOD 1		004000B4		
Formatter Chip 1, MOD 1		004004B4		
Formatter Chip 2, MOD 1		004008B4		
Formatter Chip 3, MOD 1		00400CB4		
Formatter Chip 4, MOD 1		004010B4		
Formatter Chip 5, MOD 1		004014B4		
Formatter Chip 6, MOD 1		004018B4		
Formatter Chip 7, MOD 1		00401CB4		
Pixel formatters ONLY			Bit Value	
			1	0
Bits[31: 0] : Counts the number of times the Formatter forces the FE Module data into synchronization following MCC skipped event flags			Value	

Description	REG ID	Address	Access	Width
Formatter Global PXL Resync Counter: xxx(fmt)			R	32
Formatter Chip 0, MOD 2		004000B8		
Formatter Chip 1, MOD 2		004004B8		
Formatter Chip 2, MOD 2		004008B8		
Formatter Chip 3, MOD 2		00400CB8		
Formatter Chip 4, MOD 2		004010B8		
Formatter Chip 5, MOD 2		004014B8		
Formatter Chip 6, MOD 2		004018B8		
Formatter Chip 7, MOD 2		00401CB8		
Pixel formatters ONLY			Bit Value	
			1	0
Bits[31: 0] : Counts the number of times the Formatter forces the FE Module data into synchronization following MCC skipped event flags			Value	

Description	REG ID	Address	Access	Width
Formatter Global PXL Resync Counter: xxx(fmt)			R	32
Formatter Chip 0, MOD 3		004000BC		
Formatter Chip 1, MOD 3		004004BC		
Formatter Chip 2, MOD 3		004008BC		
Formatter Chip 3, MOD 3		00400CBC		
Formatter Chip 4, MOD 3		004010BC		
Formatter Chip 5, MOD 3		004014BC		
Formatter Chip 6, MOD 3		004018BC		
Formatter Chip 7, MOD 3		00401CBC		
Pixel formatters ONLY			Bit Value	
			1	0
Bits[31: 0] : Counts the number of times the Formatter forces the FE Module data into synchronization following MCC skipped event flags			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

SCT SPECIFIC:

Description	REG ID	Address	Access	Width
<b>Formatter Data Stream Simulator Control:</b> <b>FMT_SIM_CTRL(fmt) **** SCT VERSION ****</b>			RW	32
Formatter Chip 0		004000B0		
Formatter Chip 1		004004B0		
Formatter Chip 2		004008B0		
Formatter Chip 3		00400CB0		
Formatter Chip 4		004010B0		
Formatter Chip 5		004014B0		
Formatter Chip 6		004018B0		
Formatter Chip 7		00401CB0		
			<b>Bit Value</b>	
			<b>1</b>	<b>0</b>
<b>Bit [0]</b> : Activate Simulation			ON	OFF
<b>Bit [1]</b> : CLK/2 Mode			Value	
<b>Bit [2]</b> : Debug Mode - Writes L1ID and BCID to Hit Data			Value	
<b>Bits[ 7: 3]</b> : Custom Header (Field value translated as the header)			Value	
<b>Bits[ 9: 8]</b> : Hit Probability "00" = always send a hit "01" = half hit / half empty "10" = mostly empty, some hits (1 per strip every 128 events) "11" = always an empty event			Value	
<b>Bits[11:10]</b> : Error Probability "00" = always send hit/empty, so do nothing "01" = mostly OK, but some errors "10" = half OK / half error "11" = always an error			Value	
<b>Bits[15:12]</b> : Number of chips ("0000" = 1 chip)			Value	
<b>Bits[22:16]</b> : Number of Hits/Chip			Value	
<b>Bits[25:23]</b> : Hit Map "000" = fixed at 011 "001" = fixed at 010 "010" = detector alignment 1xx "011" = detector alignment x1x "100" = detector alignment xx1 "101" = Level mode x1x "110" = Edge mode 01x "111" = Test mode xxx			Value	
<b>Bits[27:26]</b> : Cluster Size			Value	
<b>Bits[29:28]</b> : Bit Flip Probability in Link 0			Value	
<b>Bits[31:30]</b> : Bit Flip Probability in Link 1			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Formatter FE Module Stuck Bit Mask Filter Register: FMT SB MASK FILTER(fmt) **** SCT VERSION ****	RW	32
Formatter Chip 0, Link0		004000C0
Formatter Chip 1, Link0		004004C0
Formatter Chip 2, Link0		004008C0
Formatter Chip 3, Link0		00400CC0
Formatter Chip 4, Link0		004010C0
Formatter Chip 5, Link0		004014C0
Formatter Chip 6, Link0		004018C0
Formatter Chip 7, Link0		00401CC0
Formatter Chip 0, Link1		004000C4
Formatter Chip 1, Link1		004004C4
Formatter Chip 2, Link1		004008C4
Formatter Chip 3, Link1		00400CC4
Formatter Chip 4, Link1		004010C4
Formatter Chip 5, Link1		004014C4
Formatter Chip 6, Link1		004018C4
Formatter Chip 7, Link1		00401CC4
Formatter Chip 0, Link2		004000C8
Formatter Chip 1, Link2		004004C8
Formatter Chip 2, Link2		004008C8
Formatter Chip 3, Link2		00400CC8
Formatter Chip 4, Link2		004010C8
Formatter Chip 5, Link2		004014C8
Formatter Chip 6, Link2		004018C8
Formatter Chip 7, Link2		00401CC8
Formatter Chip 0, Link3		004000CC
Formatter Chip 1, Link3		004004CC
Formatter Chip 2, Link3		004008CC
Formatter Chip 3, Link3		00400CCC
Formatter Chip 4, Link3		004010CC
Formatter Chip 5, Link3		004014CC
Formatter Chip 6, Link3		004018CC
Formatter Chip 7, Link3		00401CCC
The stuck bit pipeline mask is used to mask a single time bin pipeline defect in the SCT front end module. There are 2 independent filters per link. The filter only masks orphan hits in the data stream. The stuck bit will be present in the data if it is included in a cluster	Bit Value	
	1	0
<b>Bits[3:0]</b> : Time Bin Pipeline to Mask, Filter A	Value	
<b>Bits[7:4]</b> : Chip in FE Module to Mask, Filter A	Value	
<b>Bits[14:8]</b> : Channel in FE Module to Mask , Filter A	Value	
<b>Bit [15]</b> : Enable Filter A	Enable	Disable
<b>Bits[19:16]</b> : Time Bin Pipeline to Mask, Filter B	Value	
<b>Bits[23:20]</b> : Chip in FE Module to Mask, Filter B	Value	
<b>Bits[30:24]</b> : Channel in FE Module to Mask , Filter B	Value	
<b>Bit [31]</b> : Enable Filter B	Enable	Disable

## APPENDIX A: ROD and BOC FPGA Register Definitions

Formatter FE Module Stuck Bit Mask Filter Register: FMT SB MASK FILTER(fmt) **** SCT VERSION ****			RW	32
Formatter Chip 0, Link4		004000D0		
Formatter Chip 1, Link4		004004D0		
Formatter Chip 2, Link4		004008D0		
Formatter Chip 3, Link4		00400CD0		
Formatter Chip 4, Link4		004010D0		
Formatter Chip 5, Link4		004014D0		
Formatter Chip 6, Link4		004018D0		
Formatter Chip 7, Link4		00401CD0		
Formatter Chip 0, Link5		004000D4		
Formatter Chip 1, Link5		004004D4		
Formatter Chip 2, Link5		004008D4		
Formatter Chip 3, Link5		00400CD4		
Formatter Chip 4, Link5		004010D4		
Formatter Chip 5, Link5		004014D4		
Formatter Chip 6, Link5		004018D4		
Formatter Chip 7, Link5		00401CD4		
Formatter Chip 0, Link6		004000D8		
Formatter Chip 1, Link6		004004D8		
Formatter Chip 2, Link6		004008D8		
Formatter Chip 3, Link6		00400CD8		
Formatter Chip 4, Link6		004010D8		
Formatter Chip 5, Link6		004014D8		
Formatter Chip 6, Link6		004018D8		
Formatter Chip 7, Link6		00401CD8		
Formatter Chip 0, Link7		004000DC		
Formatter Chip 1, Link7		004004DC		
Formatter Chip 2, Link7		004008DC		
Formatter Chip 3, Link7		00400CDC		
Formatter Chip 4, Link7		004010DC		
Formatter Chip 5, Link7		004014DC		
Formatter Chip 6, Link7		004018DC		
Formatter Chip 7, Link7		00401CDC		
The stuck bit pipeline mask is used to mask a single time bin pipeline defect in the SCT front end module. There are 2 independent filters per link. The filter only masks orphan hits in the data stream. The stuck bit will be present in the data if it is included in a cluster	<b>Bit Value</b>			
	1	0		
<b>Bits[3:0]</b> : Time Bin Pipeline to Mask, Filter A		Value		
<b>Bits[7:4]</b> : Chip in FE Module to Mask, Filter A		Value		
<b>Bits[14:8]</b> : Channel in FE Module to Mask , Filter A		Value		
<b>Bit [15]</b> : Enable Filter A		Enable	Disable	
<b>Bits[19:16]</b> : Time Bin Pipeline to Mask, Filter B		Value		
<b>Bits[23:20]</b> : Chip in FE Module to Mask, Filter B		Value		
<b>Bits[30:24]</b> : Channel in FE Module to Mask , Filter B		Value		
<b>Bit [31]</b> : Enable Filter B		Enable	Disable	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Formatter FE Module Stuck Bit Mask Filter Register: FMT SB MASK FILTER(fmt) **** SCT VERSION ****			RW	32
Formatter Chip 0, Link8		004000E0		
Formatter Chip 1, Link8		004004E0		
Formatter Chip 2, Link8		004008E0		
Formatter Chip 3, Link8		00400CE0		
Formatter Chip 4, Link8		004010E0		
Formatter Chip 5, Link8		004014E0		
Formatter Chip 6, Link8		004018E0		
Formatter Chip 7, Link8		00401CE0		
Formatter Chip 0, Link9		004000E4		
Formatter Chip 1, Link9		004004E4		
Formatter Chip 2, Link9		004008E4		
Formatter Chip 3, Link9		00400CE4		
Formatter Chip 4, Link9		004010E4		
Formatter Chip 5, Link9		004014E4		
Formatter Chip 6, Link9		004018E4		
Formatter Chip 7, Link9		00401CE4		
Formatter Chip 0, Link10		004000E8		
Formatter Chip 1, Link10		004004E8		
Formatter Chip 2, Link10		004008E8		
Formatter Chip 3, Link10		00400CE8		
Formatter Chip 4, Link10		004010E8		
Formatter Chip 5, Link10		004014E8		
Formatter Chip 6, Link10		004018E8		
Formatter Chip 7, Link10		00401CE8		
Formatter Chip 0, Link11		004000EC		
Formatter Chip 1, Link11		004004EC		
Formatter Chip 2, Link11		004008EC		
Formatter Chip 3, Link11		00400CEC		
Formatter Chip 4, Link11		004010EC		
Formatter Chip 5, Link11		004014EC		
Formatter Chip 6, Link11		004018EC		
Formatter Chip 7, Link11		00401CEC		
The stuck bit pipeline mask is used to mask a single time bin pipeline defect in the SCT front end module. There are 2 independent filters per link. The filter only masks orphan hits in the data stream. The stuck bit will be present in the data if it is included in a cluster	<b>Bit Value</b>			
	1	0		
<b>Bits[3:0]</b> : Time Bin Pipeline to Mask, Filter A	Value			
<b>Bits[7:4]</b> : Chip in FE Module to Mask, Filter A	Value			
<b>Bits[14:8]</b> : Channel in FE Module to Mask , Filter A	Value			
<b>Bit [15]</b> : Enable Filter A	Enable	Disable		
<b>Bits[19:16]</b> : Time Bin Pipeline to Mask, Filter B	Value			
<b>Bits[23:20]</b> : Chip in FE Module to Mask, Filter B	Value			
<b>Bits[30:24]</b> : Channel in FE Module to Mask , Filter B	Value			
<b>Bit [31]</b> : Enable Filter B	Enable	Disable		



# APPENDIX A: ROD and BOC FPGA Register Definitions

## 4 ROD EFB FPGA Registers

### 4.1 EFB Error Mask Registers, Engines 0/1

Description	REG ID	Address	Access	Width
EFB: Error mask, Engine0, Link 0, ERROR_MASK(0,0)	140	00402000	RW	32
EFB: Error mask, Engine1, Link 0, ERROR_MASK(1,0)	170	00402100	RW	32
If an Error Count Mask Bit is set in this register, the EFB will not count that specific type of Error for each specified link.	Bit Value			
				1      0
Bit 0: BC ID Error Count			Mask	Count
Bit 1: L1 ID Error Count			Mask	Count
Bit 2: FE Module Timeout Error Count			Mask	Count
Bit 3: Data may be incorrect (see Bits 31:16)			Mask	Count
Bit 4: Internal Buffer Overflow (see Bits 17:16)			Mask	Count
Bits[5:15]: Reserved for Atlas			Mask	Count
Bit 16: Almost Full Error, Data Truncated Count			Mask	Count
Bit 17: Data Overflow Count			Mask	Count
Bit 18: Header Bit Error Count			Mask	Count
Bit 19: Sync Error Count			Mask	Count
Bit 20: (SCT)Flagged Error Count / (Pixel)Invalid Row(>159) OR Column(>17)			Mask	Count
Bit 21: (SCT)Condensed Mode Hit Pattern Error / (Pixel)MCC Sent Empty Event			Mask	Count
Bit 22: (SCT)Non-Sequential Chip Num / (Pixel)MCC Flagged Error - EOCOVERFLOW			Mask	Count
Bit 23: (SCT)Invalid FE Chip / (Pixel)MCC Flagged Error - HAMMINGCODE			Mask	Count
Bit 24: (SCT)Trailer Bit Error Count / (Pixel)MCC Flagged Error - REGPARITY			Mask	Count
Bit 25: (SCT)Active Link Masked / (Pixel)MCC Flagged Error - HITPARITY			Mask	Count
Bit 26: (Pixel)MCC Flagged Error - BITFLIP			Mask	Count
Bit 27: (Pixel)MCC Flagged Error - HITOVERFLOW			Mask	Count
Bit 28: (Pixel)MCC Flagged Error - EOEOVERFLOW			Mask	Count
Bit 29: (Pixel)MCC Flagged Error - L1CHKFAILFE			Mask	Count
Bit 30: (Pixel)MCC Flagged Error - BCIDCHKFAIL			Mask	Count
Bit 31: (Pixel)MCC Flagged Error - L1CHKFAILGLOBAL			Mask	Count

## APPENDIX A: ROD and BOC FPGA Register Definitions

DESCRIPTION	REG ID	ADDRESS	TYPE	WD
EFB: Error mask, Engine0, SCT LINK0/PXL MOD00, ERROR_MASK(0,0)	140	00402000	RW	32
EFB: Error mask, Engine0, SCT LINK1/PXL MOD01, ERROR_MASK(0,1)	141	00402004	RW	32
EFB: Error mask, Engine0, SCT LINK2/PXL MOD02, ERROR_MASK(0,2)	142	00402008	RW	32
EFB: Error mask, Engine0, SCT LINK3/PXL MOD03, ERROR_MASK(0,3)	143	0040200C	RW	32
EFB: Error mask, Engine0, SCT LINK4, ERROR_MASK(0,4)	144	00402010	RW	32
EFB: Error mask, Engine0, SCT LINK5, ERROR_MASK(0,5)	145	00402014	RW	32
EFB: Error mask, Engine0, SCT LINK6, ERROR_MASK(0,6)	146	00402018	RW	32
EFB: Error mask, Engine0, SCT LINK7, ERROR_MASK(0,7)	147	0040201C	RW	32
EFB: Error mask, Engine0, SCT LINK8, ERROR_MASK(0,8)	148	00402020	RW	32
EFB: Error mask, Engine0, SCT LINK9, ERROR_MASK(0,9)	149	00402024	RW	32
EFB: Error mask, Engine0, SCT LINK10, ERROR_MASK(0,10)	14A	00402028	RW	32
EFB: Error mask, Engine0, SCT LINK11, ERROR_MASK(0,11)	14B	0040202C	RW	32
EFB: Error mask, Engine0, SCT LINK12/PXL MOD10, ERROR_MASK(0,12)	14C	00402040	RW	32
EFB: Error mask, Engine0, SCT LINK13/PXL MOD11, ERROR_MASK(0,13)	14D	00402044	RW	32
EFB: Error mask, Engine0, SCT LINK14/PXL MOD12, ERROR_MASK(0,14)	14E	00402048	RW	32
EFB: Error mask, Engine0, SCT LINK15/PXL MOD13, ERROR_MASK(0,15)	14F	0040204C	RW	32
EFB: Error mask, Engine0, SCT LINK16, ERROR_MASK(0,16)	150	00402050	RW	32
EFB: Error mask, Engine0, SCT LINK17, ERROR_MASK(0,17)	151	00402054	RW	32
EFB: Error mask, Engine0, SCT LINK18, ERROR_MASK(0,18)	152	00402058	RW	32
EFB: Error mask, Engine0, SCT LINK19, ERROR_MASK(0,19)	153	0040205C	RW	32
EFB: Error mask, Engine0, SCT LINK20, ERROR_MASK(0,20)	154	00402060	RW	32
EFB: Error mask, Engine0, SCT LINK21, ERROR_MASK(0,21)	155	00402064	RW	32
EFB: Error mask, Engine0, SCT LINK22, ERROR_MASK(0,22)	156	00402068	RW	32
EFB: Error mask, Engine0, SCT LINK23, ERROR_MASK(0,23)	157	0040206C	RW	32
EFB: Error mask, Engine0, SCT LINK24/PXL MOD20, ERROR_MASK(0,24)	158	00402080	RW	32
EFB: Error mask, Engine0, SCT LINK25/PXL MOD21, ERROR_MASK(0,25)	159	00402084	RW	32
EFB: Error mask, Engine0, SCT LINK26/PXL MOD22, ERROR_MASK(0,26)	15A	00402088	RW	32
EFB: Error mask, Engine0, SCT LINK27/PXL MOD23, ERROR_MASK(0,27)	15B	0040208C	RW	32
EFB: Error mask, Engine0, SCT LINK28, ERROR_MASK(0,28)	15C	00402090	RW	32
EFB: Error mask, Engine0, SCT LINK29, ERROR_MASK(0,29)	15D	00402094	RW	32
EFB: Error mask, Engine0, SCT LINK30, ERROR_MASK(0,30)	15E	00402098	RW	32
EFB: Error mask, Engine0, SCT LINK31, ERROR_MASK(0,31)	15F	0040209C	RW	32
EFB: Error mask, Engine0, SCT LINK32, ERROR_MASK(0,32)	160	004020A0	RW	32
EFB: Error mask, Engine0, SCT LINK33, ERROR_MASK(0,33)	161	004020A4	RW	32
EFB: Error mask, Engine0, SCT LINK34, ERROR_MASK(0,34)	162	004020A8	RW	32
EFB: Error mask, Engine0, SCT LINK35, ERROR_MASK(0,35)	163	004020AC	RW	32
EFB: Error mask, Engine0, SCT LINK36/PXL MOD30, ERROR_MASK(0,36)	164	004020C0	RW	32
EFB: Error mask, Engine0, SCT LINK37/PXL MOD31, ERROR_MASK(0,37)	165	004020C4	RW	32
EFB: Error mask, Engine0, SCT LINK38/PXL MOD32, ERROR_MASK(0,38)	166	004020C8	RW	32
EFB: Error mask, Engine0, SCT LINK39/PXL MOD33, ERROR_MASK(0,39)	167	004020CC	RW	32
EFB: Error mask, Engine0, SCT LINK40, ERROR_MASK(0,40)	168	004020D0	RW	32
EFB: Error mask, Engine0, SCT LINK41, ERROR_MASK(0,41)	169	004020D4	RW	32
EFB: Error mask, Engine0, SCT LINK42, ERROR_MASK(0,42)	16A	004020D8	RW	32
EFB: Error mask, Engine0, SCT LINK43, ERROR_MASK(0,43)	16B	004020DC	RW	32
EFB: Error mask, Engine0, SCT LINK44, ERROR_MASK(0,44)	16C	004020E0	RW	32
EFB: Error mask, Engine0, SCT LINK45, ERROR_MASK(0,45)	16D	004020E4	RW	32
EFB: Error mask, Engine0, SCT LINK46, ERROR_MASK(0,46)	16E	004020E8	RW	32
EFB: Error mask, Engine0, SCT LINK47, ERROR_MASK(0,47)	16F	004020EC	RW	32

## APPENDIX A: ROD and BOC FPGA Register Definitions

DESCRIPTION	REG ID	ADDRESS	TYPE	WD
EFB: Error mask, Engine1, SCT LINK48/PXL MOD40, ERROR_MASK(1,0)	170	00402100	RW	32
EFB: Error mask, Engine1, SCT LINK49/PXL MOD41, ERROR_MASK(1,1)	171	00402104	RW	32
EFB: Error mask, Engine1, SCT LINK50/PXL MOD42, ERROR_MASK(1,2)	172	00402108	RW	32
EFB: Error mask, Engine1, SCT LINK51/PXL MOD43, ERROR_MASK(1,3)	173	0040210C	RW	32
EFB: Error mask, Engine1, SCT LINK52, ERROR_MASK(1,4)	174	00402110	RW	32
EFB: Error mask, Engine1, SCT LINK53, ERROR_MASK(1,5)	175	00402114	RW	32
EFB: Error mask, Engine1, SCT LINK54, ERROR_MASK(1,6)	176	00402118	RW	32
EFB: Error mask, Engine1, SCT LINK55, ERROR_MASK(1,7)	177	0040211C	RW	32
EFB: Error mask, Engine1, SCT LINK56, ERROR_MASK(1,8)	178	00402120	RW	32
EFB: Error mask, Engine1, SCT LINK57, ERROR_MASK(1,9)	179	00402124	RW	32
EFB: Error mask, Engine1, SCT LINK58, ERROR_MASK(1,10)	17A	00402128	RW	32
EFB: Error mask, Engine1, SCT LINK59, ERROR_MASK(1,11)	17B	0040212C	RW	32
EFB: Error mask, Engine1, SCT LINK60/PXL MOD50, ERROR_MASK(1,12)	17C	00402140	RW	32
EFB: Error mask, Engine1, SCT LINK61/PXL MOD51, ERROR_MASK(1,13)	17D	00402144	RW	32
EFB: Error mask, Engine1, SCT LINK62/PXL MOD52, ERROR_MASK(1,14)	17E	00402148	RW	32
EFB: Error mask, Engine1, SCT LINK63/PXL MOD53, ERROR_MASK(1,15)	17F	0040214C	RW	32
EFB: Error mask, Engine1, SCT LINK64, ERROR_MASK(1,16)	180	00402150	RW	32
EFB: Error mask, Engine1, SCT LINK65, ERROR_MASK(1,17)	181	00402154	RW	32
EFB: Error mask, Engine1, SCT LINK66, ERROR_MASK(1,18)	182	00402158	RW	32
EFB: Error mask, Engine1, SCT LINK67, ERROR_MASK(1,19)	183	0040215C	RW	32
EFB: Error mask, Engine1, SCT LINK68, ERROR_MASK(1,20)	184	00402160	RW	32
EFB: Error mask, Engine1, SCT LINK69, ERROR_MASK(1,21)	185	00402164	RW	32
EFB: Error mask, Engine1, SCT LINK70, ERROR_MASK(1,22)	186	00402168	RW	32
EFB: Error mask, Engine1, SCT LINK71, ERROR_MASK(1,23)	187	0040216C	RW	32
EFB: Error mask, Engine1, SCT LINK72/PXL MOD60, ERROR_MASK(1,24)	188	00402180	RW	32
EFB: Error mask, Engine1, SCT LINK73/PXL MOD61, ERROR_MASK(1,25)	189	00402184	RW	32
EFB: Error mask, Engine1, SCT LINK74/PXL MOD62, ERROR_MASK(1,26)	18A	00402188	RW	32
EFB: Error mask, Engine1, SCT LINK75/PXL MOD63, ERROR_MASK(1,27)	18B	0040218C	RW	32
EFB: Error mask, Engine1, SCT LINK76, ERROR_MASK(1,28)	18C	00402190	RW	32
EFB: Error mask, Engine1, SCT LINK77, ERROR_MASK(1,29)	18D	00402194	RW	32
EFB: Error mask, Engine1, SCT LINK78, ERROR_MASK(1,30)	18E	00402198	RW	32
EFB: Error mask, Engine1, SCT LINK79, ERROR_MASK(1,31)	18F	0040219C	RW	32
EFB: Error mask, Engine1, SCT LINK80, ERROR_MASK(1,32)	190	004021A0	RW	32
EFB: Error mask, Engine1, SCT LINK81, ERROR_MASK(1,33)	191	004021A4	RW	32
EFB: Error mask, Engine1, SCT LINK82, ERROR_MASK(1,34)	192	004021A8	RW	32
EFB: Error mask, Engine1, SCT LINK83, ERROR_MASK(1,35)	193	004021AC	RW	32
EFB: Error mask, Engine1, SCT LINK84/PXL MOD70, ERROR_MASK(1,36)	194	004021C0	RW	32
EFB: Error mask, Engine1, SCT LINK85/PXL MOD71, ERROR_MASK(1,37)	195	004021C4	RW	32
EFB: Error mask, Engine1, SCT LINK86/PXL MOD72, ERROR_MASK(1,38)	196	004021C8	RW	32
EFB: Error mask, Engine1, SCT LINK87/PXL MOD73, ERROR_MASK(1,39)	197	004021CC	RW	32
EFB: Error mask, Engine1, SCT LINK88, ERROR_MASK(1,40)	198	004021D0	RW	32
EFB: Error mask, Engine1, SCT LINK89, ERROR_MASK(1,41)	199	004021D4	RW	32
EFB: Error mask, Engine1, SCT LINK90, ERROR_MASK(1,42)	19A	004021D8	RW	32
EFB: Error mask, Engine1, SCT LINK91, ERROR_MASK(1,43)	19B	004021DC	RW	32
EFB: Error mask, Engine1, SCT LINK92, ERROR_MASK(1,44)	19C	004021E0	RW	32
EFB: Error mask, Engine1, SCT LINK93, ERROR_MASK(1,45)	19D	004021E4	RW	32
EFB: Error mask, Engine1, SCT LINK94, ERROR_MASK(1,46)	19E	004021E8	RW	32
EFB: Error mask, Engine1, SCT LINK95, ERROR_MASK(1,47)	19F	004021EC	RW	32

# APPENDIX A: ROD and BOC FPGA Register Definitions

## 4.2 EFB Data Taking Setup Registers

Description	REG ID	Address	Access	Width
<b>EFB: Format Version Register, FORMAT_VRSN</b>	1A0	00402200	R RW	32 16
This is the Format Version Word in the Event Header. The lower half word is RW, and the upper half word is read only and refers to the Format Version defined in the Event Format Specification Distributed by CERN (Current Version = 4.0) The latest specification states that this field can still be 3.1 on the ROD with out causing data stream errors) EDMS: ATL-D-ES-0019 Atlas Communication: ATL-DAQ-98-129			<b>Bit Value</b>	
<b>Bits[31:0]:</b> Format Version Value (U=User Defined)			0301UUUU	

Description	REG ID	Address	Access	Width
<b>EFB: Source ID Register, SOURCE_ID</b>	1A1	00402204	R RW	32 23
This is the Source ID Word in the Event Header. The lower half word is RW, and the upper half word is read only and refers to the Source ID defined in the Event Format Specification Distributed by CERN (Current Version = 3.1) EDMS: ATL-D-ES-0019 Atlas Communication: ATL-DAQ-98-129			<b>Bit Value</b>	
<b>Bits[31:0]:</b> Source ID Value (U=User Defined)			0x00UUUUUU	

Description	REG ID	Address	Access	Width
<b>EFB: Run Number Register, RUN_NUMBER</b>	1A2	00402208	RW	31
This is the Run Number Word in the Event Header. This register stores the Run Number defined in the Event Format Specification Distributed by CERN (Current Version = 3.1) EDMS: ATL-D-ES-0019 Atlas Communication: ATL-DAQ-98-129			<b>Bit Value</b>	
<b>Bits[30:0]:</b> Run Number Value			Value	

Description	REG ID	Address	Access	Width
EFB: Reserved	1A3	0040220C	RW	32
			<b>Bit Value</b>	
			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>EFB: EFB Command 0 Register, EFB_CMND_0</b>	1A4	00402210	RW	32
			<b>Bit Value</b>	
			1	0
<b>Bit 0:</b> Not Used.				
<b>Bit 1:</b> Mask BCID Error When this bit is set, the EFB will not mark BCID Errors for all links			Mask	Allow
<b>Bit 2:</b> Group Event Counter Enable When this bit is set, the EFB will count Events based upon the ROD Specific Event Type			Enable	Disable
<b>Bit 3:</b> Mask L1ID Error When this bit is set, the EFB will not mark L1ID Errors for all links			Mask	Allow
<b>Bits[7:4] :</b> Data Link Output Select This value selects the formatter that supplies the input data stream to the front panel LEMO connector. Value 0x0h => select links 0 to 11 Value 0x1h => select links 12 to 23 Value 0x2h => select links 24 to 35 Value 0x3h => select links 36 to 47 Value 0x4h => select links 48 to 59 Value 0x5h => select links 60 to 71 Value 0x6h => select links 72 to 83 Value 0x7h => select links 84 to 95 Value 0xFh => OR all inputs to output ROD BUSY on the FP LEMO			Value	
<b>Bit 8 :</b> Mask TIM Clock Error When this bit is set, the EFB will not mark TIM Clock Errors.			Mask	Allow
<b>Bit 9 :</b> Mask BOC Clock Error When this bit is set, the EFB will not mark TIM Clock Errors.			Mask	Allow
<b>Bit 10 :</b> Mask Sweeper Event Error When this bit is set, the EFB will not mark Sweeper Event Errors.			Mask	Allow
<b>Bit 11 :</b> L1ID Trap Enable When this bit is set, the EFB will trap L1ID values in a block RAM. Describe the Trapping algorithm			Enable	Idle
<b>Bit 12 :</b> RoL BCID Value Select			TIM BCID	RoL BCID
<b>Bits[23:20] :</b> HV Error Flag Enable			Value	
<b>Bits[31:24] :</b> BCID Offset Value This value can be used to offset the expected BCID if required.			Value	

Description	REG ID	Address	Access	Width
<b>EFB: Formatter Enabled Status, EFB_EVT_LIMIT_THRESH</b>		00402214	R/W	15
This register stores the value used to determine if an Event is over threshold and of interest for trapping in the SDSPs. To trap over threshold events, the proper bit must be set in the Router trapping control registers.			<b>Bit Value</b>	
			1	0
<b>Bits[15:0] :</b> Event Limit Threshold for Router Trap			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>EFB: Run-Time Status Register, EFB_RUNTIME_STAT_REG</b>	<b>1A6</b>	<b>00402218</b>	<b>R</b>	<b>16</b>
			<b>Bit Value</b>	
			<b>1</b>	<b>0</b>
<b>Bit 0:</b> Event FIFO A Almost Full Status Flag Almost Full Flag for the external CY7C4265 FIFO used for EFB data engine 0, 127 words from the 16384 limit.			AFull	OK
<b>Bit 1:</b> Error Summary FIFO A Almost Full Almost Full Flag for the internal Error Summary FIFO used to queue the Event Error counts for each trigger processed in EFB data engine 0.			AFull	OK
<b>Bit 2:</b> Event ID Empty Error, Engine 0 Indicates that event data arrived from Formatter Bank A before the Event ID information was received from the RCF. Can only be cleared with a full ROD Reset.			ID Error	OK
<b>Bit 3:</b> Pause to Formatter, Engine 0 Indicates that backpressure is asserted to Formatter Bank A.			Pause Bank A	OK
<b>Bit 4:</b> Event FIFO B Almost Full Status Flag Almost Full Flag for the external CY7C4265 FIFO used for EFB data engine 1, 127 words from the 16384 word limit.			AFull	OK
<b>Bit 5:</b> Error Summary FIFO B Almost Full Almost Full Flag for the internal Error Summary FIFO used to queue the Event Error counts for each trigger processed in EFB data engine 1.			AFull	OK
<b>Bit 6:</b> Event ID Empty Error, Engine 1 Indicates that event data arrived from the Formatters before the Event ID information was received from the RCF. Can only be cleared with a full ROD Reset. Can only be cleared with a full ROD Reset.			ID Error	OK
<b>Bit 7:</b> Pause to Formatter, Engine 1 Indicates that back pressure is asserted to Formatter Bank B			Pause Bank B	OK
<b>Bit 8:</b> Halt Output from Router Indicates that the Router is asserting backpressure to the EFB. The Event FIFOs will continue to fill until they reach Almost Full			Stop EFB	OK
<b>Bit 9:</b> Event ID Data FIFO Almost Full Global Event ID Data FIFO is ??? words from the full limit			AFull	OK
<b>Bit 10:</b> ROL Test Block Enabled Indicates that the Read Out Link Test in process			Enabled	Off
<b>Bit 11:</b> L1ID Trap data ready for read out			Data Ready	Idle
<b>Bit 12:</b> TBD				
<b>Bit 13:</b> TBD				
<b>Bit 14:</b> TBD				
<b>Bit 15:</b> EFB FPGA Delay Locked Loop Lock Status			Locked	
<b>Bit 16:</b> Formatter 0 is Enabled			Enabled	Idle
<b>Bit 17:</b> Formatter 1 is Enabled			Enabled	Idle
<b>Bit 18:</b> Formatter 2 is Enabled			Enabled	Idle
<b>Bit 19:</b> Formatter 3 is Enabled			Enabled	Idle
<b>Bit 20:</b> Formatter 4 is Enabled			Enabled	Idle
<b>Bit 21:</b> Formatter 5 is Enabled			Enabled	Idle
<b>Bit 22:</b> Formatter 6 is Enabled			Enabled	Idle
<b>Bit 23:</b> Formatter 7 is Enabled			Enabled	Idle

Description	REG ID	Address	Access	Width
<b>EFB: VHDL Code Version and EFB Type, EFB_CODE_VERSION</b>	<b>1B4</b>	<b>0040221C</b>	<b>R</b>	<b>16</b>
			<b>Bit Value</b>	
			<b>1</b>	<b>0</b>
<b>Bits[ 7:0]:</b> Code Version			Value	
<b>Bits[14:8]:</b> Board Revision of Code			Value	
<b>Bit [15] :</b> ROD Type			Pixel	SCT

### 4.3 EFB Diagnostic Registers

Description	REG ID	Address	Access	Width
<b>EFB: Event Header Data, EVENT_HEADER_DATA</b>	<b>1A7</b>	<b>00402220</b>	<b>R</b>	<b>16</b>
This register is used for diagnostics to check the Event Header ID that was in the last event sent to the Router			<b>Bit Value</b>	
<b>Bits[11: 0]:</b> BCID			Value	
<b>Bits[15:12]:</b> L1ID (Lower Nibble)			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>EFB: Event FIFO Data 0, EV_FIFO_DATA1</b>	1A8	00402224	R	16
This register is used for diagnostics to check the last Event ID data that was used by EFB Engine 0.			<b>Bit Value</b>	
<b>Bits[ 7: 0]:</b> BCID (Lower Byte)			Value	
<b>Bits[11: 8]:</b> L1ID (Lower Nibble)			Value	
<b>Bits[15:12]:</b> ROD Event Type			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>EFB: Event FIFO Data 1, EV_FIFO_DATA2</b>	1A9	00402228	R	16
This register is used for diagnostics to check the last Event ID data that was used by EFB Engine 1.			<b>Bit Value</b>	
Bits[ 7: 0]: BCID (Lower Byte)			Value	
Bits[11: 8]: L1ID (Lower Nibble)			Value	
Bits[15:12]: ROD Event Type			Value	

Description	REG ID	Address	Access	Width
<b>EFB: Formatter Group Event Count</b>	1B2	00402230	R	32
The Group Event Counters Count the Occupancy of events in the Formatters sorted by the ROD Event Type field in the EVID data. When all of the data for a specific Group has passed through the EFB the appropriate counter shall be incremented by 1 if the Group counters have been enabled.			<b>Bit Value</b>	
Bits[ 3: 0]: Group 0 Event Count - ROD Event ID 0			Value	
Bits[ 7: 4]: Group 1 Event Count - ROD Event ID 1			Value	
Bits[11: 8]: Group 2 Event Count - ROD Event ID 2			Value	
Bits[15:12]: Group 3 Event Count - ROD Event ID 3			Value	
Bits[19:16]: Group 4 Event Count - ROD Event ID 4			Value	
Bits[23:20]: Group 5 Event Count - ROD Event ID 5			Value	
Bits[27:24]: Group 6 Event Count - ROD Event ID 6			Value	
Bits[31:28]: Group 7 Event Count - ROD Event ID 7			Value	

Description	REG ID	Address	Access	Width
<b>EFB: EFB Bandwidth Counter</b>	1B3	00402234	R	32
			<b>Bit Value</b>	
Bits[15: 0]: Data Count			Value	
Bits[31:16]: Time Count			Value	

Description	REG ID	Address	Access	Width
<b>EFB: Temporary Debug Register</b>	1B4	00402238	R	32
			<b>Bit Value</b>	
Bits[31: 0]:			Value	

Description	REG ID	Address	Access	Width
<b>EFB: Temporary Debug Register</b>	1B5	0040223C	R	32
			<b>Bit Value</b>	
Bits[31: 0]:			Value	

Description	REG ID	Address	Access	Width
<b>EFB: Diagnostic Mode Control Register, EVT_MEM_MODE</b>	1AA	00402240	RW	3
This register is used to set the diagnostic mode of the EFB. (Bits 0, 1 and 2 cannot be turned on simultaneously)			<b>Bit Value</b>	
Bit 0: Enable EFB Diagnostic Mode 0 Write to the EVENTMEM FIFO using the ROD Bus EFB Path, play out to the Router.			1	0
Bit 1: Enable EFB Diagnostic Mode 1 Write to the EVENTMEM FIFO using the ROD Bus EFB Path, read back over the ROD Bus through the EVENTMEM path.			Enable	Disable
Bit 2: Enable EFB Diagnostic Mode 2 Trap Link Data in the EVENTMEM FIFO from normal EFB operation, read back over the ROD Bus through the EVENTMEM path.			Enable	Disable

Description	REG ID	Address	Access	Width
<b>EFB: Diagnostic Mode FIFO Select, EVT_MEM_CMND_STAT</b>	1AB	00402244	RW	7
Bits 0 to 2 cannot be turned on simultaneously.			<b>Bit Value</b>	
Bit 0: EVENTMEM FIFO A Select			1	0
Bit 1: EVENTMEM FIFO B Select			Select	Off
Bit 2: Header Trailer FIFO Select			Select	Off
Bit 3: Output 1 Event Fragment			Select	Off
Bit 4: Flag to indicate FIFO A Bus is Enabled			Enable	Disable
Bit 5: Flag to indicate FIFO B Bus is Enabled			Enable	Disable
Bit 6: Flag to indicate Event Header/Trailer Bus is enabled			Enable	Disable



## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>EFB: Event Memory FIFO Reset, EVT MEM RESET</b>	1AC	00402248	RW	1
When this bit is set, the EFB sends a reset pulse to the Event Memory FIFO. This bit is self-clearing, and cancels an ongoing play command.			<b>Bit Value</b>	
			1	0
<b>Bit 0:</b> Reset Event Memory FIFO			Reset	Ready

Description	REG ID	Address	Access	Width
<b>EFB: FIFO Status Flags, EVT MEM FLAGS</b>	1AD	0040224C	R	24
This register is used for diagnostics to check the EFB FIFO.			<b>Bit Value</b>	
			1	0
<b>Bit 0:</b> FIFO A Empty Status Flag			Empty	OK
<b>Bit 1:</b> FIFO A Almost Empty Status Flag			AEmpty	OK
<b>Bit 2:</b> FIFO A Almost Full Status Flag			AFull	OK
<b>Bit 3:</b> FIFO A Full Status Flag			Full	OK
<b>Bit 4:</b> FIFO B Empty Status Flag			Empty	OK
<b>Bit 5:</b> FIFO B Almost Empty Status Flag			AEmpty	OK
<b>Bit 6:</b> FIFO B Almost Full Status Flag			AFull	OK
<b>Bit 7:</b> FIFO B Full Status Flag			Full	OK
<b>Bit 8:</b> Header Trailer FIFO Empty Status Flag			Empty	OK
<b>Bit 9:</b> Header Trailer FIFO Full Status Flag			Full	OK
<b>Bit 10:</b> Event ID FIFO A Empty Status Flag			Empty	OK
<b>Bit 11:</b> Event ID FIFO A AlmostFull Status Flag			Full	OK
<b>Bit 12:</b> Event ID FIFO B Empty Status Flag			Empty	OK
<b>Bit 13:</b> Event ID FIFO B AlmostFull Status Flag			Full	OK
<b>Bit 14:</b> Header Event ID FIFO Empty Status Flag			Empty	OK
<b>Bit 15:</b> Header Event ID FIFO Almost Full Status Flag			AFull	OK
<b>Bit 16:</b> Header Event ID FIFO Full Status Flag			Full	OK
<b>Bit 17:</b> Event Data ID FIFO Empty Status Flag			Empty	OK
<b>Bit 18:</b> Event ID FIFO A FIFO Full Status Flag			Full	OK
<b>Bit 19:</b> Event ID FIFO B FIFO Full Status Flag			Full	OK
<b>Bit 20:</b> Word Count FIFO A Full Status Flag			Full	OK
<b>Bit 21:</b> Word Count FIFO B Full Status Flag			Full	OK
<b>Bit 22:</b> Error Summary FIFO A Full Status Flag			Full	OK
<b>Bit 23:</b> Error Summary FIFO B Full Status Flag			Full	OK

Description	REG ID	Address	Access	Width
<b>EFB: FIFO Input Data Word [15:0]</b>	ACCESS FIFO	00402250	RW	16
This is the low 16 bits of a word that is to be written into the Event Memory FIFO for diagnostics.			<b>Bit Value</b>	
<b>Bits[15:0]:</b> FIFO Input Data Word (15:0)			Value	

Description	REG ID	Address	Access	Width
<b>EFB: FIFO Input Data Word [31:16]</b>	ACCESS FIFO	00402254	RW	16
This is the middle 16 bits of a word that is to be written into the Event Memory FIFO for diagnostics.			<b>Bit Value</b>	
<b>Bits[15:0]:</b> FIFO Input Data Word (31:16)			Value	

Description	REG ID	Address	Access	Width
<b>EFB: FIFO Input Data Word [45:32]</b>	ACCESS FIFO	00402258	RW	14
This is the upper 14 bits of a word that is to be written into the Event Memory FIFO for diagnostics.			<b>Bit Value</b>	
<b>Bits[13:0]:</b> FIFO Input Data Word (45:32)			Value	

Description	REG ID	Address	Access	Width
<b>EFB: Write Word to Selected FIFO</b>	ACCESS FIFO	0040225C	RW	1
When this bit is set, the EFB sends a write pulse to the Event Memory FIFO. This bit is self-clearing.			<b>Bit Value</b>	
<b>Bit 0:</b> Write to Event Memory FIFO			1	0
			Write	Ready

Description	REG ID	Address	Access	Width
<b>EFB: Number of Words to Play-FIFO A, EVT MEM A WRD CNT</b>	1AE	00402260	RW	14
This value is used in diagnostics mode to indicate the number of words to be played from Event Memory FIFO A when simulated data has been written into the FIFO			<b>Bit Value</b>	
<b>Bits[13:0]:</b> Number of Words			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>EFB: Number of Words to Play-FIFO B, EVT MEM B WRD CNT</b>	1AF	00402264	RW	14
This value is used in diagnostics mode to indicate the number of words to be played from Event Memory FIFO B when simulated data has been written into the FIFO			Bit Value	
Bits[13:0]: Number of Words			Value	

Description	REG ID	Address	Access	Width
<b>EFB: Play Selected FIFO, EVT MEM PLAY EVENT</b>	1B0	00402268	RW	1
When this bit is set, the EFB sends a read pulse to the Event Memory FIFO. This bit will stay set until the Play Command is complete.			Bit Value	
Bit 0: Write to Event Memory FIFO			1	0
			Play	Idle

Description	REG ID	Address	Access	Width
<b>EFB: Diagnostic Status Register, EVT MEM STATUS</b>	1B1	0040226C	R	16
			Bit Value	
Bits[15:0]: Miscellaneous Status Bits			1	0

Description	REG ID	Address	Access	Width
<b>EFB: Send Empty Events,</b>		00402270	RW	1
When this bit is set, the EFB will flush the output and EVID data FIFOs and send a empty event fragment. This bit is self-clearing. Not Implemented yet			Bit Value	
Bit 0: Send Empty Events			1	0
			Send	Idle

Description	REG ID	Address	Access	Width
<b>EFB: L1ID/BCID TTC Trap Value</b>		0040227C	RW	1
The TTC values for BCID and L1ID when trapping Event ID data.			Bit Value	
			1	0
Bits[ 3: 0]: EFB Engine 0 - TTC L1ID			Value	
Bits[15: 8]: EFB Engine 0 - TTC BCID			Value	
Bits[19:16]: EFB Engine 1 - TTC L1ID			Value	
Bits[31:24]: EFB Engine 1 - TTC BCID			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>EFB: Link/Module L1ID/BCID Trap Value</b>			R	32
Link0/Link48 Trap Values		00402280		
Link1/Link49 Trap Values		00402284		
Link2/Link50 Trap Values		00402288		
Link3/Link51 Trap Values		0040228C		
Link4/Link52 Trap Values		00402290		
Link5/Link53 Trap Values		00402294		
Link6/Link54 Trap Values		00402298		
Link7/Link55 Trap Values		0040229C		
Link8/Link56 Trap Values		004022A0		
Link9/Link57 Trap Values		004022A4		
Link10/Link58 Trap Values		004022A8		
Link11/Link59 Trap Values		004022AC		
Link12/Link60 Trap Values		004022B0		
Link13/Link61 Trap Values		004022B4		
Link14/Link62 Trap Values		004022B8		
Link15/Link63 Trap Values		004022BC		
Link16/Link64 Trap Values		004022C0		
Link17/Link65 Trap Values		004022C4		
Link18/Link66 Trap Values		004022C8		
Link19/Link67 Trap Values		004022CC		
Link20/Link68 Trap Values		004022D0		
Link21/Link69 Trap Values		004022D4		
Link22/Link70 Trap Values		004022D8		
Link23/Link71 Trap Values		004022DC		
Link24/Link72 Trap Values		004022E0		
Link25/Link73 Trap Values		004022E4		
Link26/Link74 Trap Values		004022E8		
Link27/Link75 Trap Values		004022EC		
Link28/Link76 Trap Values		004022F0		
Link29/Link77 Trap Values		004022F4		
Link30/Link78 Trap Values		004022F8		
Link31/Link79 Trap Values		004022FC		
Link32/Link80 Trap Values		00402300		
Link33/Link81 Trap Values		00402304		
Link34/Link82 Trap Values		00402308		
Link35/Link83 Trap Values		0040230C		
Link36/Link84 Trap Values		00402310		
Link37/Link85 Trap Values		00402314		
Link38/Link86 Trap Values		00402318		
Link39/Link87 Trap Values		0040231C		
Link40/Link88 Trap Values		00402320		
Link41/Link89 Trap Values		00402324		
Link42/Link90 Trap Values		00402328		
Link43/Link91 Trap Values		0040232C		
Link44/Link92 Trap Values		00402330		
Link45/Link93 Trap Values		00402334		
Link46/Link94 Trap Values		00402338		
Link47/Link95 Trap Values		0040233C		
Event ID data value trap memory. The data field includes the L1ID and BCID values received from the module or chip and the expected L1ID value used in the error checking process. [n=0 to 47]			<b>Bit Value</b>	
			1	0
<b>Bits[ 3: 0] : Module/Chip L1ID - Link(n)</b>			Value	
<b>Bits[ 7: 4] : Expected Link L1ID - Link(n)</b>			Value	
<b>Bits[15: 8] : Module/Chip BCID - Link(n)</b>			Value	
<b>Bits[19:16] : Module/Chip L1ID - Link(n+48)</b>			Value	
<b>Bits[23:20] : Expected Link L1ID - Link(n+48)</b>			Value	
<b>Bits[31:24] : Module/Chip BCID - Link(n+48)</b>			Value	

# APPENDIX A: ROD and BOC FPGA Register Definitions

## 5 ROD Router FPGA Registers

### 5.1 DSP Trap Setup Registers

Description	REG ID	Address	Access	Width
Router: DSP0 Command Register0, RTR_TRAP_CMND_0(0)	1C2	00402400	RW	8
Router: DSP1 Command Register0, RTR_TRAP_CMND_0(1)	1C3	00402440	RW	8
Router: DSP2 Command Register0, RTR_TRAP_CMND_0(2)	1C4	00402480	RW	8
Router: DSP3 Command Register0, RTR_TRAP_CMND_0(3)	1C5	004024C0	RW	8
			<b>Bit Value</b>	
			<b>1</b>	<b>0</b>
<b>Bit 0:</b> Trap Atlas Specific Event Type			On	Off
<b>Bit 1:</b> Trap TIM Specific Event Type			On	Off
<b>Bit 2:</b> Trap ROD Specific Event Type			On	Off
<p><b>Bit 3:</b> Error Data Format (This bit is common to both Traps)</p> <p>Error Format: As the data comes into the router, six 32-bit words with 2 bits per link are built. The two bits encode the following cases:            00 = no data (the router did not get a header for this link)            01 = good data on the link, no errors            10 = bcid or llid error            11 = timeout error</p> <p>Three of these words overwrite the event fragment trailer words t2-t4. The other three are additional words that would be inserted before the E0F00000 word in the event fragment trailer.</p> <p>Event fragment header into the DSP            H0: 0xB0F00000            H1: 0xEE1234EE (start of header word)            H2: 0x00000006 (number of header words) H2            H3: L1ID (level 1 ID) -&gt; was H6 &lt;-            H4: BCID (bunch crossing ID) -&gt; was H7 &lt;-            H5: L1TT (level 1 trigger type) -&gt; was H8 &lt;-            H6: DET (detector event type) -&gt; was H9 &lt;-            --</p> <p>Event fragment trailer            T0: error count (status 1: count of words with errors)            T1: error flags (status 2: bitted error type occurrence word)            T2: error status for links 15 - 0 (link 0 bits are stored in bits 1 &amp; 0)            T3: error status for links 31 - 16            T4: error status for links 47 - 32            T5: error status for links 63 - 48            T6: error status for links 79 - 64            T7: error status for links 95 - 80            T8: 0xE0F00000</p>			Error Format	S-Link Format
<b>Bit 4:</b> Slink Data Format to the SDSP with the Error codes included in the Event Fragment Trailer.			On	Off
<b>Bit 5:</b> Trap All Events			On	Off
<p><b>Bit 6:</b> Set Trap into Data Driven Mode (This bit is common to both Traps)</p> <p>If this bit is set, the router writes Events into the Internal FIFO in consecutive order such that more than 1 Event can occupy the same Frame in the DSP memory. If this bit is cleared, only 1 event will be present in each frame or multiple consecutive groups of frames. A word count of the event is always written to the last memory location of last frame used for the specific event.</p>			On	Off
<b>Bit 7:</b> Trap All Error Events			On	Off
<b>Bit 8:</b> Trap Events that are larger than the Event Limit Threshold Event Limit Threshold value is set in EFB register 0x00402214			On	Off

Description	REG ID	Address	Access	Width
Router: DSP0 Command Register1, RTR_TRAP_CMND_1(0)	1C6	00402404	RW	7
Router: DSP1 Command Register1, RTR_TRAP_CMND_1(1)	1C7	00402444	RW	7
Router: DSP2 Command Register1, RTR_TRAP_CMND_1(2)	1C8	00402484	RW	7
Router: DSP3 Command Register1, RTR_TRAP_CMND_1(3)	1C9	004024C4	RW	7
			<b>Bit Value</b>	
			<b>1</b>	<b>0</b>
<b>Bit 0:</b> Trap Atlas Specific Event Type			On	Off
<b>Bit 1:</b> Trap TIM Specific Event Type			On	Off
<b>Bit 2:</b> Trap ROD Specific Event Type			On	Off

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Router: DSP0 Trap Reset/Load/Flush Reg, RTR_TRAP_RESET(0)	1CA	00402408	RW	4
Router: DSP1 Trap Reset/Load/Flush Reg, RTR_TRAP_RESET(1)	1CB	00402448	RW	4
Router: DSP2 Trap Reset/Load/Flush Reg, RTR_TRAP_RESET(2)	1CC	00402488	RW	4
Router: DSP3 Trap Reset/Load/Flush Reg, RTR_TRAP_RESET(3)	1CD	004024C8	RW	4
All bits in this Register are self-clearing			Bit Value	
			1	0
<b>Bit 0:</b> Reset Trap This bit resets both Traps for a specific DSP.			Reset	
<b>Bit 1:</b> Load New Trap0 Value This bit must be set to load new trap information for Trap0.			Load	
<b>Bit 2:</b> Load New Trap1 Value This bit must be set to load new trap information for Trap1.			Load	
<b>Bit 3:</b> Flush Trap FIFO This bit flushes the Trap FIFO for a specific DSP			Flush	

Description	REG ID	Address	Access	Width
Router: DSP0 Status Register, RTR_TRAP_STATUS(0)	1CE	0040240C	RW	9
Router: DSP1 Status Register, RTR_TRAP_STATUS(1)	1CF	0040244C	RW	9
Router: DSP2 Status Register, RTR_TRAP_STATUS(2)	1D0	0040248C	RW	9
Router: DSP3 Status Register, RTR_TRAP_STATUS(3)	1D1	004024CC	RW	9
			Bit Value	
			1	0
<b>Bit 0:</b> Trap Enable Control from DSP			Enabled	Idle
<b>Bit 1:</b> Interrupt Mask Control from DSP			Mask DFR Int	Allow DFR Int
<b>Bit 2:</b> Trapping FIFO Empty			Empty	Not Empty
<b>Bit 3:</b> Trapping FIFO Full			Full	Not Full
<b>Bit 4:</b> Trap0 - Trap match detected AND/OR Trapping Data			On	Off
<b>Bit 5:</b> Trap1 - Trap match detected AND/OR Trapping Data			On	Off
<b>Bit 6:</b> Trap0 Ready (Clears on WR to Cmd Reg0, Set on Load New Trap0)			Ready	Not Ready
<b>Bit 7:</b> Trap1 Ready (Clears on WR to Cmd Reg1, Set on Load New Trap1)			Ready	Not Ready
<b>Bit 8:</b> DSP0 SBSRAM Clock DLL Locked			Locked	Not Locked

Description	REG ID	Address	Access	Width
Router: DSP0 Trap Match Reg0, RTR_TRAP_MATCH_0(0)	1D2	00402410	RW	8
Router: DSP1 Trap Match Reg0, RTR_TRAP_MATCH_0(1)	1D3	00402450	RW	8
Router: DSP2 Trap Match Reg0, RTR_TRAP_MATCH_0(2)	1D4	00402490	RW	8
Router: DSP3 Trap Match Reg0, RTR_TRAP_MATCH_0(3)	1D5	004024D0	RW	8
			Bit Value	
<b>Bits[ 7:0]:</b> Trap Match value for DSP Command Reg0			Value	

Description	REG ID	Address	Access	Width
Router: DSP0 Pre-Scale Value Reg0, RTR_TRAP_MOD_0(0)	1D6	00402414	RW	16
Router: DSP1 Pre-Scale Value Reg0, RTR_TRAP_MOD_0(1)	1D7	00402454	RW	16
Router: DSP2 Pre-Scale Value Reg0, RTR_TRAP_MOD_0(2)	1D8	00402494	RW	16
Router: DSP3 Pre-Scale Value Reg0, RTR_TRAP_MOD_0(3)	1D9	004024D4	RW	16
If Trap Match Scale = 0, trap 1 event only If Trap Match Scale = 1, trap all events that match the Trap Match value If Trap Match Scale > 1, trap all events that meet the following. Trap Match is true (Increment Trap Match Count), AND Trap Match Count = Trap Match Remainder (Scale=Period) EXPLAIN REMAINDER FUNCTION			Bit Value	
<b>Bits[ 7:0]:</b> Trap Match Scale for Trap 0			Value	
<b>Bits[15:8]:</b> Trap Match Remainder for Trap0			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Router: DSP0 Trap Match Reg1, RTR_TRAP_MATCH_1(0)	1DA	00402418	RW	8
Router: DSP1 Trap Match Reg1, RTR_TRAP_MATCH_1(1)	1DB	00402458	RW	8
Router: DSP2 Trap Match Reg1, RTR_TRAP_MATCH_1(2)	1DC	00402498	RW	8
Router: DSP3 Trap Match Reg1, RTR_TRAP_MATCH_1(3)	1DD	004024D8	RW	8
				Bit Value
Bits[ 7:0]: Trap Match value for DSP Command Reg1				Value

Description	REG ID	Address	Access	Width
Router: DSP0 Pre-Scale Value Reg1, RTR_TRAP_MOD_1(0)	1DE	0040241C	RW	16
Router: DSP1 Pre-Scale Value Reg1, RTR_TRAP_MOD_1(1)	1DF	0040245C	RW	16
Router: DSP2 Pre-Scale Value Reg1, RTR_TRAP_MOD_1(2)	1E0	0040249C	RW	16
Router: DSP3 Pre-Scale Value Reg1, RTR_TRAP_MOD_1(3)	1E1	004024DC	RW	16
If Trap Match Scale = 0, trap 1 event only If Trap Match Scale = 1, trap all events that match the Trap Match value If Trap Match Scale > 1, trap all events that meet the following. Trap Match is true (Increment Trap Match Count), AND Trap Match Count = Trap Match Remainder (Scale=Period)				Bit Value
Bits[ 7:0]: Trap Match Scale for Trap 1				Value
Bits[15:8]: Trap Match Remainder for Trap1				Value

Description	REG ID	Address	Access	Width
Router: DSP0 FIFO Word Count, RTR_TRAP_FIFO_WRD_CNT(0)	1E6	00402424	R	10
Router: DSP1 FIFO Word Count, RTR_TRAP_FIFO_WRD_CNT(1)	1E7	00402464	R	10
Router: DSP2 FIFO Word Count, RTR_TRAP_FIFO_WRD_CNT(2)	1E8	004024A4	R	10
Router: DSP3 FIFO Word Count, RTR_TRAP_FIFO_WRD_CNT(3)	1E9	004024E4	R	10
				Bit Value
Bits[ 9: 0]: Internal FIFO Word Count				Value
Bits[15:12]: Data Frame Ready State Machine Status				Value
State		Value		
Reset	0x0			
Idle	0x1			
Re-Test Occupancy	0x2			
Issue Frame Ready Interrupt	0x3			
Wait for ISR handshake	0x4			
ISR Done	0x5			
Decrement Block Count	0x6			
Mask Interrupt Request	0x7			

Description	REG ID	Address	Access	Width
Router: DSP0 Interrupt Mask Delay Count RTR_TRAP_INT_DELAY_CNT(0)	1F2	00402430	RW	6
Router: DSP1 Interrupt Mask Delay Count RTR_TRAP_INT_DELAY_CNT(1)	1F3	00402470	RW	6
Router: DSP2 Interrupt Mask Delay Count RTR_TRAP_INT_DELAY_CNT(2)	1F4	004024B0	RW	6
Router: DSP3 Interrupt Mask Delay Count RTR_TRAP_INT_DELAY_CNT(3)	1F5	004024F0	RW	6
This value is used to prevent the Router from issuing interrupts before the Slave DSP has finished exiting its ISR.				Bit Value
Bits[ 5:0]: Interrupt Mask Delay Count Value				1      0
				Value

Description	REG ID	Address	Access	Width
Router: DSP0 Interrupt 4 Period (Diagnostic Reg)		00402434	RW	16
Router: DSP1 Interrupt 4 Period (Diagnostic Reg)		00402474	RW	16
Router: DSP2 Interrupt 4 Period (Diagnostic Reg)		004024B4	RW	16
Router: DSP3 Interrupt 4 Period (Diagnostic Reg)		004024F4	RW	16
This value is used to set the period of DSP INT4 pulses sent to the Slave DSPs. If this value is 0, no interrupts will be sent. If the value is equal to 1, the RTR will set the Int4 signal to value = 1. The output signal is not gated by the mask interrupt function, so the user must check that the DSP is ready to accept an interrupt before generating the pulse. If the value is greater than 1, the period of the pulse train will be equal to the register value multiplied by 100ns.				Bit Value
Bits[15:0]: Interrupt 4 Period Count Value				1      0
				Value

## APPENDIX A: ROD and BOC FPGA Register Definitions

### 5.2 Router Slink Command and Status Registers

Description	REG ID	Address	Access	Width
Router: Command/Status Register, RTR_CMND_STAT	202	00402500	RW	16
			Bit Value	
			1	0
<b>Bit 0:</b> Dump Atlas Specific Event Type			On	Off
<b>Bit 1:</b> Dump TIM Specific Event Type			On	Off
<b>Bit 2:</b> Dump ROD Specific Event Type			On	Off
<b>Bit 3:</b> Inhibit S-Link Write Enable This bit allows the user to block writes to the S-Link. Slink Xoff is ignored is this bit is set to value = 1.			Inhibit	Allow
<b>Bit 4:</b> Reset S-Link			Reset	Ready
<b>Bit 5:</b> Set S-Link Test Bit			Test	Normal
<b>Bit 6:</b> Enable Calibration Back Pressure to EFB This bit can only be used in Calibration and Configuration			Enable	Disable
<b>Bit 7:</b> Mask LDOWN# Bit (Allow data transmission when S-Link is down)			Mask	Normal
<b>Bit 8:</b> S-Link Xoff Status (Read Only)			Xoff	Xon
<b>Bit 9:</b> S-Link LDown Status (Read Only)			LDown	OK
<b>Bit 10:</b> Stop Output (Back pressure to the EFB) (Read Only)			Stop EFB	OK
<b>Bit 11:</b> 40MHz Clock DLL Locked (Read Only)			Locked	Error
<b>Bit 12:</b> 80MHz Clock DLL Locked (Read Only)			Locked	Error
<b>Bit 13:</b> S-Link Xoff Status Latched (Read Only)			Xoff	OK
<b>Bit 14:</b> S-Link Endianness Bit (SCT Only)			LE	BE
<b>Bit 15:</b> Not Used				

Description	REG ID	Address	Access	Width
Router: S-Link Atlas/TIM Event Type Dump Match Register RTR_SLNK_ATLAS_DUMP_MATCH	203	00402504	RW	10
			Bit Value	
<b>Bits[ 7:0]:</b> Atlas Specific Event Type			Value	
<b>Bits[ 9:8]:</b> TIM Specific Event Type			Value	

Description	REG ID	Address	Access	Width
Router: S-Link ROD Specific Dump Match Register RTR_SLNK_ATLAS_DUMP_MATCH	204	00402508	RW	6
			Bit Value	
<b>Bits[ 5:0]:</b> ROD Specific Event Type			Value	

Description	REG ID	Address	Access	Width
Router: Code Version - RTR_CODE_VERSION	205	0040250C	RW	16
			Bit Value	
<b>Bits[ 7:0]:</b> Code Version			Value	
<b>Bits[14:8]:</b> Board Revision of Code			Value	
<b>Bit[15]:</b> ROD Type			Pixel	SCT

Description	REG ID	Address	Access	Width
Router: Test Output Mux Register - RTR_OUTPUT_SIGNAL_MUX	206	00402510	RW	4
Selects the group of test outputs for the Router			Bit Value	
<b>Bits[ 3:0]:</b> Test Output Mux Value			Value	
<b>Bits[15:4]:</b> Not Used				

Description	REG ID	Address	Access	Width
Router: Xoff Counter Register - RTR_XOFF_COUNT	207	00402514	R	16
Indicates the number of times that Xoff has been asserted. Self clears when it is read.			Bit Value	
<b>Bits[15:0]:</b> Xoff Counter Value			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>Router: S-Link FIFO Status - RTR_SLFIFO_STAT</b>		00402518	R	3
Indicates the occupancy status of the S-Link pipeline FIFO at the output of the Router.			<b>Bit Value</b>	
			1	0
<b>Bit[0]:</b> S-Link FIFO Empty			EMPTY	
<b>Bit[1]:</b> S-Link FIFO Almost Full			AFULL	
<b>Bit[2]:</b> S-Link FIFO Full			FULL	

Description	REG ID	Address	Access	Width
<b>Router: Next Event Delay Count Register - RTR_NEXT_EVT_DELAY_COUNT</b>		0040251C	R	16
To prevent events overlap in calibration mode when multiple group are configured, the B0F and EOF words need to be separated by multiple system clocks. This register allow the user to adjust the time between the end of one event and the star of another for calibration type data runs. The default value is 0x8 (200ns). This function of the register is only active when the Calibration back pressure bit on the Router is valid.			<b>Bit Value</b>	
<b>Bits[15:0]:</b> Next Event Delay Count			Value	



# APPENDIX A: ROD and BOC FPGA Register Definitions

## 6 ROD Controller FPGA Registers

### 6.1 ROD Controller Command, Status and Mode Registers

Description	REG ID	Address	Access	Width
ROD Controller: Master DSP General Purpose Register	1C5	00404400	RW	2
			Bit Value	
			1	0

Description	REG ID	Address	Access	Width
ROD Controller: General Purpose Diagnostics Register		00404404	R	32
			Bit Value	
TBD			Value	

Description	REG ID	Address	Access	Width
ROD Controller: HPI Time Out Counter:		00404408	RW	32
			Bit Value	
Bits[31:0]: HPI Time Out Counter Value			Value	

Description	REG ID	Address	Access	Width
ROD Controller: Code Version and ROD Board Revision: RRIF_CODE_VERSION	216	0040440C	RW	16
			Bit Value	
Bits[ 7:0]: Code Version Number			Value	
Bits[15:8]: ROD Board Revision Number			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
ROD Controller: Main Control Register, RRIF_CMND_1	217	00404410	RW	32
			Bit Value	
			1	0
<b>Bit 0:</b> Enable/Disable FE Command Output Data Streams			On	Off
<b>Bit 1:</b> Select FE Command Input Source for Mask0			TIM	DSP SFO
<b>Bit 2:</b> FE Command Mask, "New Mask Ready Bit" (Self Clearing) In Normal Data Taking Mode, when a new FE Command Link Mask has been written to the RCF from the MDSP, this bit must be set to allow the next L1A to use the new mask. If the RRIF_CMND_1, Bit(20) is set, the new mask will be loaded when this bit is set.			Ready	Idle
<b>Bit 3:</b> FE Occupancy Counter Enable, Read Link Trailers			Enable	Reset
<b>Bit 4:</b> NOT USED				
<b>Bit 5:</b> FE Command Pulse Counter Enable When enabled, all L1 Triggers sent to the ROD will increment this counter, and a Command Cycle will be initiated. When a Command Cycle has been completed (Mode bits and Token to the Formatters, and Dynamic Mask to the EFB) the counter will be decremented.			Enable	Reset
<b>Bit 6:</b> FE Command Pulse Counter Load Loads maximum value into the FE Command Pulse Counter. This is a function that is used for diagnostic test only.			Load	Idle
<b>Bit 7:</b> NOT USED				
<b>Bit 8:</b> Trigger Signal Decoder Enable Enable for TIM/TTC serial data decoders.			Enable	Reset
<b>Bit 9:</b> NOT USED				
<b>Bit 10:</b> Formatter Mode Bits Encoder Enable Enable for the block that writes Dynamic Mode Bit data to the Formatters for each L1 Trigger			Enable	Reset
<b>Bit 11:</b> NOT USED				
<b>Bit 12:</b> EFB Dynamic Mask Encoder Enable Enable for the block that writes the Event ID and Dynamic Mask Bit data to the EFB for each L1 Trigger			Enable	Reset
<b>Bit 13:</b> NOT USED				
<b>Bit 14:</b> NOT USED				
<b>Bit 15:</b> NOT USED				
<b>Bit 16:</b> Test Bench I/O Enable Enable for the Internal Test Bench Block used for stand-alone testing of the ROD. The Debug-Mode Configuration Registers are used to configure different tests on the ROD.			Enable	Reset
<b>Bit 17:</b> Test Bench I/O Run This bit starts the ROD test, and must be cleared by the host when the test is finished. See the Debug-Mode Status Register definitions for more information			Run	Idle
<b>Bit 18:</b> Calibration Trigger Signal Decoder Enable This bit selects the ROD Register Calibration Parameters to be used for the testing of Data Taking Modes and calibration and enables the RCF block that detects Command types from the Serial Port Inputs.			Enable	Idle
<b>Bit 19:</b> Configuration Read back Enable This bit enables the trapping of data on the input links to the ROD into the Input Memory FIFO.			Enable	Idle
<b>Bit 20:</b> Configuration/Calibration Mask Load Enable This bit allows a new FE Command mask to be loaded when the ROD is configuring Modules or is in Calibration Mode			Enable Load	Idle
<b>Bit 21:</b> Static Calibration BCID Enable This bit selects between the value for the BCID used during calibration			Static BCID	Dynamic BCID
<b>Bit 22:</b> Static Calibration L1ID Enable This bit selects between the value for the L1ID used during calibration			Static L1ID	Dynamic L1ID
<b>Bit 23:</b> Corrective Mode Bits and Dynamic Mask Ready (Self Clearing) This bit indicates that corrective Mode Bits and Dynamic Mask bits have been set and are ready to transmit when the next L1A is detected.			Mask Ready	Idle
<b>Bit 24:</b> Input Memory FIFO Playback Inhibit			Inhibit	Play
<b>Bit 25:</b> Control Signal Mux(0)			See "Modes of Operation" Table	
<b>Bit 26:</b> Control Signal Mux(1)				
<b>Bit 27:</b> Control Signal Mux(2)				
<b>Bit 28:</b> Control Signal Mux(3)				
<b>Bit 29:</b> Start Internal Scan Engine (WR protected for SCT ROD)			Start	Stop
<b>Bit 30:</b> Clear Internal Scan Engine nEvent Counters			Clear	Idle
<b>Bit 31:</b> Not Used				

## APPENDIX A: ROD and BOC FPGA Register Definitions

Control Signal Mux Value <b>Bits[28:25]</b>	Modes of Operation
"0000"	Disable FE Inputs
"0001"	Connect the RCF FIFO Interface Control Signals to the Diagnostic FIFOs This mode is used to Load and Read the FIFOs with MDSP control
"0010"	Connect FE Input Control to the Test Bench Interface Control Signals
"0011"	Not Used - Disable FE Inputs
"0100"	Enable the normal data Path
"0101"	Connect FE Input control for Configuration Readback Mode
"0110"	Connect FE Input control for Calibration Test Mode
"0111"	Route the input link data to the InMems and Formatters
"1000"- "1111"	Not Used - Disable FE Inputs

Description	REG ID	Address	Access	Width
<b>ROD Controller: Spare Control Register, RRIF_CMND_0</b>	218	00404414	RW	13
			<b>Bit Value</b>	
			1	0
<b>Bit 0:</b> Formatter A Mode Bits FIFO Reset (default: '0', '1' self clearing)			Reset	Ready
<b>Bit 1:</b> Formatter B Mode Bits FIFO Reset (default: '0', '1' self clearing)			Reset	Ready
<b>Bit 2:</b> EFB Dynamic Mask Bits FIFO Reset (default: '0', '1' self clearing)			Reset	Ready
<b>Bit 3:</b> INMEM FIFO Reset			Reset	Ready
<b>Bit 4:</b> Not Used				
<b>Bit 5:</b> Not Used				
<b>Bit 6:</b> Internal TIM FIFO Reset			Reset	Ready
<b>Bit 7:</b> Corrective Trigger FIFO Reset			Reset	Ready
<b>Bit 8:</b> Internal TIM FIFO Re-Transmit (default: '0', '1' self clearing)			Re-Tx	Idle
<b>Bit 9:</b> INMEM FIFO Re-Transmit (default: '0', '1' self clearing)			Re-Tx	Idle
<b>Bit 10:</b> Diagnostic EFB Generated ROD Busy			Enable	Disable
<b>Bit 11:</b> Diagnostic Event Counters			Enable	Reset
<b>Bit 12:</b> ECR ID Counter Reset			Reset	Idle
<b>Bits [17:13]:</b> SP1 Frame Sync Offset If Offset Value = 0, the frame sync pulse to SP0 and SP1 will occur on the same clock edge. If Offset Value = n, the Frame Sync pulse to SP1 will occur n system clocks after the Frame Sync pulse for SP0.			Offset Value	
<b>Bit 18:</b> FSX CLKX Output Enable This bit allows the RCF FSX and CLKX outputs to be set to High Z.			On	Off
<b>Bit 19:</b> SP0 Input Mask			Mask	On
<b>Bit 20:</b> SP1 Input Mask			Mask	On
<b>Bits[24:21]:</b> Not Used				
<b>Bit 25:</b> MDSP Tout Enable			On	Off
<b>Bit 26:</b> MDSP INT4 Enable			On	Off
<b>Bit 27:</b> MDSP INT5 Enable			On	Off
<b>Bit 28:</b> MDSP INT6 Enable			On	Off
<b>Bit 29:</b> MDSP INT7 Enable			On	Off
<b>Bit 30:</b> SDSP Interrupt Enable (All Slaves)			On	Off
<b>Bit 31:</b> VME Interrupt Enable			On	Off

Description	REG ID	Address	Access	Width
<b>ROD Controller: Mode Register, ROD_MODE_REG</b>	219	00404418	RW	4
<b>Bits[3:0]:</b> ROD Controller Modes. The ROD Controller Mode is controlled by the MDSP. This register does not cause any function to occur on the ROD.			<b>Bit Value</b>	

Description	REG ID	Address	Access	Width
<b>ROD Controller: FE Mask LUT Select, FE_MASK_LUT_SELECT</b>	21A	0040441C	RW	3
			<b>Bit Value</b>	
<b>Bits[ 2:0]:</b> FE Mask Select			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
ROD Controller: Main Status Register, RRIF_STATUS_1	21B	00404420	R	32
			Bit Value	
			1	0
Bit 0: TIM Clock OK			OK	Fail
Bit 1: BOC Clock OK			OK	Fail
Bit 2: BOC Busy			Busy	Ready
Bit 3: Configuration Read Back Done/Trap Link Data Done			Done	Ready
Bit 4: Cal Test Ready			Ready	Running
Bit 5: FE Trigger FIFO Empty Flag			Empty	Not
Bit 6: FE Trigger FIFO Full Flag			Full	Not
Bit 7: Formatter A, EFB Stop Output			Stop Tx	TX OK
Bit 8: Formatter A Mode Bits FIFO Full Flag			Full	Not
Bit 9: Formatter B EFB Stop Output			Stop Tx	TX OK
Bit 10: Formatter B Mode Bits FIFO Full Flag			Full	Not
Bit 11: Header/Trailer Limit Formatter Bank A			Limit	OK
Bit 12: Header/Trailer Limit Formatter Bank B			Limit	OK
Bit 13: ROD Busy Limit Formatter Bank A			Busy	OK
Bit 14: ROD Busy Limit Formatter Bank B			Busy	OK
Bit 15: EFB Dynamic Mask Bits FIFO Empty Flag			Empty	Not
Bit 16: EFB Dynamic Mask Bits FIFO Full Flag			Full	Not
Bit 17: EFB Event ID Empty Error If this bit is set, the data from the Formatters has arrived at the EFB before the ID information was ready for the building of the event. This is a fatal error that requires a soft reset for recovery.			Error	OK
Bit 18: Event Memory A FIFO Empty Flag			Empty	Not
Bit 19: Event Memory A FIFO Full Flag			Full	Not
Bit 20: Event Memory B FIFO Empty Flag			Empty	Not
Bit 21: Event Memory B FIFO Full Flag			Full	Not
Bits[29:22]: FE Command Pulse Counter			Count	
Bit 30: FE Occupancy Counters All Zero			All Zero	> Zero
Bit 31: Command Mask Ready			Ready	Not

Description	REG ID	Address	Access	Width
ROD Controller: Spare Status Register, RRIF_STATUS_0	21C	00404424	R	32
			Bit Value	
Bits [ 7:0]: TTC line Monitor			Value	
Bits [18:8]: Trigger Counter Value			Count	
Bit 19: External Interrupt Ack Num Input 0			Ack	Clear
Bit 20: External Interrupt Ack Num Input 1			Ack	Clear
Bit 21: External Interrupt Ack Num Input 2			Ack	Clear
Bit 22: External Interrupt Ack Num Input 3			Ack	Clear
Bit 23: External Interrupt Ack Num Input 4			Ack	Clear
Bit 24: RCF DLL Locked			Locked	Not
Bit 25: S-Link Xoff			Xoff	OK
Bit 26: S-Link Down or not Installed			Down	OK
Bit 27: Slave DSP0 Detect Input			Present	Not
Bit 28: Slave DSP1 Detect Input			Present	Not
Bit 29: Slave DSP2 Detect Input			Present	Not
Bit 30: Slave DSP3 Detect Input			Present	Not
Bit 31: ROD Type from EFB			Pixel	SCT



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## 6.2 ROD Controller FE Command Stream Mask Registers

Description	REG ID	Address	Access	Width
<b>ROD Controller: FE Command Link Mask0_LO Register</b> <b>FE_CMND_MASK_0_LO</b>	21F	00404430	RW	32
Mask for Data Streams 0 to 31. This Mask applies to the Serial Data Streams generated by the TIM or MDSP SP0.			<b>Bit Value</b>	
			1	0
<b>Bits [31:0]:</b> FE Command Link 0 to 31 Mask Bit 0 sets the mask for Link 0, bit 1 for link 1, up to bit 31 for link 31. To load the mask, the "New Mask Ready" bit must be set in the Main Control Register after the mask value has been written to this register. If the ROD is in Normal Data Taking Mode, the Mask will be loaded when the next L1 Trigger is received from the TIM. If the "Config/Cal Mask Load Enable" bit is set in the Main Control Register, the mask will be loaded when the "New Mask Ready" bit is set.			Enable Output	Mask Output

Description	REG ID	Address	Access	Width
<b>ROD Controller: FE Command Link Mask0_HI Register</b> <b>FE_CMND_MASK_0_HI</b>	220	00404434	RW	16
Mask for Data Streams 32 to 47. This Mask applies to the Serial Data Streams generated by the TIM or MDSP SP0.			<b>Bit Value</b>	
			1	0
<b>Bits [31:0]:</b> FE Command Link 32 to 47 Mask Bit 0 sets the mask for Link 32, bit 1 for link 37, up to bit 15 for link 47. To load the mask, the "New Mask Ready" bit must be set in the Main Control Register after the mask value has been written to this register. If the ROD is in Normal Data Taking Mode, the Mask will be loaded when the next L1 Trigger is received from the TIM. If the "Config/Cal Mask Load Enable" bit is set in the Main Control Register, the mask will be loaded when the "New Mask Ready" bit is set.			Enable Output	Mask Output

Description	REG ID	Address	Access	Width
<b>ROD Controller: FE Command Link Mask1_LO Register</b> <b>FE_CMND_MASK_1_LO</b>	221	00404438	RW	32
Mask for Data Streams 0 to 31. This Mask applies to the Serial Data Streams generated by MDSP SP1.			<b>Bit Value</b>	
			1	0
<b>Bits [31:0]:</b> FE Command Link 0 to 31 Mask Bit 0 sets the mask for Link 0, bit 1 for link 1, up to bit 31 for link 31. To load the mask, the "New Mask Ready" bit must be set in the Main Control Register after the mask value has been written to this register. If the ROD is in Normal Data Taking Mode, the Mask will be loaded when the next L1 Trigger is received from the TIM. If the "Config/Cal Mask Load Enable" bit is set in the Main Control Register, the mask will be loaded when the "New Mask Ready" bit is set.			Enable Output	Mask Output

Description	REG ID	Address	Access	Width
<b>ROD Controller: FE Command Link Mask1_HI Register</b> <b>FE_CMND_MASK_1_HI</b>	222	0040443C	RW	16
Mask for Data Streams 32 to 47. This Mask applies to the Serial Data Streams generated by MDSP SP1.			<b>Bit Value</b>	
			1	0
<b>Bits [31:0]:</b> FE Command Link 32 to 47 Mask Bit 0 sets the mask for Link 32, bit 1 for link 37, up to bit 15 for link 47. To load the mask, the "New Mask Ready" bit must be set in the Main Control Register after the mask value has been written to this register. If the ROD is in Normal Data Taking Mode, the Mask will be loaded when the next L1 Trigger is received from the TIM. If the "Config/Cal Mask Load Enable" bit is set in the Main Control Register, the mask will be loaded when the "New Mask Ready" bit is set.			Enable Output	Mask Output

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### 6.3 ROD Controller Calibration Command Registers

Description	REG ID	Address	Access	Width
ROD Controller: Calibration Strobe Delay Register <b>CALSTROBE_DELAY</b>	223	00404440	RW	8
Sets the amount of delay in 25ns increments that will be inserted before sending the contents of the Cal Command Register after receiving a Cal Strobe from the TIM			Bit Value	
Bits [7:0]: Calibration Strobe Delay			Count	

Description	REG ID	Address	Access	Width
ROD Controller: Calibration Command Data Register <b>CAL_CMND</b>	224	00404444	RW	26
Sets the Calibration Command Serial Data Stream to be sent after receiving a Cal Strobe from the TIM. <b>SCT ONLY</b>			Bit Value	
Bits [25:0]: Calibration Command Data			Value	

Description	REG ID	Address	Access	Width
ROD Controller: ECR Counter Register <b>ECR_COUNTER_VAL</b>	225	00404448	RW	8
Used to set the required ECR Counter value.			Bit Value	
Bits [7:0]: Initial ECR Value			Value	

Description	REG ID	Address	Access	Width
ROD Controller: ECR Counter Register <b>ECR_COUNTER_STAT</b>	226	0040444C	RW	8
ECR Counter Value Monitor.			Bit Value	
Bits [7:0]: Current ECR Value			Value	

### 6.4 ROD Controller Mode Bits and Dynamic Mask Status Registers

Description	REG ID	Address	Access	Width
ROD Controller: Formatter Mode Bits FIFO Status Reg <b>FRMT_RMB_STATUS</b>	227	00404450	R	32
			Bit Value	
			1	0
Bit 0: Internal Formatter A Mode Bits FIFO Empty Flag			Empty	OK
Bit 1: Internal Formatter A Mode Bits FIFO Full Flag			Full	OK
Bits [9:2]: Internal Formatter A Mode Bits Occupancy Count			Count	
Bits [15:10]: Not Used				
Bit 16: Internal Formatter B Mode Bits FIFO Empty Flag			Empty	OK
Bit 17: Internal Formatter B Mode Bits FIFO Full Flag			Full	OK
Bits [25:18]: Internal Formatter B Mode Bits Occupancy Count			Count	
Bits [31:26]: Not Used				

Description	REG ID	Address	Access	Width
ROD Controller: EFB Dynamic Mask FIFO Flags Status Reg <b>EFB_DM_FIFO_FLAG_STA</b>	229	00404458	R	32
			Bit Value	
			1	0
Bit 0: Internal L1ID/BCID FIFO Empty Flag			Empty	OK
Bit 1: Internal Trigger Type FIFO Empty Flag			Empty	OK
Bit 2: Internal L1ID/BCID/TT FIFO Empty Flag			Empty	OK
Bit 3: Internal Default Dynamic Mask FIFO Empty Flag			Empty	OK
Bit 4: Internal Corrective Dynamic Mask FIFO Empty Flag			Empty	OK
Bits[7:5]: Not Used				
Bit 8: Internal L1ID/BCID FIFO Full Flag			Full	OK
Bit 9: Internal Trigger Type FIFO Full Flag			Full	OK
Bit 10: Internal L1ID/BCID/TT FIFO Full Flag			Full	OK
Bit 11: Internal Default Dynamic Mask FIFO Full Flag			Full	OK
Bit 12: Internal Corrective Dynamic Mask FIFO Full Flag			Full	OK
Bits[31:13]: Not Used				

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Description	REG ID	Address	Access	Width
<b>ROD Controller: EFB Dynamic Mask FIFO Word Count Reg</b> <b>EFB DM WC STA REG</b>	22A	0040445C	R	32
Word Count Status for all of the FIFO used in the EFB Dynamic Mask Encoder Block of the Controller FPGA.			<b>Bit Value</b>	
			1	0
<b>Bits[ 6: 0]:</b> Internal L1ID/BCID FIFO Count			Count	
<b>Bits[14: 8]:</b> Internal Trigger Type FIFO Count			Count	
<b>Bits[22:16]:</b> Internal Event Mask FIFO Count			Count	
<b>Bits[30:24]:</b> Internal Event Header FIFO Count			Count	

### 6.5 ROD Controller Diagnostic Counters Command and Status Registers

Description	REG ID	Address	Access	Width
<b>ROD Controller: Inmem A/B Count Register, INP MEM CTRL</b>	22B	00404460	RW	32
The ROD Controller Test Bench Block uses these counter registers. See the section that describes the Test Bench Modes to see the definitions for each of the registers. Each increment in value is equal to 25ns.			<b>Bit Value</b>	
<b>Bits[15: 0]:</b> Inmem A Count Value			Count	
<b>Bits[31:16]:</b> Inmem B Count Value			Count	

Description	REG ID	Address	Access	Width
<b>ROD Controller: DEBUGMEM A/B Count Register, DBG MEM CTRL</b>	22C	00404464	RW	32
The ROD Controller Test Bench Block uses these counter registers. See the section that describes the Test Bench Modes to see the definitions for each of the registers. Each increment in value is equal to 25ns.			<b>Bit Value</b>	
<b>Bits[15: 0]:</b> DEBUGMEM A Count Value			Count	
<b>Bits[31:16]:</b> DEBUGMEM B Count Value			Count	

Description	REG ID	Address	Access	Width
<b>ROD Controller: Configuration Readback Count Register</b> <b>CFG_READBACK_CNT</b>	22D	00404468	RW	32
The ROD Controller uses these counter registers to set the parameters used when configuration data is being read back from the modules. Each increment in value is equal to 25ns.			<b>Bit Value</b>	
<b>Bits[15: 0]:</b> Write FIFO Count Value This value sets the length of time that the FIFO will be trapping data.			Count	
<b>Bits[31:16]:</b> Delay FIFO Write Count Value This value sets the length of delay from the time that the "Configuration ReadBack" bit (Bit 19, Register 0x00404410) is set to when Write Enable is active on the Input Memory FIFO.			Count	



## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
<b>ROD Controller: Debug Mode Configuration Register</b> IDE_MEM_CTRL	22F	00404470	RW	32
			<b>Bit Value</b>	
			1	0
<b>Bit 0:</b> External Control, INMEM A Count Enable			Enable	Idle
<b>Bit 1:</b> External Control, INMEM A Count Load			Load	Idle
<b>Bit 2:</b> External Control, INMEM B Count Enable			Enable	Idle
<b>Bit 3:</b> External Control, INMEM B Count Load			Load	Idle
<b>Bit 4:</b> External Control, DEBUGMEM A Count Enable			Enable	Idle
<b>Bit 5:</b> External Control, DEBUGMEM A Count Load			Load	Idle
<b>Bit 6:</b> External Control, DEBUGMEM B Count Enable			Enable	Idle
<b>Bit 7:</b> External Control, DEBUGMEM B Count Load			Load	Idle
<b>Bit 8:</b> External Control, CNFGRDBACK Write Count Enable			Enable	Idle
<b>Bit 9:</b> External Control, CNFGRDBACK Write Count Load			Load	Idle
<b>Bit 10:</b> External Control, CNFGRDBACK Delay Count Enable			Enable	Idle
<b>Bit 11:</b> External Control, CNFGRDBACK Delay Count Load			Load	Idle
<b>Bits[17:12]:</b> Test Bench Mode Select				
INMEM->Formatters->EFB->Router->SDSP			1	0 0 0 0 0
INMEM A Word Count: Number of Words to play out of the FIFO				
INMEM->Formatters->EFB->Router->SDSP with retransmit			1	0 0 1 0 0
INMEM A Word Count: Number of Words to play out of the FIFO				
INMEM B Word Count: Numbers of Retransmits				
<b>Bits[23:20]:</b> ROL Test Block Control				
SETUP step                      OPERATION/RUN                      RESET/STOP				
Send Repeat Events - Bits[23:21] = 0x0; Set Bit 20 = 0x1; Clear Bit 20				
Send Single Event - Bits[23:21] = 0x1; Set Bit 20 = 0x1; Clear Bit 20				
Send TIM Events - Bits[23:21] = 0x2; Set Bit 20 = 0x1; Clear Bit 20				
Send n Events - Bits[23:21] = 0x4; Set Bit 20 = 0x1; Clear Bit 20, Status=Bit15, IDE_MEM_STAT n = Bits[23:0], DBG_MEM_CTRL				
The setup step must be done before the ROL Start bit is set				
<b>Bit 20:</b> Start ROL Test			Start	Idle
<b>Bit 21:</b> Send Single Event			Single	Repeat
<b>Bit 22:</b> Send ROL Test Block with L1A			Send	Idle
<b>Bit 23:</b> Enable ROL Trigger Counter (0x00404464 - DBG_MEM_CTRL: 22C)			Enable	Idle
<b>Bits [29:24]:</b> ROL Test Block Multiplier			Value	

Description	REG ID	Address	Access	Width
<b>ROD Controller: Debug Mode Status Register</b> IDE_MEM_STAT	230	00404474	R	32
			<b>Bit Value</b>	
			1	0
<b>Bit 0:</b> INMEM A Count Done			Done	Idle
<b>Bit 1:</b> INMEM B Count Done			Done	Idle
<b>Bit 2:</b> DEBUGMEM A Count Done			Done	Idle
<b>Bit 3:</b> DEBUGMEM B Count Done			Done	Idle
<b>Bit 4:</b> CNFGRDBACK Write Count Done			Done	Idle
<b>Bit 5:</b> CNFGRDBACK Delay Count Done			Done	Idle
<b>Bit 6:</b> Test Bench OP0 Status Bit			Done	Idle
<b>Bit 7:</b> Test Bench OP1 Status Bit			Done	Idle
<b>Bit 8:</b> Input Memory A FIFO Empty Flag			Empty	OK
<b>Bit 9:</b> Input Memory A FIFO Full Flag			Full	OK
<b>Bit 10:</b> Input Memory B FIFO Empty Flag			Empty	OK
<b>Bit 11:</b> Input Memory B FIFO Full Flag			Full	OK
<b>Bit 12:</b> NOT USED			Empty	OK
<b>Bit 13:</b> NOT USED			Full	OK
<b>Bit 14:</b> NOT USED			Empty	OK
<b>Bit 15:</b> ROL Test Triggers Active			Active	Idle
<b>Bit 16:</b> Internal TIM FIFO Empty Flag			Empty	OK
<b>Bit 17:</b> Internal TIM FIFO Full Flag			Full	OK
<b>Bits [30:18]:</b> Internal TIM FIFO Occupancy Count			Count	

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### 6.6 ROD Controller Internal TIM FIFO Register

Description	REG ID	Address	Access	Width
ROD Controller: Internal TIM FIFO Input Register	ACCESS FIFO	00404480	RW	8
			Bit Value	
Bits[7:0]: Internal TIM Input Data A read to this register will read the data from the Internal TIM FIFO, and place the result at this memory location. A write to this register will data the value to the next available TIM FIFO Write Location.			Value	

### 6.7 ROD Controller DSP Interrupt Registers

Description	REG ID	Address	Access	Width
ROD Controller: MDSP to SDSP Interrupt, INTRPT_TO_SLV	237	00404490	RW	4
MDSP can issue interrupt to Ext pin 5 input of all Slaves			Bit Value	
			1	0
Bit 0: MDSP to SDSP0			Int	Idle
Bit 1: MDSP to SDSP1			Int	Idle
Bit 2: MDSP to SDSP2			Int	Idle
Bit 3: MDSP to SDSP3			Int	Idle

Description	REG ID	Address	Access	Width
ROD Controller: SDSP to MDSP Interrupt, INTRPT_FROM_SLV	238	00404494	RW	4
HPI Interrupt Out from each slave can be mapped to any MDSP External Interrupt input			Bit Value	
			1	0
Bit 0: SDSP0 to MDSP			Int	Idle
Bit 1: SDSP1 to MDSP			Int	Idle
Bit 2: SDSP2 to MDSP			Int	Idle
Bit 3: SDSP3 to MDSP			Int	Idle

Description	REG ID	Address	Access	Width
ROD Controller: VME Interrupt Test		00404498	RW	7
Signal used to test VME interrupts			Bit Value	
			1	0
Bit 0: Generate Test Pulse (Self Clearing)			Int	Idle
Bits[6:4]: IRQ value			Value	

### 6.8 ROD Controller FE Occupancy Counter Control Registers

Description	REG ID	Address	Access	Width
ROD Controller: FE Occupancy Counter Reset: Links (31:0) FE_OCC_CNTR_RESET(0)	24F	004044A0	RW	32
Reset the FE Occupancy counters for Input Data Links 0 to 31.			Bit Value	
			1	0
Bits [31:0]: Resets for the FE Occupancy Counters Bit 0 resets the counter for Link 0, bit 1 for link 1, up to bit 31 for link 31.			Reset	Count

Description	REG ID	Address	Access	Width
ROD Controller: FE Occupancy Counter Reset: Links (63:32) FE_OCC_CNTR_RESET(1)	250	004044A4	RW	32
Reset the FE Occupancy counters for Input Data Links 32 to 63.			Bit Value	
			1	0
Bits [31:0]: Resets for the FE Occupancy Counters Bit 0 resets the counter for Link 32, bit 1 for link 33, up to bit 31 for link 63.			Reset	Count

Description	REG ID	Address	Access	Width
ROD Controller: FE Occupancy Counter Reset: Links (95:64) FE_OCC_CNTR_RESET(2)	251	004044A8	RW	32
Reset the FE Occupancy counters for Input Data Links 64 to 95.			Bit Value	
			1	0
Bits [31:0]: Resets for the FE Occupancy Counters Bit 0 resets the counter for Link 64, bit 1 for link 65, up to bit 31 for link 95.			Reset	Count

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Description	REG ID	Address	Access	Width
<b>ROD Controller: FE Occupancy Counter L1A Value (31:0)</b> <b>FE OCC CNTR NUM ACC(0)</b>	252	004044B0	RW	32
This register stores the number of L1 Accepts to expect from each FE module and is used in the Pixel FE Occupancy Counters.			<b>Bit Value</b>	
<b>Bits [ 3: 0]:</b> Num Accepts value for FE Module (0:0 F40 F80 F160)			Value	
<b>Bits [ 7: 4]:</b> Num Accepts value for FE Module (0:1 F40 F80)			Value	
<b>Bits [11: 8]:</b> Num Accepts value for FE Module (0:2 F40)			Value	
<b>Bits [15:12]:</b> Num Accepts value for FE Module (0:3 F40)			Value	
<b>Bits [19:16]:</b> Num Accepts value for FE Module (1:0 F40 F80 F160)			Value	
<b>Bits [23:20]:</b> Num Accepts value for FE Module (1:1 F40 F80)			Value	
<b>Bits [27:24]:</b> Num Accepts value for FE Module (1:2 F40)			Value	
<b>Bits [31:28]:</b> Num Accepts value for FE Module (2:0 F40 F80 F1600)			Value	

Description	REG ID	Address	Access	Width
<b>ROD Controller: FE Occupancy Counter L1A Value (31:0)</b> <b>FE OCC CNTR NUM ACC(1)</b>	253	004044B4	RW	32
This register stores the number of L1 Accepts to expect from each FE module and is used in the Pixel FE Occupancy Counters.			<b>Bit Value</b>	
<b>Bits [ 3: 0]:</b> Num Accepts value for FE Module (2:1 F40 F80)			Value	
<b>Bits [ 7: 4]:</b> Num Accepts value for FE Module (2:2 F40)			Value	
<b>Bits [11: 8]:</b> Num Accepts value for FE Module (2:3 F40)			Value	
<b>Bits [15:12]:</b> Num Accepts value for FE Module (3:0 F40 F80 F160)			Value	
<b>Bits [19:16]:</b> Num Accepts value for FE Module (3:1 F40 F80)			Value	
<b>Bits [23:20]:</b> Num Accepts value for FE Module (4:0 F40 F80 F160)			Value	
<b>Bits [27:24]:</b> Num Accepts value for FE Module (4:1 F40 F80)			Value	
<b>Bits [31:28]:</b> Num Accepts value for FE Module (4:2 F40)			Value	

Description	REG ID	Address	Access	Width
<b>ROD Controller: FE Occupancy Counter L1A Value (31:0)</b> <b>FE OCC CNTR NUM ACC(2)</b>	254	004044B8	RW	32
This register stores the number of L1 Accepts to expect from each FE module and is used in the Pixel FE Occupancy Counters.			<b>Bit Value</b>	
<b>Bits [ 3: 0]:</b> Num Accepts value for FE Module (4:3 F40)			Value	
<b>Bits [ 7: 4]:</b> Num Accepts value for FE Module (5:0 F40 F80 F160)			Value	
<b>Bits [11: 8]:</b> Num Accepts value for FE Module (5:1 F40 F80)			Value	
<b>Bits [15:12]:</b> Num Accepts value for FE Module (5:2 F40)			Value	
<b>Bits [19:16]:</b> Num Accepts value for FE Module (6:0 F40 F80 F160)			Value	
<b>Bits [23:20]:</b> Num Accepts value for FE Module (6:1 F40 F80)			Value	
<b>Bits [27:24]:</b> Num Accepts value for FE Module (6:2 F40)			Value	
<b>Bits [31:28]:</b> Num Accepts value for FE Module (6:3 F40)			Value	

Description	REG ID	Address	Access	Width
<b>ROD Controller: FE Occupancy Counter L1A Value (31:0)</b> <b>FE OCC CNTR NUM ACC(3)</b>	255	004044BC	RW	8
This register stores the number of L1 Accepts to expect from each FE module and is used in the Pixel FE Occupancy Counters.			<b>Bit Value</b>	
<b>Bits [ 3:0]:</b> Num Accepts value for FE Module (7:0 F40 F80 F160)			Value	
<b>Bits [ 7:4]:</b> Num Accepts value for FE Module (7:1 F40 F80)			Value	
<b>Bits [31:8]:</b> Not Used			0	

### 6.9 ROD Controller Internal Scan Calibration and Event ID Registers

Description	REG ID	Address	Access	Width
<b>ROD Controller: Internal Scan NEvent Register: (23:0)</b> <b>DATA LINK MASK(0)</b>	256	004044C0	RW	15
Number of events to issue to Pixel FE Modules. NEvent : Number of command sequences to issue in this mask stage			<b>Bit Value</b>	
<b>Bits [15: 0]:</b> NEvent Value			Value	
<b>Bits [23:16]:</b> Pre CAL Command Delay Value			Value	

Description	REG ID	Address	Access	Width
<b>ROD Controller: Internal Scan TrigDelay Register: (31:0)</b> <b>DATA LINK MASK(1)</b>	257	004044C4	RW	32
Trigger Delay for Internal scans. TrigDelay0 : Delay between CAL and L1 commands in 100ns inc. for even groups TrigDelay1 : Delay between CAL and L1 commands in 100ns inc. for odd groups			<b>Bit Value</b>	
<b>Bits [15: 0]:</b> TrigDelay0			Value	
<b>Bits [31:16]:</b> TrigDelay1			Value	

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Description	REG ID	Address	Access	Width
<b>ROD Controller: Internal Scan Interval Register: (31:0) DATA LINK MASK(2)</b>	258	004044C8	RW	32
Event Interval for Internal scans. Interval : Delay between successive cmd sequences in 25ns increment			<b>Bit Value</b>	
Bits [31:0]: Event Interval			1	0
			Value	

Description	REG ID	Address	Access	Width
<b>ROD Controller: Internal Scan Trigger Mode: (31:0) Trigger Mode Select Register/Active groups</b>		004044CC	RW	32
Trigger Mode for Internal scans. VALUE SCAN DESCRIPTION			<b>Bit Value</b>	
0x1 Self Trigger up to 4 groups L1A only			1	0
0x2 Group synchronous scan >> CAL/TD0/L1A				
0x3 Fixed interval scan >> CAL/TD0/L1A				
0x4 Fully synchronous scan >> CAL/TD0/L1A				
0x5 Cross-Talk 1 scan: Group(0) Default Mask >> CAL/TD0/L1A Group(0) Corrective >> PREDELAY/CAL/TD1/L1A				
0x6 Cross-Talk 2 scan: Group(0) Default Mask >> CAL/TD0/L1A Group(0) Corrective >> PREDELAY/NOCAL/TD1/L1A NOCAL = "00000000" to match timing of Pixel CAL command				
Bits [3:0]: Trigger Mode			Value	

Description	REG ID	Address	Access	Width
<b>ROD Controller: Calibration Event Type0 Register CAL_L1_TRIG_TYPE_0</b>	23B	004044D0	RW	10
ATLAS and TIM Event Types to send to the EFB if DSP SP0 is used as the source for the Command Data Streams			<b>Bit Value</b>	
Bits [7:0]: ATLAS Event Type for SP0			Value	
Bits [9:8]: TIM Event Type for SP0			Value	

Description	REG ID	Address	Access	Width
<b>ROD Controller: Calibration Event Type1 Register CAL_L1_TRIG_TYPE_1</b>	23C	004044D4	RW	10
ATLAS and TIM Event Types to send to the EFB if DSP SP1 is used as the source for the Command Data Streams			<b>Bit Value</b>	
Bits [7:0]: ATLAS Event Type for SP1			Value	
Bits [9:8]: TIM Event Type for SP1			Value	

Description	REG ID	Address	Access	Width
<b>ROD Controller: Internal Scan Status</b>		004044D8	R	1
			<b>Bit Value</b>	
Bit [0]: Scan Done			Done	Idle

Description	REG ID	Address	Access	Width
<b>ROD Controller: Calibration L1ID SP0 Register CAL_L1_ID_0</b>	23D	004044E0	R	24
If the ROD is configured for calibration using MDSP SP0 as a trigger source, then the value of this register is the L1ID sent to Event Fragment Builder. In this mode the user can choose to set the register prior to each trigger or allow a counter to increment the value for each trigger detected. If the ROD is configured in Internal Calibration mode, then the value in this register will increment for each trigger detected. If the ROD is configured in Physics Data Taking mode and the Diagnostic Event Counter bit is set then this register will count L1 triggers received from the TTC system.			<b>Bit Value</b>	
Bits [23:0]: L1ID for SP0			Value	

Description	REG ID	Address	Access	Width
<b>ROD Controller: Calibration L1ID SP1 Register CAL_L1_ID_1</b>	23E	004044E4	R	24
If the ROD is configured for calibration using MDSP SP1 as a trigger source, then the value of this register is the L1ID sent to Event Fragment Builder. In this mode the user can choose to set the register prior to each trigger or allow a counter to increment the value for each trigger detected. If the ROD is configured in Internal Calibration mode, then the value in this register will increment for each trigger detected. If the ROD is configured in Physics Data Taking mode and the Diagnostic Event Counter bit is set then this register will count L1 triggers received from the TTC system while ROD Busy is asserted.			<b>Bit Value</b>	

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Bits [23:0]: L1ID for SP1			Value	
Description	REG ID	Address	Access	Width
ROD Controller: Calibration BCID Register CAL_BCID	23F	004044E8	RW	28
BCID values to send to the EFB if DSP SP0 or SP1 are used as the sources for the Command Data Streams			Bit Value	
Bits [11: 0]: BCID for SP0			Value	
Bits [27:16]: BCID for SP1			Value	

Description	REG ID	Address	Access	Width
ROD Controller: Event L1ID		004044EC	RW	23
Latched value of the last L1ID sent to the EFB			Bit Value	
Bits [23: 0]: L1ID			Value	

### 6.10 ROD Controller Fixed Frequency Trigger Veto Registers

Description	REG ID	Address	Access	Width
ROD Controller: Fixed Frequency Trigger Veto Command FFTV_CMND		004044F0	RW	8
			Bit Value	
			1	0
Bit [0] : Emergency Clear			Clear	Idle
Bit [1] : Count Clear			Clear	Idle
Bit [2] : ID Clear			Clear	Idle
Bit [3] : Not Used				
Bits [7:4] : FFTV Match Level			Value	

Description	REG ID	Address	Access	Width
ROD Controller: Fixed Frequency Trigger Veto Busy Counter FFTV_BUSY_COUNT		004044F4	R	23
			Bit Value	
			1	0
Bits [19:0] : Busy Time Counter			Value	
Bit [20] : Busy Time Counter Rollover (Latching)			Over	Idle
Bit [21] : Busy Active			Busy	Idle
Bit [22] : Busy Active (Latching)			Busy	Idle
Bit [23] : Emergency Active			Emerg	Idle
Bit [24] : Emergency Active (Latching)			Emerg	Idle

Description	REG ID	Address	Access	Width
ROD Controller: Fixed Frequency Trigger Veto Status FFTV_STAT		004044F8	R	21
			Bit Value	
			1	0
Bits [11:0] : ID Counter			Value	
Bit [12] : ID Counter Rollover (Latching)			Over	Idle
Bit [13] : Not Used			Over	Idle
Bit [14] : Not Used			Over	Idle
Bit [15] : Not Used			Over	Idle
Bits [19:16] : FFTV Match Level Readback			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

### 6.11 ROD Controller FE Occupancy Counters

Description	REG ID	Address	Access	Width
FE Occupancy Counters: Links ( 7: 0), FE OCC CNTR(0)	259	00404500	R	32
FE Occupancy Counters: Links (15: 8), FE OCC CNTR(1)	25A	00404504	R	32
FE Occupancy Counters: Links (23:16), FE OCC CNTR(2)	25B	00404508	R	32
FE Occupancy Counters: Links (31:24), FE OCC CNTR(3)	25C	0040450C	R	32
FE Occupancy Counters: Links (39:32), FE OCC CNTR(4)	25D	00404510	R	32
FE Occupancy Counters: Links (47:40), FE OCC CNTR(5)	25E	00404514	R	32
FE Occupancy Counters: Links (55:48), FE OCC CNTR(6)	25F	00404518	R	32
FE Occupancy Counters: Links (63:56), FE OCC CNTR(7)	260	0040451C	R	32
FE Occupancy Counters: Links (71:64), FE OCC CNTR(8)		00404520	R	32
FE Occupancy Counters: Links (79:72), FE OCC CNTR(9)		00404524	R	32
FE Occupancy Counters: Links (87:80), FE OCC CNTR(10)		00404528	R	32
FE Occupancy Counters: Links (95:88), FE OCC CNTR(11)		0040452C	R	32
			Bit Value	
Bits[ 3: 0]: FE OCC Counter Links 0, 8,16,24,32,40,48,56,64,72,80,88			Count	
Bits[ 7: 4]: FE OCC Counter Links 1, 9,17,25,33,41,49,57,65,73,81,89			Count	
Bits[11: 8]: FE OCC Counter Links 2,10,18,26,34,42,50,58,66,74,82,90			Count	
Bits[15:12]: FE OCC Counter Links 3,11,19,27,35,43,51,59,67,75,83,91			Count	
Bits[19:16]: FE OCC Counter Links 4,12,20,28,36,44,52,60,68,76,84,92			Count	
Bits[23:20]: FE OCC Counter Links 5,13,21,29,37,45,53,61,69,77,85,93			Count	
Bits[27:24]: FE OCC Counter Links 6,14,22,30,38,46,54,62,70,78,86,94			Count	
Bits[32:28]: FE OCC Counter Links 7,15,23,31,39,47,55,63,71,79,87,95			Count	

### 6.12 ROD Controller Internal Scan Group to Link Map

Description	REG ID	Address	Access	Width
FE Occupancy Counters: Group to Link Map		00404530	RW	32
Highest link in Engine 0 → (12*n + 0, 1, 2, 3)      n=Formatter Number			Bit Value	
Highest link in Engine 1 → ((48+(12*n) + 0, 1, 2, 3)				
Bits[ 5: 0]: Group 0 Highest Link in Engine 0			0x0 to 0x2F	
Bits[13: 8]: Group 0 Highest Link in Engine 1			0x0 to 0x2F	
Bits[21:16]: Group 1 Highest Link in Engine 0			0x0 to 0x2F	
Bits[29:24]: Group 1 Highest Link in Engine 1			0x0 to 0x2F	

Description	REG ID	Address	Access	Width
FE Occupancy Counters: Group to Link Map		00404534	RW	32
Highest link in Engine 0 → (12*n + 0, 1, 2, 3)      n=Formatter Number			Bit Value	
Highest link in Engine 1 → ((48+(12*n) + 0, 1, 2, 3)				
Bits[ 5: 0]: Group 2 Highest Link in Engine 0			0x0 to 0x2F	
Bits[13: 8]: Group 2 Highest Link in Engine 1			0x0 to 0x2F	
Bits[21:16]: Group 3 Highest Link in Engine 0			0x0 to 0x2F	
Bits[29:24]: Group 3 Highest Link in Engine 1			0x0 to 0x2F	

Description	REG ID	Address	Access	Width
FE Occupancy Counters: Internal Scan Group Enable		00404540	RW	8
			Bit Value	
Bit[0]: Group 0 Enable			Enable	Disable
Bit[1]: Group 1 Enable			Enable	Disable
Bit[2]: Group 2 Enable			Enable	Disable
Bit[3]: Group 3 Enable			Enable	Disable
—Bit[4]: Group 4 Enable			Enable	Disable
—Bit[5]: Group 5 Enable			Enable	Disable
—Bit[6]: Group 6 Enable			Enable	Disable
—Bit[7]: Group 7 Enable			Enable	Disable

# APPENDIX A: ROD and BOC FPGA Register Definitions

## 6.13 ROD Controller FE Command Mask LUT

Description	REG ID	Address	Access	Width
FE Command Mask, SP0, Mask 0, Links (31:0): CMND_MASK_LUT(0,0,0)	398	00404600	RW	32
FE Command Mask, SP0, Mask 0, Links (47:32): CMND_MASK_LUT(0,0,1)	399	00404604	RW	16
FE Command Mask, SP1, Mask 0, Links (31: 0): CMND_MASK_LUT(0,1,0)	39A	00404608	RW	32
FE Command Mask, SP1, Mask 0, Links (47:32): CMND_MASK_LUT(0,1,1)	39B	0040460C	RW	16
FE Command Mask, SP0, Mask 1, Links (31:0): CMND_MASK_LUT(1,0,0)	39C	00404610	RW	32
FE Command Mask, SP0, Mask 1, Links (47:32): CMND_MASK_LUT(1,0,1)	39D	00404614	RW	16
FE Command Mask, SP1, Mask 1, Links (31: 0): CMND_MASK_LUT(1,1,0)	39E	00404618	RW	32
FE Command Mask, SP1, Mask 1, Links (47:32): CMND_MASK_LUT(1,1,1)	39F	0040461C	RW	16
FE Command Mask, SP0, Mask 2, Links (31:0): CMND_MASK_LUT(2,0,0)	3A0	00404620	RW	32
FE Command Mask, SP0, Mask 2, Links (47:32): CMND_MASK_LUT(2,0,1)	3A1	00404624	RW	16
FE Command Mask, SP1, Mask 2, Links (31: 0): CMND_MASK_LUT(2,1,0)	3A2	00404628	RW	32
FE Command Mask, SP1, Mask 2, Links (47:32): CMND_MASK_LUT(2,1,1)	3A3	0040462C	RW	16
FE Command Mask, SP0, Mask 3, Links (31:0): CMND_MASK_LUT(3,0,0)	3A4	00404630	RW	32
FE Command Mask, SP0, Mask 3, Links (47:32): CMND_MASK_LUT(3,0,1)	3A5	00404634	RW	16
FE Command Mask, SP1, Mask 3, Links (31: 0): CMND_MASK_LUT(3,1,0)	3A6	00404638	RW	32
FE Command Mask, SP1, Mask 3, Links (47:32): CMND_MASK_LUT(3,1,1)	3A7	0040463C	RW	16
FE Command Mask, SP0, Mask 4, Links (31:0): CMND_MASK_LUT(4,0,0)	3A8	00404640	RW	32
FE Command Mask, SP0, Mask 4, Links (47:32): CMND_MASK_LUT(4,0,1)	3A9	00404644	RW	16
FE Command Mask, SP1, Mask 4, Links (31: 0): CMND_MASK_LUT(4,1,0)	3AA	00404648	RW	32
FE Command Mask, SP1, Mask 4, Links (47:32): CMND_MASK_LUT(4,1,1)	3AB	0040464C	RW	16
FE Command Mask, SP0, Mask 5, Links (31:0): CMND_MASK_LUT(5,0,0)	3AC	00404650	RW	32
FE Command Mask, SP0, Mask 5, Links (47:32): CMND_MASK_LUT(5,0,1)	3AD	00404654	RW	16
FE Command Mask, SP1, Mask 5, Links (31: 0): CMND_MASK_LUT(5,1,0)	3AE	00404658	RW	32
FE Command Mask, SP1, Mask 5, Links (47:32): CMND_MASK_LUT(5,1,1)	3AF	0040465C	RW	16
FE Command Mask, SP0, Mask 6, Links (31:0): CMND_MASK_LUT(6,0,0)	3B0	00404660	RW	32
FE Command Mask, SP0, Mask 6, Links (47:32): CMND_MASK_LUT(6,0,1)	3B1	00404664	RW	16
FE Command Mask, SP1, Mask 6, Links (31: 0): CMND_MASK_LUT(6,1,0)	3B2	00404668	RW	32
FE Command Mask, SP1, Mask 6, Links (47:32): CMND_MASK_LUT(6,1,1)	3B3	0040466C	RW	16
FE Command Mask, SP0, Mask 7, Links (31:0): CMND_MASK_LUT(7,0,0)	3B4	00404670	RW	32
FE Command Mask, SP0, Mask 7, Links (47:32): CMND_MASK_LUT(7,0,1)	3B5	00404674	RW	16
FE Command Mask, SP1, Mask 7, Links (31: 0): CMND_MASK_LUT(7,1,0)	3B6	00404678	RW	32
FE Command Mask, SP1, Mask 7, Links (47:32): CMND_MASK_LUT(7,1,1)	3B7	0040467C	RW	16
Stores the values used by the FE Command Processor to send or mask commands to the FE Modules.				Bit Value
Bits[31: 0]: Mask Values for output command links				Value

## APPENDIX A: ROD and BOC FPGA Register Definitions

### 6.14 ROD Controller Default Event Type Register

Description	REG ID	Address	Access	Width
<b>ROD Default Event Type (7:0), DFLT ROD EVT TYPE</b>	<b>239</b>	<b>00404700</b>	<b>RW</b>	<b>7</b>
This Register stores the value of the ROD Specific Event Type used when a Normal or SP0 L1A Trigger is detected			<b>Bit Value</b>	
<b>Bits [7: 0]:</b> Default ROD Event Type			Value	

### 6.15 ROD Controller Default Dynamic Mask LUTs

The EFB Dynamic Mask Bits, default and corrective, are stored in Look-Up Tables (LUTs) that are implemented using internal block RAM blocks in the ROD Controller FPGA (RCF). When the RCF is configured (loading of configuration data from the Program Reset Manager FPGA or a hardware reset), the values in the RAM blocks are initialized to 0. **A software reset to the ROD does not clear the previous values stored in the EFB DM LUTs.** After a soft reset to the ROD the EFB dynamic mask bits must be set to the desired values prior to a take data command.

Description	REG ID	Address	Access	Width
<b>EFB Default Dynamic Mask: Links ( 7: 0), DM DFLT LUT(0)</b>	<b>270</b>	<b>00404704</b>	<b>RW</b>	<b>16</b>
<b>EFB Default Dynamic Mask: Links (15: 8), DM DFLT LUT(1)</b>	<b>271</b>	<b>00404708</b>	<b>RW</b>	<b>16</b>
<b>EFB Default Dynamic Mask: Links (23:16), DM DFLT LUT(2)</b>	<b>272</b>	<b>0040470C</b>	<b>RW</b>	<b>16</b>
<b>EFB Default Dynamic Mask: Links (31:24), DM DFLT LUT(3)</b>	<b>273</b>	<b>00404710</b>	<b>RW</b>	<b>16</b>
<b>EFB Default Dynamic Mask: Links (39:32), DM DFLT LUT(4)</b>	<b>274</b>	<b>00404714</b>	<b>RW</b>	<b>16</b>
<b>EFB Default Dynamic Mask: Links (47:40), DM DFLT LUT(5)</b>	<b>275</b>	<b>00404718</b>	<b>RW</b>	<b>16</b>
<b>EFB Default Dynamic Mask: Links (55:48), DM DFLT LUT(6)</b>	<b>276</b>	<b>0040471C</b>	<b>RW</b>	<b>16</b>
<b>EFB Default Dynamic Mask: Links (63:56), DM DFLT LUT(7)</b>	<b>277</b>	<b>00404720</b>	<b>RW</b>	<b>16</b>
<b>EFB Default Dynamic Mask: Links (71:64), DM DFLT LUT(8)</b>	<b>278</b>	<b>00404724</b>	<b>RW</b>	<b>16</b>
<b>EFB Default Dynamic Mask: Links (79:72), DM DFLT LUT(9)</b>	<b>279</b>	<b>00404728</b>	<b>RW</b>	<b>16</b>
<b>EFB Default Dynamic Mask: Links (87:80), DM DFLT LUT(10)</b>	<b>27A</b>	<b>0040472C</b>	<b>RW</b>	<b>16</b>
<b>EFB Default Dynamic Mask: Links (95:88), DM DFLT LUT(11)</b>	<b>27B</b>	<b>00404730</b>	<b>RW</b>	<b>16</b>
This Register stores the mask values used when a Normal or SP0 L1A Trigger is detected. Mask = 00: L1ID OK, No Modification Mask = 01: Increment L1ID for this Link by 1 Mask = 10: Decrement L1ID for this Link by 1			<b>Bit Value</b>	
<b>Bits[ 1: 0]:</b> Default Mask, Links 0, 8,16,24,32,40,48,56,64,72,80,88			Mask	
<b>Bits[ 3: 2]:</b> Default Mask, Links 1, 9,17,25,33,41,49,57,65,73,81,89			Mask	
<b>Bits[ 5: 4]:</b> Default Mask, Links 2,10,18,26,34,42,50,58,66,74,82,90			Mask	
<b>Bits[ 7: 6]:</b> Default Mask, Links 3,11,19,27,35,43,51,59,67,75,83,91			Mask	
<b>Bits[ 9: 8]:</b> Default Mask, Links 4,12,20,28,36,44,52,60,68,76,84,92			Mask	
<b>Bits[11:10]:</b> Default Mask, Links 5,13,21,29,37,45,53,61,69,77,85,93			Mask	
<b>Bits[13:12]:</b> Default Mask, Links 6,14,22,30,38,46,54,62,70,78,86,94			Mask	
<b>Bits[15:14]:</b> Default Mask, Links 7,15,23,31,39,47,55,63,71,79,87,95			Mask	

### 6.16 ROD Controller Corrective Event Type Register

Description	REG ID	Address	Access	Width
<b>ROD Corrective Event Type (7:0), CRTV ROD EVT TYPE</b>	<b>23A</b>	<b>00404740</b>	<b>RW</b>	<b>7</b>
This Register stores the value of the ROD Specific Event Type used when a Corrective or SP1 L1A Trigger is detected			<b>Bit Value</b>	
<b>Bits [7: 0]:</b> Corrective ROD Event Type			Value	



## APPENDIX A: ROD and BOC FPGA Register Definitions

### 6.17 ROD Controller Corrective Dynamic Mask LUTs

Description	REG ID	Address	Access	Width
EFB Corrective Dynamic Mask: Links ( 7: 0) , DM CRTV LUT(0)	27C	00404744	RW	16
EFB Corrective Dynamic Mask: Links(15: 8) , DM CRTV LUT(1)	27D	00404748	RW	16
EFB Corrective Dynamic Mask: Links(23:16) , DM CRTV LUT(2)	27E	0040474C	RW	16
EFB Corrective Dynamic Mask: Links(31:24) , DM CRTV LUT(3)	27F	00404750	RW	16
EFB Corrective Dynamic Mask: Links(39:32) , DM CRTV LUT(4)	280	00404754	RW	16
EFB Corrective Dynamic Mask: Links(47:40) , DM CRTV LUT(5)	281	00404758	RW	16
EFB Corrective Dynamic Mask: Links(55:48) , DM CRTV LUT(6)	282	0040475C	RW	16
EFB Corrective Dynamic Mask: Links(63:56) , DM CRTV LUT(7)	283	00404760	RW	16
EFB Corrective Dynamic Mask: Links(71:64) , DM CRTV LUT(8)	284	00404764	RW	16
EFB Corrective Dynamic Mask: Links(79:72) , DM CRTV LUT(9)	285	00404768	RW	16
EFB Corrective Dynamic Mask: Links(87:80) , DM CRTV LUT(10)	286	0040476C	RW	16
EFB Corrective Dynamic Mask: Links(95:88) , DM CRTV LUT(11)	287	00404770	RW	16
This Register stores the mask values used when a Corrective or SP1 L1A Trigger is detected. Mask = 00: L1ID OK, No Modification Mask = 01: Increment L1ID for this Link by 1 Mask = 10: Decrement L1ID for this Link by 1			Bit Value	
Bits[ 1: 0]: Corrective Mask Links 0, 8,16,24,32,40,48,56,64,72,80,88			Mask	
Bits[ 3: 2]: Corrective Mask Links 1, 9,17,25,33,41,49,57,65,73,81,89			Mask	
Bits[ 5: 4]: Corrective Mask Links 2,10,18,26,34,42,50,58,66,74,82,90			Mask	
Bits[ 7: 6]: Corrective Mask Links 3,11,19,27,35,43,51,59,67,75,83,91			Mask	
Bits[ 9: 8]: Corrective Mask Links 4,12,20,28,36,44,52,60,68,76,84,92			Mask	
Bits[11:10]: Corrective Mask Links 5,13,21,29,37,45,53,61,69,77,85,93			Mask	
Bits[13:12]: Corrective Mask Links 6,14,22,30,38,46,54,62,70,78,86,94			Mask	
Bits[15:14]: Corrective Mask Links 7,15,23,31,39,47,55,63,71,79,87,95			Mask	

### 6.18 ROD Controller Corrected Events FIFO

Description	REG ID	Address	Access	Width
Corrected Event FIFO, CORRECTED_EVENTS_FIFO	288	00404780	RW	16
			Bit Value	
Bits[15: 0]: Corrective Events FIFO Data			Value	

### 6.19 ROD Controller Formatter Mode Bits LUT

The Formatter Dynamic Mode Bits, default and corrective, are stored in Look-Up Tables (LUTs) that are implemented using internal block RAM blocks in the ROD Controller FPGA (RCF). When the RCF is configured (loading of configuration data from the Program Reset Manager FPGA or a hardware reset), the values in the RAM blocks are initialized to 0. **A software reset to the ROD does not clear the previous values stored in the FMB LUT.** After a soft reset to the ROD the dynamic mode bits must be set to the desired values prior to a take data command.

MB1	MB0	Formatter Read Out Mode Bits Definitions
0	0	Play 1st event from Link FIFO. Normal data flow from Formatter to EFB.
0	1	Mask this link for 1 event. In this mode, the formatter will dump one event from the link FIFO.
1	0	Skip read out of this link for 1 event for re-synchronization.
1	1	Read out 1 <sup>st</sup> event from FIFO and dump it on the floor, play the 2nd event to the EFB.

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Default MB0, Links (11: 0), Mask0: RMB DFLT LUT (0,0,0)	298	00404800	RW	12
Default MB0, Links (23:12), Mask0: RMB DFLT LUT (0,1,0)	29A	00404808	RW	12
Default MB0, Links (35:24), Mask0: RMB DFLT LUT (0,2,0)	29C	00404810	RW	12
Default MB0, Links (47:36), Mask0: RMB DFLT LUT (0,3,0)	29E	00404818	RW	12
Default MB0, Links (59:48), Mask0: RMB DFLT LUT (0,4,0)	2A0	00404820	RW	12
Default MB0, Links (71:60), Mask0: RMB DFLT LUT (0,5,0)	2A2	00404828	RW	12
Default MB0, Links (83:72), Mask0: RMB DFLT LUT (0,6,0)	2A4	00404830	RW	12
Default MB0, Links (95:84), Mask0: RMB DFLT LUT (0,7,0)	2A6	00404838	RW	12
This Register stores the values of Mode Bit 0 (MB0) used when a normal or SP0 Trigger is detected.			Bit Value	
Bit 0: Formatter Mode Bits: Default MB0, Links 0,12,24,36,48,60,72,84			MB0	
Bit 1: Formatter Mode Bits: Default MB0, Links 1,13,25,37,49,61,73,85			MB0	
Bit 2: Formatter Mode Bits: Default MB0, Links 2,14,26,38,50,62,74,86			MB0	
Bit 3: Formatter Mode Bits: Default MB0, Links 3,15,27,39,51,63,75,87			MB0	
Bit 4: Formatter Mode Bits: Default MB0, Links 4,16,28,40,52,64,76,88			MB0	
Bit 5: Formatter Mode Bits: Default MB0, Links 5,17,29,41,53,65,77,89			MB0	
Bit 6: Formatter Mode Bits: Default MB0, Links 6,18,30,42,54,66,78,90			MB0	
Bit 7: Formatter Mode Bits: Default MB0, Links 7,19,31,43,55,67,79,91			MB0	
Bit 8: Formatter Mode Bits: Default MB0, Links 8,20,32,44,56,68,80,92			MB0	
Bit 9: Formatter Mode Bits: Default MB0, Links 9,21,33,45,57,69,81,93			MB0	
Bit 10: Formatter Mode Bits: Default MB0, Links 10,22,34,46,58,70,82,94			MB0	
Bit 11: Formatter Mode Bits: Default MB0, Links 11,23,35,47,59,71,83,95			MB0	

Description	REG ID	Address	Access	Width
Default MB1, Links (11: 0), Mask0: RMB DFLT LUT (0,0,1)	299	00404804	RW	12
Default MB1, Links (23:12), Mask0: RMB DFLT LUT (0,1,1)	29B	0040480C	RW	12
Default MB1, Links (35:24), Mask0: RMB DFLT LUT (0,2,1)	29D	00404814	RW	12
Default MB1, Links (47:36), Mask0: RMB DFLT LUT (0,3,1)	29F	0040481C	RW	12
Default MB1, Links (59:48), Mask0: RMB DFLT LUT (0,4,1)	2A1	00404824	RW	12
Default MB1, Links (71:60), Mask0: RMB DFLT LUT (0,5,1)	2A3	0040482C	RW	12
Default MB1, Links (83:72), Mask0: RMB DFLT LUT (0,6,1)	2A5	00404834	RW	12
Default MB1, Links (95:84), Mask0: RMB DFLT LUT (0,7,1)	2A7	0040483C	RW	12
This Register stores the values of Mode Bit 1 (MB1) used when a normal or SP0 Trigger is detected.			Bit Value	
Bit 0: Formatter Mode Bits: Default MB1, Links 0,12,24,36,48,60,72,84			MB1	
Bit 1: Formatter Mode Bits: Default MB1, Links 1,13,25,37,49,61,73,85			MB1	
Bit 2: Formatter Mode Bits: Default MB1, Links 2,14,26,38,50,62,74,86			MB1	
Bit 3: Formatter Mode Bits: Default MB1, Links 3,15,27,39,51,63,75,87			MB1	
Bit 4: Formatter Mode Bits: Default MB1, Links 4,16,28,40,52,64,76,88			MB1	
Bit 5: Formatter Mode Bits: Default MB1, Links 5,17,29,41,53,65,77,89			MB1	
Bit 6: Formatter Mode Bits: Default MB1, Links 6,18,30,42,54,66,78,90			MB1	
Bit 7: Formatter Mode Bits: Default MB1, Links 7,19,31,43,55,67,79,91			MB1	
Bit 8: Formatter Mode Bits: Default MB1, Links 8,20,32,44,56,68,80,92			MB1	
Bit 9: Formatter Mode Bits: Default MB1, Links 9,21,33,45,57,69,81,93			MB1	
Bit 10: Formatter Mode Bits: Default MB1, Links 10,22,34,46,58,70,82,94			MB1	
Bit 11: Formatter Mode Bits: Default MB1, Links 11,23,35,47,59,71,83,95			MB1	

Description	REG ID	Address	Access	Width
Corrective MB0, Links (11: 0), Mask0: RMB CRTV LUT (0,0,0)	318	00404840	RW	12
Corrective MB0, Links (23:12), Mask0: RMB CRTV LUT (0,1,0)	31A	00404848	RW	12
Corrective MB0, Links (35:24), Mask0: RMB CRTV LUT (0,2,0)	31C	00404850	RW	12
Corrective MB0, Links (47:36), Mask0: RMB CRTV LUT (0,3,0)	31E	00404858	RW	12
Corrective MB0, Links (59:48), Mask0: RMB CRTV LUT (0,4,0)	320	00404860	RW	12
Corrective MB0, Links (71:60), Mask0: RMB CRTV LUT (0,5,0)	322	00404868	RW	12
Corrective MB0, Links (83:72), Mask0: RMB CRTV LUT (0,6,0)	324	00404870	RW	12
Corrective MB0, Links (95:84), Mask0: RMB CRTV LUT (0,7,0)	326	00404878	RW	12
This Register stores the values of Mode Bit 0 (MB0) used when a Corrective or SPL Trigger is detected.			Bit Value	
Bit 0: Formatter Mode Bits: Corrective MB0, Links 0,12,24,36,48,60,72,84			MB0	
Bit 1: Formatter Mode Bits: Corrective MB0, Links 1,13,25,37,49,61,73,85			MB0	
Bit 2: Formatter Mode Bits: Corrective MB0, Links 2,14,26,38,50,62,74,86			MB0	
Bit 3: Formatter Mode Bits: Corrective MB0, Links 3,15,27,39,51,63,75,87			MB0	
Bit 4: Formatter Mode Bits: Corrective MB0, Links 4,16,28,40,52,64,76,88			MB0	
Bit 5: Formatter Mode Bits: Corrective MB0, Links 5,17,29,41,53,65,77,89			MB0	
Bit 6: Formatter Mode Bits: Corrective MB0, Links 6,18,30,42,54,66,78,90			MB0	
Bit 7: Formatter Mode Bits: Corrective MB0, Links 7,19,31,43,55,67,79,91			MB0	
Bit 8: Formatter Mode Bits: Corrective MB0, Links 8,20,32,44,56,68,80,92			MB0	
Bit 9: Formatter Mode Bits: Corrective MB0, Links 9,21,33,45,57,69,81,93			MB0	
Bit 10: Formatter Mode Bits: Corrective MB0, Links 10,22,34,46,58,70,82,94			MB0	
Bit 11: Formatter Mode Bits: Corrective MB0, Links 11,23,35,47,59,71,83,95			MB0	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Corrective MB1, Links (11: 0), Mask0: RMB CRTV LUT(0,0,1)	319	00404844	RW	12
Corrective MB1, Links (23:12), Mask0: RMB CRTV LUT(0,1,1)	31B	0040484C	RW	12
Corrective MB1, Links (35:24), Mask0: RMB CRTV LUT(0,2,1)	31D	00404854	RW	12
Corrective MB1, Links (47:36), Mask0: RMB CRTV LUT(0,3,1)	31F	0040485C	RW	12
Corrective MB1, Links (59:48), Mask0: RMB CRTV LUT(0,4,1)	321	00404864	RW	12
Corrective MB1, Links (71:60), Mask0: RMB CRTV LUT(0,5,1)	323	0040486C	RW	12
Corrective MB1, Links (83:72), Mask0: RMB CRTV LUT(0,6,1)	325	00404874	RW	12
Corrective MB1, Links (95:84), Mask0: RMB CRTV LUT(0,7,1)	327	0040487C	RW	12
This Register stores the values of Mode Bit 1 (MB1) used when a Corrective or SPI Trigger is detected.			Bit Value	
Bit 0: Formatter Mode Bits: Corrective MB1, Links 0,12,24,36,48,60,72,84			MB1	
Bit 1: Formatter Mode Bits: Corrective MB1, Links 1,13,25,37,49,61,73,85			MB1	
Bit 2: Formatter Mode Bits: Corrective MB1, Links 2,14,26,38,50,62,74,86			MB1	
Bit 3: Formatter Mode Bits: Corrective MB1, Links 3,15,27,39,51,63,75,87			MB1	
Bit 4: Formatter Mode Bits: Corrective MB1, Links 4,16,28,40,52,64,76,88			MB1	
Bit 5: Formatter Mode Bits: Corrective MB1, Links 5,17,29,41,53,65,77,89			MB1	
Bit 6: Formatter Mode Bits: Corrective MB1, Links 6,18,30,42,54,66,78,90			MB1	
Bit 7: Formatter Mode Bits: Corrective MB1, Links 7,19,31,43,55,67,79,91			MB1	
Bit 8: Formatter Mode Bits: Corrective MB1, Links 8,20,32,44,56,68,80,92			MB1	
Bit 9: Formatter Mode Bits: Corrective MB1, Links 9,21,33,45,57,69,81,93			MB1	
Bit 10: Formatter Mode Bits: Corrective MB1, Links 10,22,34,46,58,70,82,94			MB1	
Bit 11: Formatter Mode Bits: Corrective MB1, Links 11,23,35,47,59,71,83,95			MB1	

Description	REG ID	Address	Access	Width
Default MB0, Links (11: 0), Mask1: RMB DFLT LUT(1,0,0)	2A8	00404880	RW	12
Default MB1, Links (11: 0), Mask1: RMB DFLT LUT(1,0,1)	2A9	00404884	RW	12
Default MB0, Links (23:12), Mask1: RMB DFLT LUT(1,1,0)	2AA	00404888	RW	12
Default MB1, Links (23:12), Mask1: RMB DFLT LUT(1,1,1)	2AB	0040488C	RW	12
Default MB0, Links (35:24), Mask1: RMB DFLT LUT(1,2,0)	2AC	00404890	RW	12
Default MB1, Links (35:24), Mask1: RMB DFLT LUT(1,2,1)	2AD	00404894	RW	12
Default MB0, Links (47:36), Mask1: RMB DFLT LUT(1,3,0)	2AE	00404898	RW	12
Default MB1, Links (47:36), Mask1: RMB DFLT LUT(1,3,1)	2AF	0040489C	RW	12
Default MB0, Links (59:48), Mask1: RMB DFLT LUT(1,4,0)	2B0	004048A0	RW	12
Default MB1, Links (59:48), Mask1: RMB DFLT LUT(1,4,1)	2B1	004048A4	RW	12
Default MB0, Links (71:60), Mask1: RMB DFLT LUT(1,5,0)	2B2	004048A8	RW	12
Default MB1, Links (71:60), Mask1: RMB DFLT LUT(1,5,1)	2B3	004048AC	RW	12
Default MB0, Links (83:72), Mask1: RMB DFLT LUT(1,6,0)	2B4	004048B0	RW	12
Default MB1, Links (83:72), Mask1: RMB DFLT LUT(1,6,1)	2B5	004048B4	RW	12
Default MB0, Links (95:84), Mask1: RMB DFLT LUT(1,7,0)	2B6	004048B8	RW	12
Default MB1, Links (95:84), Mask1: RMB DFLT LUT(1,7,1)	2B7	004048BC	RW	12
Corrective MB0, Links (11: 0), Mask1: RMB CRTV LUT(1,0,0)	328	004048C0	RW	12
Corrective MB1, Links (11: 0), Mask1: RMB CRTV LUT(1,0,1)	329	004048C4	RW	12
Corrective MB0, Links (23:12), Mask1: RMB CRTV LUT(1,1,0)	32A	004048C8	RW	12
Corrective MB1, Links (23:12), Mask1: RMB CRTV LUT(1,1,1)	32B	004048CC	RW	12
Corrective MB0, Links (35:24), Mask1: RMB CRTV LUT(1,2,0)	32C	004048D0	RW	12
Corrective MB1, Links (35:24), Mask1: RMB CRTV LUT(1,2,1)	32D	004048D4	RW	12
Corrective MB0, Links (47:36), Mask1: RMB CRTV LUT(1,3,0)	32E	004048D8	RW	12
Corrective MB1, Links (47:36), Mask1: RMB CRTV LUT(1,3,1)	32F	004048DC	RW	12
Corrective MB0, Links (59:48), Mask1: RMB CRTV LUT(1,4,0)	330	004048E0	RW	12
Corrective MB1, Links (59:48), Mask1: RMB CRTV LUT(1,4,1)	331	004048E4	RW	12
Corrective MB0, Links (71:60), Mask1: RMB CRTV LUT(1,5,0)	332	004048E8	RW	12
Corrective MB1, Links (71:60), Mask1: RMB CRTV LUT(1,5,1)	333	004048EC	RW	12
Corrective MB0, Links (83:72), Mask1: RMB CRTV LUT(1,6,0)	334	004048F0	RW	12
Corrective MB1, Links (83:72), Mask1: RMB CRTV LUT(1,6,1)	335	004048F4	RW	12
Corrective MB0, Links (95:84), Mask1: RMB CRTV LUT(1,7,0)	336	004048F8	RW	12
Corrective MB1, Links (95:84), Mask1: RMB CRTV LUT(1,7,1)	337	004048FC	RW	12

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Default MB0, Links (11: 0), Mask2: RMB_DFLT_LUT(2,0,0)	2B8	00404900	RW	12
Default MB1, Links (11: 0), Mask2: RMB_DFLT_LUT(2,0,1)	2B9	00404904	RW	12
Default MB0, Links (23:12), Mask2: RMB_DFLT_LUT(2,1,0)	2BA	00404908	RW	12
Default MB1, Links (23:12), Mask2: RMB_DFLT_LUT(2,1,1)	2BB	0040490C	RW	12
Default MB0, Links (35:24), Mask2: RMB_DFLT_LUT(2,2,0)	2BC	00404910	RW	12
Default MB1, Links (35:24), Mask2: RMB_DFLT_LUT(2,2,1)	2BD	00404914	RW	12
Default MB0, Links (47:36), Mask2: RMB_DFLT_LUT(2,3,0)	2BE	00404918	RW	12
Default MB1, Links (47:36), Mask2: RMB_DFLT_LUT(2,3,1)	2BF	0040491C	RW	12
Default MB0, Links (59:48), Mask2: RMB_DFLT_LUT(2,4,0)	2C0	00404920	RW	12
Default MB1, Links (59:48), Mask2: RMB_DFLT_LUT(2,4,1)	2C1	00404924	RW	12
Default MB0, Links (71:60), Mask2: RMB_DFLT_LUT(2,5,0)	2C2	00404928	RW	12
Default MB1, Links (71:60), Mask2: RMB_DFLT_LUT(2,5,1)	2C3	0040492C	RW	12
Default MB0, Links (83:72), Mask2: RMB_DFLT_LUT(2,6,0)	2C4	00404930	RW	12
Default MB1, Links (83:72), Mask2: RMB_DFLT_LUT(2,6,1)	2C5	00404924	RW	12
Default MB0, Links (95:84), Mask2: RMB_DFLT_LUT(2,7,0)	2C6	00404938	RW	12
Default MB1, Links (95:84), Mask2: RMB_DFLT_LUT(2,7,1)	2C7	0040493C	RW	12
Corrective MB0, Links (11: 0), Mask2: RMB_CRTV_LUT(2,0,0)	338	00404940	RW	12
Corrective MB1, Links (11: 0), Mask2: RMB_CRTV_LUT(2,0,1)	339	00404944	RW	12
Corrective MB0, Links (23:12), Mask2: RMB_CRTV_LUT(2,1,0)	33A	00404948	RW	12
Corrective MB1, Links (23:12), Mask2: RMB_CRTV_LUT(2,1,1)	33B	0040494C	RW	12
Corrective MB0, Links (35:24), Mask2: RMB_CRTV_LUT(2,2,0)	33C	00404950	RW	12
Corrective MB1, Links (35:24), Mask2: RMB_CRTV_LUT(2,2,1)	33D	00404954	RW	12
Corrective MB0, Links (47:36), Mask2: RMB_CRTV_LUT(2,3,0)	33E	00404958	RW	12
Corrective MB1, Links (47:36), Mask2: RMB_CRTV_LUT(2,3,1)	33F	0040495C	RW	12
Corrective MB0, Links (59:48), Mask2: RMB_CRTV_LUT(2,4,0)	340	00404960	RW	12
Corrective MB1, Links (59:48), Mask2: RMB_CRTV_LUT(2,4,1)	341	00404964	RW	12
Corrective MB0, Links (71:60), Mask2: RMB_CRTV_LUT(2,5,0)	342	00404968	RW	12
Corrective MB1, Links (71:60), Mask2: RMB_CRTV_LUT(2,5,1)	343	0040496C	RW	12
Corrective MB0, Links (83:72), Mask2: RMB_CRTV_LUT(2,6,0)	344	00404970	RW	12
Corrective MB1, Links (83:72), Mask2: RMB_CRTV_LUT(2,6,1)	345	00404974	RW	12
Corrective MB0, Links (95:84), Mask2: RMB_CRTV_LUT(2,7,0)	346	00404978	RW	12
Corrective MB1, Links (95:84), Mask2: RMB_CRTV_LUT(2,7,1)	347	0040497C	RW	12

Description	REG ID	Address	Access	Width
Default MB0, Links (11: 0), Mask3: RMB_DFLT_LUT(3,0,0)	2C8	00404980	RW	12
Default MB1, Links (11: 0), Mask3: RMB_DFLT_LUT(3,0,1)	2C9	00404984	RW	12
Default MB0, Links (23:12), Mask3: RMB_DFLT_LUT(3,1,0)	2CA	00404988	RW	12
Default MB1, Links (23:12), Mask3: RMB_DFLT_LUT(3,1,1)	2CB	0040498C	RW	12
Default MB0, Links (35:24), Mask3: RMB_DFLT_LUT(3,2,0)	2CC	00404990	RW	12
Default MB1, Links (35:24), Mask3: RMB_DFLT_LUT(3,2,1)	2CD	00404994	RW	12
Default MB0, Links (47:36), Mask3: RMB_DFLT_LUT(3,3,0)	2CE	00404998	RW	12
Default MB1, Links (47:36), Mask3: RMB_DFLT_LUT(3,3,1)	2CF	0040499C	RW	12
Default MB0, Links (59:48), Mask3: RMB_DFLT_LUT(3,4,0)	2D0	004049A0	RW	12
Default MB1, Links (59:48), Mask3: RMB_DFLT_LUT(3,4,1)	2D1	004049A4	RW	12
Default MB0, Links (71:60), Mask3: RMB_DFLT_LUT(3,5,0)	2D2	004049A8	RW	12
Default MB1, Links (71:60), Mask3: RMB_DFLT_LUT(3,5,1)	2D3	004049AC	RW	12
Default MB0, Links (83:72), Mask3: RMB_DFLT_LUT(3,6,0)	2D4	004049B0	RW	12
Default MB1, Links (83:72), Mask3: RMB_DFLT_LUT(3,6,1)	2D5	004049B4	RW	12
Default MB0, Links (95:84), Mask3: RMB_DFLT_LUT(3,7,0)	2D6	004049B8	RW	12
Default MB1, Links (95:84), Mask3: RMB_DFLT_LUT(3,7,1)	2D7	004049BC	RW	12
Corrective MB0, Links (11: 0), Mask3: RMB_CRTV_LUT(3,0,0)	348	004049C0	RW	12
Corrective MB1, Links (11: 0), Mask3: RMB_CRTV_LUT(3,0,1)	349	004049C4	RW	12
Corrective MB0, Links (23:12), Mask3: RMB_CRTV_LUT(3,1,0)	34A	004049C8	RW	12
Corrective MB1, Links (23:12), Mask3: RMB_CRTV_LUT(3,1,1)	34B	004049CC	RW	12
Corrective MB0, Links (35:24), Mask3: RMB_CRTV_LUT(3,2,0)	34C	004049D0	RW	12
Corrective MB1, Links (35:24), Mask3: RMB_CRTV_LUT(3,2,1)	34D	004049D4	RW	12
Corrective MB0, Links (47:36), Mask3: RMB_CRTV_LUT(3,3,0)	34E	004049D8	RW	12
Corrective MB1, Links (47:36), Mask3: RMB_CRTV_LUT(3,3,1)	34F	004049DC	RW	12
Corrective MB0, Links (59:48), Mask3: RMB_CRTV_LUT(3,4,0)	350	004049E0	RW	12
Corrective MB1, Links (59:48), Mask3: RMB_CRTV_LUT(3,4,1)	351	004049E4	RW	12
Corrective MB0, Links (71:60), Mask3: RMB_CRTV_LUT(3,5,0)	352	004049E8	RW	12
Corrective MB1, Links (71:60), Mask3: RMB_CRTV_LUT(3,5,1)	353	004049EC	RW	12
Corrective MB0, Links (83:72), Mask3: RMB_CRTV_LUT(3,6,0)	354	004049F0	RW	12
Corrective MB1, Links (83:72), Mask3: RMB_CRTV_LUT(3,6,1)	355	004049F4	RW	12
Corrective MB0, Links (95:84), Mask3: RMB_CRTV_LUT(3,7,0)	356	004049F8	RW	12
Corrective MB1, Links (95:84), Mask3: RMB_CRTV_LUT(3,7,1)	357	004049FC	RW	12

## APPENDIX A: ROD and BOC FPGA Register Definitions

Default MB0, Links (11: 0), Mask4: RMB_DFLT_LUT(4,0,0)	2D8	00404A00	RW	12
Default MB1, Links (11: 0), Mask4: RMB_DFLT_LUT(4,0,1)	2D9	00404A04	RW	12
Default MB0, Links (23:12), Mask4: RMB_DFLT_LUT(4,1,0)	2DA	00404A08	RW	12
Default MB1, Links (23:12), Mask4: RMB_DFLT_LUT(4,1,1)	2DB	00404A0C	RW	12
Default MB0, Links (35:24), Mask4: RMB_DFLT_LUT(4,2,0)	2DC	00404A10	RW	12
Default MB1, Links (35:24), Mask4: RMB_DFLT_LUT(4,2,1)	2DD	00404A14	RW	12
Default MB0, Links (47:36), Mask4: RMB_DFLT_LUT(4,3,0)	2DE	00404A18	RW	12
Default MB1, Links (47:36), Mask4: RMB_DFLT_LUT(4,3,1)	2DF	00404A1C	RW	12
Default MB0, Links (59:48), Mask4: RMB_DFLT_LUT(4,4,0)	2E0	00404A20	RW	12
Default MB1, Links (59:48), Mask4: RMB_DFLT_LUT(4,4,1)	2E1	00404A24	RW	12
Default MB0, Links (71:60), Mask4: RMB_DFLT_LUT(4,5,0)	2E2	00404A28	RW	12
Default MB1, Links (71:60), Mask4: RMB_DFLT_LUT(4,5,1)	2E3	00404A2C	RW	12
Default MB0, Links (83:72), Mask4: RMB_DFLT_LUT(4,6,0)	2E4	00404A30	RW	12
Default MB1, Links (83:72), Mask4: RMB_DFLT_LUT(4,6,1)	2E5	00404A34	RW	12
Default MB0, Links (95:84), Mask4: RMB_DFLT_LUT(4,7,0)	2E6	00404A38	RW	12
Default MB1, Links (95:84), Mask4: RMB_DFLT_LUT(4,7,1)	2E7	00404A3C	RW	12
Corrective MB0, Links (11: 0), Mask4: RMB_CRTV_LUT(4,0,0)	358	00404A40	RW	12
Corrective MB1, Links (11: 0), Mask4: RMB_CRTV_LUT(4,0,1)	359	00404A44	RW	12
Corrective MB0, Links (23:12), Mask4: RMB_CRTV_LUT(4,1,0)	35A	00404A48	RW	12
Corrective MB1, Links (23:12), Mask4: RMB_CRTV_LUT(4,1,1)	35B	00404A4C	RW	12
Corrective MB0, Links (35:24), Mask4: RMB_CRTV_LUT(4,2,0)	35C	00404A50	RW	12
Corrective MB1, Links (35:24), Mask4: RMB_CRTV_LUT(4,2,1)	35D	00404A54	RW	12
Corrective MB0, Links (47:36), Mask4: RMB_CRTV_LUT(4,3,0)	35E	00404A58	RW	12
Corrective MB1, Links (47:36), Mask4: RMB_CRTV_LUT(4,3,1)	35F	00404A5C	RW	12
Corrective MB0, Links (59:48), Mask4: RMB_CRTV_LUT(4,4,0)	360	00404A60	RW	12
Corrective MB1, Links (59:48), Mask4: RMB_CRTV_LUT(4,4,1)	361	00404A64	RW	12
Corrective MB0, Links (71:60), Mask4: RMB_CRTV_LUT(4,5,0)	362	00404A68	RW	12
Corrective MB1, Links (71:60), Mask4: RMB_CRTV_LUT(4,5,1)	363	00404A6C	RW	12
Corrective MB0, Links (83:72), Mask4: RMB_CRTV_LUT(4,6,0)	364	00404A70	RW	12
Corrective MB1, Links (83:72), Mask4: RMB_CRTV_LUT(4,6,1)	365	00404A74	RW	12
Corrective MB0, Links (95:84), Mask4: RMB_CRTV_LUT(4,7,0)	366	00404A78	RW	12
Corrective MB1, Links (95:84), Mask4: RMB_CRTV_LUT(4,7,1)	367	00404A7C	RW	12

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Default MB0, Links (11: 0), Mask5: RMB DFLT LUT(5,0,0)	2E8	00404A80	RW	12
Default MB1, Links (11: 0), Mask5: RMB DFLT LUT(5,0,1)	2E9	00404A84	RW	12
Default MB0, Links (23:12), Mask5: RMB DFLT LUT(5,1,0)	2EA	00404A88	RW	12
Default MB1, Links (23:12), Mask5: RMB DFLT LUT(5,1,1)	2EB	00404A8C	RW	12
Default MB0, Links (35:24), Mask5: RMB DFLT LUT(5,2,0)	2EC	00404A90	RW	12
Default MB1, Links (35:24), Mask5: RMB DFLT LUT(5,2,1)	2ED	00404A94	RW	12
Default MB0, Links (47:36), Mask5: RMB DFLT LUT(5,3,0)	2EE	00404A98	RW	12
Default MB1, Links (47:36), Mask5: RMB DFLT LUT(5,3,1)	2EF	00404A9C	RW	12
Default MB0, Links (59:48), Mask5: RMB DFLT LUT(5,4,0)	2F0	00404AA0	RW	12
Default MB1, Links (59:48), Mask5: RMB DFLT LUT(5,4,1)	2F1	00404AA4	RW	12
Default MB0, Links (71:60), Mask5: RMB DFLT LUT(5,5,0)	2F2	00404AA8	RW	12
Default MB1, Links (71:60), Mask5: RMB DFLT LUT(5,5,1)	2F3	00404AAC	RW	12
Default MB0, Links (83:72), Mask5: RMB DFLT LUT(5,6,0)	2F4	00404AB0	RW	12
Default MB1, Links (83:72), Mask5: RMB DFLT LUT(5,6,1)	2F5	00404AB4	RW	12
Default MB0, Links (95:84), Mask5: RMB DFLT LUT(5,7,0)	2F6	00404AB8	RW	12
Default MB1, Links (95:84), Mask5: RMB DFLT LUT(5,7,1)	2F7	00404ABC	RW	12
Corrective MB0, Links (11: 0), Mask5: RMB CRTV LUT(5,0,0)	368	00404AC0	RW	12
Corrective MB1, Links (11: 0), Mask5: RMB CRTV LUT(5,0,1)	369	00404AC4	RW	12
Corrective MB0, Links (23:12), Mask5: RMB CRTV LUT(5,1,0)	36A	00404AC8	RW	12
Corrective MB1, Links (23:12), Mask5: RMB CRTV LUT(5,1,1)	36B	00404ACC	RW	12
Corrective MB0, Links (35:24), Mask5: RMB CRTV LUT(5,2,0)	36C	00404AD0	RW	12
Corrective MB1, Links (35:24), Mask5: RMB CRTV LUT(5,2,1)	36D	00404AD4	RW	12
Corrective MB0, Links (47:36), Mask5: RMB CRTV LUT(5,3,0)	36E	00404AD8	RW	12
Corrective MB1, Links (47:36), Mask5: RMB CRTV LUT(5,3,1)	36F	00404ADC	RW	12
Corrective MB0, Links (59:48), Mask5: RMB CRTV LUT(5,4,0)	370	00404AE0	RW	12
Corrective MB1, Links (59:48), Mask5: RMB CRTV LUT(5,4,1)	371	00404AE4	RW	12
Corrective MB0, Links (71:60), Mask5: RMB CRTV LUT(5,5,0)	372	00404AE8	RW	12
Corrective MB1, Links (71:60), Mask5: RMB CRTV LUT(5,5,1)	373	00404AEC	RW	12
Corrective MB0, Links (83:72), Mask5: RMB CRTV LUT(5,6,0)	374	00404AF0	RW	12
Corrective MB1, Links (83:72), Mask5: RMB CRTV LUT(5,6,1)	375	00404AF4	RW	12
Corrective MB0, Links (95:84), Mask5: RMB CRTV LUT(5,7,0)	376	00404AF8	RW	12
Corrective MB1, Links (95:84), Mask5: RMB CRTV LUT(5,7,1)	377	00404AFC	RW	12
Default MB0, Links (11: 0), Mask6: RMB DFLT LUT(6,0,0)	2F8	00404B00	RW	12
Default MB1, Links (11: 0), Mask6: RMB DFLT LUT(6,0,1)	2F9	00404B04	RW	12
Default MB0, Links (23:12), Mask6: RMB DFLT LUT(6,1,0)	2FA	00404B08	RW	12
Default MB1, Links (23:12), Mask6: RMB DFLT LUT(6,1,1)	2FB	00404B0C	RW	12
Default MB0, Links (35:24), Mask6: RMB DFLT LUT(6,2,0)	2FC	00404B10	RW	12
Default MB1, Links (35:24), Mask6: RMB DFLT LUT(6,2,1)	2FD	00404B14	RW	12
Default MB0, Links (47:36), Mask6: RMB DFLT LUT(6,3,0)	2FE	00404B18	RW	12
Default MB1, Links (47:36), Mask6: RMB DFLT LUT(6,3,1)	2FF	00404B1C	RW	12
Default MB0, Links (59:48), Mask6: RMB DFLT LUT(6,4,0)	300	00404B20	RW	12
Default MB1, Links (59:48), Mask6: RMB DFLT LUT(6,4,1)	301	00404B24	RW	12
Default MB0, Links (71:60), Mask6: RMB DFLT LUT(6,5,0)	302	00404B28	RW	12
Default MB1, Links (71:60), Mask6: RMB DFLT LUT(6,5,1)	303	00404B2C	RW	12
Default MB0, Links (83:72), Mask6: RMB DFLT LUT(6,6,0)	304	00404B30	RW	12
Default MB1, Links (83:72), Mask6: RMB DFLT LUT(6,6,1)	305	00404B34	RW	12
Default MB0, Links (95:84), Mask6: RMB DFLT LUT(6,7,0)	306	00404B38	RW	12
Default MB1, Links (95:84), Mask6: RMB DFLT LUT(6,7,1)	307	00404B3C	RW	12
Corrective MB0, Links (11: 0), Mask6: RMB CRTV LUT(6,0,0)	378	00404B40	RW	12
Corrective MB1, Links (11: 0), Mask6: RMB CRTV LUT(6,0,1)	379	00404B44	RW	12
Corrective MB0, Links (23:12), Mask6: RMB CRTV LUT(6,1,0)	37A	00404B48	RW	12
Corrective MB1, Links (23:12), Mask6: RMB CRTV LUT(6,1,1)	37B	00404B4C	RW	12
Corrective MB0, Links (35:24), Mask6: RMB CRTV LUT(6,2,0)	37C	00404B50	RW	12
Corrective MB1, Links (35:24), Mask6: RMB CRTV LUT(6,2,1)	37D	00404B54	RW	12
Corrective MB0, Links (47:36), Mask6: RMB CRTV LUT(6,3,0)	37E	00404B58	RW	12
Corrective MB1, Links (47:36), Mask6: RMB CRTV LUT(6,3,1)	37F	00404B5C	RW	12
Corrective MB0, Links (59:48), Mask6: RMB CRTV LUT(6,4,0)	380	00404B60	RW	12
Corrective MB1, Links (59:48), Mask6: RMB CRTV LUT(6,4,1)	381	00404B64	RW	12
Corrective MB0, Links (71:60), Mask6: RMB CRTV LUT(6,5,0)	382	00404B68	RW	12
Corrective MB1, Links (71:60), Mask6: RMB CRTV LUT(6,5,1)	383	00404B6C	RW	12
Corrective MB0, Links (83:72), Mask6: RMB CRTV LUT(6,6,0)	384	00404B70	RW	12
Corrective MB1, Links (83:72), Mask6: RMB CRTV LUT(6,6,1)	385	00404B74	RW	12
Corrective MB0, Links (95:84), Mask6: RMB CRTV LUT(6,7,0)	386	00404B78	RW	12
Corrective MB1, Links (95:84), Mask6: RMB CRTV LUT(6,7,1)	387	00404B7C	RW	12

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Default MB0, Links (11: 0), Mask7: RMB_DFLT_LUT(7,0,0)	308	00404B80	RW	12
Default MB1, Links (11: 0), Mask7: RMB_DFLT_LUT(7,0,1)	309	00404B84	RW	12
Default MB0, Links (23:12), Mask7: RMB_DFLT_LUT(7,1,0)	30A	00404B88	RW	12
Default MB1, Links (23:12), Mask7: RMB_DFLT_LUT(7,1,1)	30B	00404B8C	RW	12
Default MB0, Links (35:24), Mask7: RMB_DFLT_LUT(7,2,0)	30C	00404B90	RW	12
Default MB1, Links (35:24), Mask7: RMB_DFLT_LUT(7,2,1)	30D	00404B94	RW	12
Default MB0, Links (47:36), Mask7: RMB_DFLT_LUT(7,3,0)	30E	00404B98	RW	12
Default MB1, Links (47:36), Mask7: RMB_DFLT_LUT(7,3,1)	30F	00404B9C	RW	12
Default MB0, Links (59:48), Mask7: RMB_DFLT_LUT(7,4,0)	310	00404BA0	RW	12
Default MB1, Links (59:48), Mask7: RMB_DFLT_LUT(7,4,1)	311	00404BA4	RW	12
Default MB0, Links (71:60), Mask7: RMB_DFLT_LUT(7,5,0)	312	00404BA8	RW	12
Default MB1, Links (71:60), Mask7: RMB_DFLT_LUT(7,5,1)	313	00404BAC	RW	12
Default MB0, Links (83:72), Mask7: RMB_DFLT_LUT(7,6,0)	314	00404BB0	RW	12
Default MB1, Links (83:72), Mask7: RMB_DFLT_LUT(7,6,1)	315	00404BB4	RW	12
Default MB0, Links (95:84), Mask7: RMB_DFLT_LUT(7,7,0)	316	00404BB8	RW	12
Default MB1, Links (95:84), Mask7: RMB_DFLT_LUT(7,7,1)	317	00404BBC	RW	12
Corrective MB0, Links (11: 0), Mask7: RMB_CRTV_LUT(7,0,0)	388	00404BC0	RW	12
Corrective MB1, Links (11: 0), Mask7: RMB_CRTV_LUT(7,0,1)	389	00404BC4	RW	12
Corrective MB0, Links (23:12), Mask7: RMB_CRTV_LUT(7,1,0)	38A	00404BC8	RW	12
Corrective MB1, Links (23:12), Mask7: RMB_CRTV_LUT(7,1,1)	38B	00404BCC	RW	12
Corrective MB0, Links (35:24), Mask7: RMB_CRTV_LUT(7,2,0)	38C	00404BD0	RW	12
Corrective MB1, Links (35:24), Mask7: RMB_CRTV_LUT(7,2,1)	38D	00404BD4	RW	12
Corrective MB0, Links (47:36), Mask7: RMB_CRTV_LUT(7,3,0)	38E	00404BD8	RW	12
Corrective MB1, Links (47:36), Mask7: RMB_CRTV_LUT(7,3,1)	38F	00404BDC	RW	12
Corrective MB0, Links (59:48), Mask7: RMB_CRTV_LUT(7,4,0)	390	00404BE0	RW	12
Corrective MB1, Links (59:48), Mask7: RMB_CRTV_LUT(7,4,1)	391	00404BE4	RW	12
Corrective MB0, Links (71:60), Mask7: RMB_CRTV_LUT(7,5,0)	392	00404BE8	RW	12
Corrective MB1, Links (71:60), Mask7: RMB_CRTV_LUT(7,5,1)	393	00404BEC	RW	12
Corrective MB0, Links (83:72), Mask7: RMB_CRTV_LUT(7,6,0)	394	00404BF0	RW	12
Corrective MB1, Links (83:72), Mask7: RMB_CRTV_LUT(7,6,1)	395	00404BF4	RW	12
Corrective MB0, Links (95:84), Mask7: RMB_CRTV_LUT(7,7,0)	396	00404BF8	RW	12
Corrective MB1, Links (95:84), Mask7: RMB_CRTV_LUT(7,7,1)	397	00404BFC	RW	12

# APPENDIX A: ROD and BOC FPGA Register Definitions

## 7 ROD Diagnostic Memory FIFO Registers

### 7.1 Input Memory FIFO Registers

Description	Address	Access	Width
Input Memory FIFO A: Low Order Word Write Register	00406000	RW	32
			Bit Value
Bits[31: 0]: LSW Value			Value

Description	Address	Access	Width
Input Memory FIFO A: High Order Word Write Register	00406004	RW	16
			Bit Value
Bits[15: 0]: MSW Value			Value

Description	Address	Access	Width
Input Memory FIFO B: Low Order Word Write Register	00406008	RW	32
			Bit Value
Bits[31: 0]: LSW Value			Value

Description	Address	Access	Width
Input Memory FIFO B: High Order Word Write Register	0040600C	RW	16
			Bit Value
Bits[15: 0]: MSW Value			Value

Description	Address	Access	Width
Input Memory FIFO A: Low Order Word Read Register	00406020	R	32
			Bit Value
Bits[31: 0]: LSW Value			Value

Description	Address	Access	Width
Input Memory FIFO A: High Order Word Read Register	00406024	R	16
			Bit Value
Bits[15: 0]: MSW Value			Value

Description	Address	Access	Width
Input Memory FIFO B: Low Order Word Read Register	00406028	R	32
			Bit Value
Bits[31: 0]: LSW Value			Value

Description	Address	Access	Width
Input Memory FIFO B: High Order Word Read Register	0040602C	R	16
			Bit Value
Bits[15: 0]: MSW Value			Value

Description	Address	Access	Width
Input Memory FIFO A: Advance FIFO A	00406040	RW	1
A write operation to this register writes the value in the Write Register for FIFO A into the FIFO. A read operation to this register loads the data from the FIFO into the Read Register. The bit value of this register is ignored.			Bit Value
Bit 0: Advance 1 Word			1 0 ADV IDLE

Description	Address	Access	Width
Input Memory FIFO B: Advance FIFO B	00406048	RW	1
A write operation to this register writes the value in the Write Register for FIFO A into the FIFO. A read operation to this register loads the data from the FIFO into the Read Register. The bit value of this register is ignored.			Bit Value
Bit 0: Advance 1 Word			1 0 ADV IDLE



## APPENDIX A: ROD and BOC FPGA Register Definitions

### 7.2 Event Memory FIFO Registers

Description	Address	Access	Width
Event Memory FIFO A: Low Order Word Read Register	00406120	R	32
		Bit Value	
Bits[31: 0]: LSW Value		Value	
Description	Address	Access	Width
Event Memory FIFO A: High Order Word Read Register	00406124	R	16
		Bit Value	
Bits[15: 0]: MSW Value		Value	
Description	Address	Access	Width
Event Memory FIFO B: Low Order Word Read Register	00406128	R	32
		Bit Value	
Bits[31: 0]: LSW Value		Value	
Description	Address	Access	Width
Event Memory FIFO B: High Order Word Read Register	0040612C	R	16
		Bit Value	
Bits[15: 0]: MSW Value		Value	
Description	Address	Access	Width
Event Memory FIFO C: Word Read Register	00406130	R	32
		Bit Value	
Bits[31: 0]: Value		Value	
Description	Address	Access	Width
Event Memory FIFO A: Advance FIFO A	00406140	R	1
A read operation to this register loads the data from the FIFO into the Read Register. A write operation to this register is ignored. The bit value of this register is ignored.		Bit Value	
Bit 0: Advance 1 Word		1	0
		ADV	IDLE
Description	Address	Access	Width
Event Memory FIFO B: Advance FIFO B	00406148	R	1
A read operation to this register loads the data from the FIFO into the Read Register. A write operation to this register is ignored. The bit value of this register is ignored.		Bit Value	
Bit 0: Advance 1 Word		1	0
		ADV	IDLE
Description	Address	Access	Width
Event Memory FIFO C: Advance FIFO C	00406150	R	1
A read operation to this register loads the data from the FIFO into the Read Register. A write operation to this register is ignored. The bit value of this register is ignored.		Bit Value	
Bit 0: Advance 1 Word		1	0
		ADV	IDLE

# APPENDIX A: ROD and BOC FPGA Register Definitions

## 8 BOC Registers

### BOC1 Set-Up Bus Top Level Address Map

Mnemonic	VME Add (Hex)	SetUpBus Add (hex)	Function	Mnemonic	VME Add (Hex)	SetUpBus Add (hex)	Function			
TXDACS:	00408600	200	Unused	CREGS:	00408F00	400	BOC Control Registers			
		1E0				Reserved		3E0		
		1C0						3C0		
		1A0	TX Laser Current DACs			3A0	Reserved			
		180	Reserved			380	Monitoring(series)			
		160				360	Reserved			
		140				RX Threshold DACs	340			
		120					320			
		100					300			
		0F0				BPM12_3 Lasers[47:36]	RXDACS:	00408C00	2E0	Strobe Delays
		0E0	Reserved						2C0	
		0D0							2A0	
0C0	BPM12_2 Lasers[35:24]	00408A00	280							
0B0		Reserved	CLK_PHASES:	00408980	260				Clock Phases	
0A0	BPM12_1 Lasers[23:12]		00408800	240	Delays					
090		00408800	220							
080	BPM12_0 Lasers[11:0]	RXDDELAYS:	00408800	200						
070		00408800								
060										
050										
040										
030										
020										
010										
000										
BPMS:	00408000	000								

## APPENDIX A: ROD and BOC FPGA Register Definitions

### 8.1 FE Command Stream Control Registers

Description	REG ID	Address	Access	Width
FE Command Stream 0: Stream Inhibit		00408000	RW	1
FE Command Stream 1: Stream Inhibit		00408010		
FE Command Stream 2: Stream Inhibit		00408020		
FE Command Stream 3: Stream Inhibit		00408030		
FE Command Stream 4: Stream Inhibit		00408040		
FE Command Stream 5: Stream Inhibit		00408050		
FE Command Stream 6: Stream Inhibit		00408060		
FE Command Stream 7: Stream Inhibit		00408070		
FE Command Stream 8: Stream Inhibit		00408080		
FE Command Stream 9: Stream Inhibit		00408090		
FE Command Stream 10: Stream Inhibit		004080A0		
FE Command Stream 11: Stream Inhibit		004080B0		
FE Command Stream 12: Stream Inhibit		00408100		
FE Command Stream 13: Stream Inhibit		00408110		
FE Command Stream 14: Stream Inhibit		00408120		
FE Command Stream 15: Stream Inhibit		00408130		
FE Command Stream 16: Stream Inhibit		00408140		
FE Command Stream 17: Stream Inhibit		00408150		
FE Command Stream 18: Stream Inhibit		00408160		
FE Command Stream 19: Stream Inhibit		00408170		
FE Command Stream 20: Stream Inhibit		00408180		
FE Command Stream 21: Stream Inhibit		00408190		
FE Command Stream 22: Stream Inhibit		004081A0		
FE Command Stream 23: Stream Inhibit		004081B0		
FE Command Stream 24: Stream Inhibit		00408200		
FE Command Stream 25: Stream Inhibit		00408210		
FE Command Stream 26: Stream Inhibit		00408220		
FE Command Stream 27: Stream Inhibit		00408230		
FE Command Stream 28: Stream Inhibit		00408240		
FE Command Stream 29: Stream Inhibit		00408250		
FE Command Stream 30: Stream Inhibit		00408260		
FE Command Stream 31: Stream Inhibit		00408270		
FE Command Stream 32: Stream Inhibit		00408280		
FE Command Stream 33: Stream Inhibit		00408290		
FE Command Stream 34: Stream Inhibit		004082A0		
FE Command Stream 35: Stream Inhibit		004082B0		
FE Command Stream 36: Stream Inhibit		00408300		
FE Command Stream 37: Stream Inhibit		00408310		
FE Command Stream 38: Stream Inhibit		00408320		
FE Command Stream 39: Stream Inhibit		00408330		
FE Command Stream 40: Stream Inhibit		00408340		
FE Command Stream 41: Stream Inhibit		00408350		
FE Command Stream 42: Stream Inhibit		00408360		
FE Command Stream 43: Stream Inhibit		00408370		
FE Command Stream 44: Stream Inhibit		00408380		
FE Command Stream 45: Stream Inhibit		00408390		
FE Command Stream 46: Stream Inhibit		004083A0		
FE Command Stream 47: Stream Inhibit		004083B0		
			<b>Bit Value</b>	
Bit to inhibit output of optical data streams			1	0
Bit 0: Stream Inhibit (Reset Value = 0)			Inhibit	Enabled

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
FE Command Stream 0: Mark Space		00408004	RW	5
FE Command Stream 1: Mark Space		00408014		
FE Command Stream 2: Mark Space		00408024		
FE Command Stream 3: Mark Space		00408034		
FE Command Stream 4: Mark Space		00408044		
FE Command Stream 5: Mark Space		00408054		
FE Command Stream 6: Mark Space		00408064		
FE Command Stream 7: Mark Space		00408074		
FE Command Stream 8: Mark Space		00408084		
FE Command Stream 9: Mark Space		00408094		
FE Command Stream 10: Mark Space		004080A4		
FE Command Stream 11: Mark Space		004080B4		
FE Command Stream 12: Mark Space		00408104		
FE Command Stream 13: Mark Space		00408114		
FE Command Stream 14: Mark Space		00408124		
FE Command Stream 15: Mark Space		00408134		
FE Command Stream 16: Mark Space		00408144		
FE Command Stream 17: Mark Space		00408154		
FE Command Stream 18: Mark Space		00408164		
FE Command Stream 19: Mark Space		00408174		
FE Command Stream 20: Mark Space		00408184		
FE Command Stream 21: Mark Space		00408194		
FE Command Stream 22: Mark Space		004081A4		
FE Command Stream 23: Mark Space		004081B4		
FE Command Stream 24: Mark Space		00408204		
FE Command Stream 25: Mark Space		00408214		
FE Command Stream 26: Mark Space		00408224		
FE Command Stream 27: Mark Space		00408234		
FE Command Stream 28: Mark Space		00408244		
FE Command Stream 29: Mark Space		00408254		
FE Command Stream 30: Mark Space		00408264		
FE Command Stream 31: Mark Space		00408274		
FE Command Stream 32: Mark Space		00408284		
FE Command Stream 33: Mark Space		00408294		
FE Command Stream 34: Mark Space		004082A4		
FE Command Stream 35: Mark Space		004082B4		
FE Command Stream 36: Mark Space		00408304		
FE Command Stream 37: Mark Space		00408314		
FE Command Stream 38: Mark Space		00408324		
FE Command Stream 39: Mark Space		00408334		
FE Command Stream 40: Mark Space		00408344		
FE Command Stream 41: Mark Space		00408354		
FE Command Stream 42: Mark Space		00408364		
FE Command Stream 43: Mark Space		00408374		
FE Command Stream 44: Mark Space		00408384		
FE Command Stream 45: Mark Space		00408394		
FE Command Stream 46: Mark Space		004083A4		
FE Command Stream 47: Mark Space		004083B4		
			Bit Value	
Bits[4:0]: Mark Space (Reset Value = 0x13 /~50%)			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
FE Command Stream 0: Coarse Delay		00408008	RW	5
FE Command Stream 1: Coarse Delay		00408018		
FE Command Stream 2: Coarse Delay		00408028		
FE Command Stream 3: Coarse Delay		00408038		
FE Command Stream 4: Coarse Delay		00408048		
FE Command Stream 5: Coarse Delay		00408058		
FE Command Stream 6: Coarse Delay		00408068		
FE Command Stream 7: Coarse Delay		00408078		
FE Command Stream 8: Coarse Delay		00408088		
FE Command Stream 9: Coarse Delay		00408098		
FE Command Stream 10: Coarse Delay		004080A8		
FE Command Stream 11: Coarse Delay		004080B8		
FE Command Stream 12: Coarse Delay		00408108		
FE Command Stream 13: Coarse Delay		00408118		
FE Command Stream 14: Coarse Delay		00408128		
FE Command Stream 15: Coarse Delay		00408138		
FE Command Stream 16: Coarse Delay		00408148		
FE Command Stream 17: Coarse Delay		00408158		
FE Command Stream 18: Coarse Delay		00408168		
FE Command Stream 19: Coarse Delay		00408178		
FE Command Stream 20: Coarse Delay		00408188		
FE Command Stream 21: Coarse Delay		00408198		
FE Command Stream 22: Coarse Delay		004081A8		
FE Command Stream 23: Coarse Delay		004081B8		
FE Command Stream 24: Coarse Delay		00408208		
FE Command Stream 25: Coarse Delay		00408218		
FE Command Stream 26: Coarse Delay		00408228		
FE Command Stream 27: Coarse Delay		00408238		
FE Command Stream 28: Coarse Delay		00408248		
FE Command Stream 29: Coarse Delay		00408258		
FE Command Stream 30: Coarse Delay		00408268		
FE Command Stream 31: Coarse Delay		00408278		
FE Command Stream 32: Coarse Delay		00408288		
FE Command Stream 33: Coarse Delay		00408298		
FE Command Stream 34: Coarse Delay		004082A8		
FE Command Stream 35: Coarse Delay		004082B8		
FE Command Stream 36: Coarse Delay		00408308		
FE Command Stream 37: Coarse Delay		00408318		
FE Command Stream 38: Coarse Delay		00408328		
FE Command Stream 39: Coarse Delay		00408338		
FE Command Stream 40: Coarse Delay		00408348		
FE Command Stream 41: Coarse Delay		00408358		
FE Command Stream 42: Coarse Delay		00408368		
FE Command Stream 43: Coarse Delay		00408378		
FE Command Stream 44: Coarse Delay		00408388		
FE Command Stream 45: Coarse Delay		00408398		
FE Command Stream 46: Coarse Delay		004083A8		
FE Command Stream 47: Coarse Delay		004083B8		
Value that determines the coarse timing delay of the FE Command signal in 25 nsec steps (775 nsec maximum)			<b>Bit Value</b>	
Bits[4:0]: Coarse Delay (Reset Value = 0)			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
FE Command Stream 0: Fine Delay		0040800C	RW	7
FE Command Stream 1: Fine Delay		0040801C		
FE Command Stream 2: Fine Delay		0040802C		
FE Command Stream 3: Fine Delay		0040803C		
FE Command Stream 4: Fine Delay		0040804C		
FE Command Stream 5: Fine Delay		0040805C		
FE Command Stream 6: Fine Delay		0040806C		
FE Command Stream 7: Fine Delay		0040807C		
FE Command Stream 8: Fine Delay		0040808C		
FE Command Stream 9: Fine Delay		0040809C		
FE Command Stream 10: Fine Delay		004080AC		
FE Command Stream 11: Fine Delay		004080BC		
FE Command Stream 12: Fine Delay		0040810C		
FE Command Stream 13: Fine Delay		0040811C		
FE Command Stream 14: Fine Delay		0040812C		
FE Command Stream 15: Fine Delay		0040813C		
FE Command Stream 16: Fine Delay		0040814C		
FE Command Stream 17: Fine Delay		0040815C		
FE Command Stream 18: Fine Delay		0040816C		
FE Command Stream 19: Fine Delay		0040817C		
FE Command Stream 20: Fine Delay		0040818C		
FE Command Stream 21: Fine Delay		0040819C		
FE Command Stream 22: Fine Delay		004081AC		
FE Command Stream 23: Fine Delay		004081BC		
FE Command Stream 24: Fine Delay		0040820C		
FE Command Stream 25: Fine Delay		0040821C		
FE Command Stream 26: Fine Delay		0040822C		
FE Command Stream 27: Fine Delay		0040823C		
FE Command Stream 28: Fine Delay		0040824C		
FE Command Stream 29: Fine Delay		0040825C		
FE Command Stream 30: Fine Delay		0040826C		
FE Command Stream 31: Fine Delay		0040827C		
FE Command Stream 32: Fine Delay		0040828C		
FE Command Stream 33: Fine Delay		0040829C		
FE Command Stream 34: Fine Delay		004082AC		
FE Command Stream 35: Fine Delay		004082BC		
FE Command Stream 36: Fine Delay		0040830C		
FE Command Stream 37: Fine Delay		0040831C		
FE Command Stream 38: Fine Delay		0040832C		
FE Command Stream 39: Fine Delay		0040833C		
FE Command Stream 40: Fine Delay		0040834C		
FE Command Stream 41: Fine Delay		0040835C		
FE Command Stream 42: Fine Delay		0040836C		
FE Command Stream 43: Fine Delay		0040837C		
FE Command Stream 44: Fine Delay		0040838C		
FE Command Stream 45: Fine Delay		0040839C		
FE Command Stream 46: Fine Delay		004083AC		
FE Command Stream 47: Fine Delay		004083BC		
Value that determines the fine timing delay of the FE Command signal in 280 psec steps (35 nsec maximum)			<b>Bit Value</b>	
Bits[6:0]: Fine Delay (Reset Value = 0)			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

### 8.2 BPM Laser BPM Test Structure Registers

Description	REG ID	Address	Access	Width
BPM12 Test Structures: 1 <sup>st</sup> BPM12, channel 12		004080C0	RW	8
				Bit Value
Bits[7:0]: Must be set to 0x20 for proper operation of BPM12				Value

Description	REG ID	Address	Access	Width
BPM12 Test Structures: 1 <sup>st</sup> BPM12, channel 13		004080D0	RW	8
				Bit Value
Bits[7:0]: Must be set to 0x40 for proper operation of BPM12				Value

Description	REG ID	Address	Access	Width
BPM12 Test Structures: 2 <sup>nd</sup> BPM12, channel 12		004081C0	RW	8
				Bit Value
Bits[7:0]: Must be set to 0x20 for proper operation of BPM12				Value

Description	REG ID	Address	Access	Width
BPM12 Test Structures: 2 <sup>nd</sup> BPM12, channel 13		004081D0	RW	8
				Bit Value
Bits[7:0]: Must be set to 0x40 for proper operation of BPM12				Value

Description	REG ID	Address	Access	Width
BPM12 Test Structures: 3 <sup>rd</sup> BPM12, channel 12		004082C0	RW	8
				Bit Value
Bits[7:0]: Must be set to 0x20 for proper operation of BPM12				Value

Description	REG ID	Address	Access	Width
BPM12 Test Structures: 3 <sup>rd</sup> BPM12, channel 13		004082D0	RW	8
				Bit Value
Bits[7:0]: Must be set to 0x40 for proper operation of BPM12				Value

Description	REG ID	Address	Access	Width
BPM12 Test Structures: 4 <sup>th</sup> BPM12, channel 12		004083C0	RW	8
				Bit Value
Bits[7:0]: Must be set to 0x20 for proper operation of BPM12				Value

Description	REG ID	Address	Access	Width
BPM12 Test Structures: 4 <sup>th</sup> BPM12, channel 13		004083D0	RW	8
				Bit Value
Bits[7:0]: Must be set to 0x40 for proper operation of BPM12				Value

# APPENDIX A: ROD and BOC FPGA Register Definitions

## 8.3 FE Command Laser Current DAC Registers

Description	REG ID	Address	Access	Width
FE Command Stream 0: Laser Current DAC		00408600	RW	8
FE Command Stream 1: Laser Current DAC		00408604		
FE Command Stream 2: Laser Current DAC		00408608		
FE Command Stream 3: Laser Current DAC		0040860C		
FE Command Stream 4: Laser Current DAC		00408610		
FE Command Stream 5: Laser Current DAC		00408610		
FE Command Stream 6: Laser Current DAC		00408610		
FE Command Stream 7: Laser Current DAC		00408610		
FE Command Stream 8: Laser Current DAC		00408620		
FE Command Stream 9: Laser Current DAC		00408620		
FE Command Stream 10: Laser Current DAC		00408620		
FE Command Stream 11: Laser Current DAC		00408620		
FE Command Stream 12: Laser Current DAC		00408630		
FE Command Stream 13: Laser Current DAC		00408630		
FE Command Stream 14: Laser Current DAC		00408630		
FE Command Stream 15: Laser Current DAC		00408630		
FE Command Stream 16: Laser Current DAC		00408640		
FE Command Stream 17: Laser Current DAC		00408640		
FE Command Stream 18: Laser Current DAC		00408640		
FE Command Stream 19: Laser Current DAC		00408640		
FE Command Stream 20: Laser Current DAC		00408650		
FE Command Stream 21: Laser Current DAC		00408650		
FE Command Stream 22: Laser Current DAC		00408650		
FE Command Stream 23: Laser Current DAC		00408650		
FE Command Stream 24: Laser Current DAC		00408660		
FE Command Stream 25: Laser Current DAC		00408660		
FE Command Stream 26: Laser Current DAC		00408660		
FE Command Stream 27: Laser Current DAC		00408660		
FE Command Stream 28: Laser Current DAC		00408670		
FE Command Stream 29: Laser Current DAC		00408670		
FE Command Stream 30: Laser Current DAC		00408670		
FE Command Stream 31: Laser Current DAC		00408670		
FE Command Stream 32: Laser Current DAC		00408680		
FE Command Stream 33: Laser Current DAC		00408680		
FE Command Stream 34: Laser Current DAC		00408680		
FE Command Stream 35: Laser Current DAC		00408680		
FE Command Stream 36: Laser Current DAC		00408690		
FE Command Stream 37: Laser Current DAC		00408690		
FE Command Stream 38: Laser Current DAC		00408690		
FE Command Stream 39: Laser Current DAC		00408690		
FE Command Stream 40: Laser Current DAC		004086A0		
FE Command Stream 41: Laser Current DAC		004086A0		
FE Command Stream 42: Laser Current DAC		004086A0		
FE Command Stream 43: Laser Current DAC		004086A0		
FE Command Stream 44: Laser Current DAC		004086B0		
FE Command Stream 45: Laser Current DAC		004086B0		
FE Command Stream 46: Laser Current DAC		004086B0		
FE Command Stream 47: Laser Current DAC		004086B0		
Value that determines the current out of the Laser Current DAC			<b>Bit Value</b>	
Bits[7:0]: Laser Current Value			Value	



## APPENDIX A: ROD and BOC FPGA Register Definitions

### 8.4 FE Link Input Data Delay Registers

Description	REG ID	Address	Access	Width
Input Link 0: Data Delay		00408800	RW	5
Input Link 1: Data Delay		00408804		
Input Link 2: Data Delay		00408808		
Input Link 3: Data Delay		0040880C		
Input Link 4: Data Delay		00408810		
Input Link 5: Data Delay		00408814		
Input Link 6: Data Delay		00408818		
Input Link 7: Data Delay		0040881C		
Input Link 8: Data Delay		00408820		
Input Link 9: Data Delay		00408824		
Input Link 10: Data Delay		00408828		
Input Link 11: Data Delay		0040882C		
Input Link 12: Data Delay		00408830		
Input Link 13: Data Delay		00408834		
Input Link 14: Data Delay		00408838		
Input Link 15: Data Delay		0040883C		
Input Link 16: Data Delay		00408840		
Input Link 17: Data Delay		00408844		
Input Link 18: Data Delay		00408848		
Input Link 19: Data Delay		0040884C		
Input Link 20: Data Delay		00408850		
Input Link 21: Data Delay		00408854		
Input Link 22: Data Delay		00408858		
Input Link 23: Data Delay		0040885C		
Input Link 24: Data Delay		00408860		
Input Link 25: Data Delay		00408864		
Input Link 26: Data Delay		00408868		
Input Link 27: Data Delay		0040886C		
Input Link 28: Data Delay		00408870		
Input Link 29: Data Delay		00408874		
Input Link 30: Data Delay		00408878		
Input Link 31: Data Delay		0040887C		
Input Link 32: Data Delay		00408880		
Input Link 33: Data Delay		00408884		
Input Link 34: Data Delay		00408888		
Input Link 35: Data Delay		0040888C		
Input Link 36: Data Delay		00408890		
Input Link 37: Data Delay		00408894		
Input Link 38: Data Delay		00408898		
Input Link 39: Data Delay		0040889C		
Input Link 40: Data Delay		004088A0		
Input Link 41: Data Delay		004088A4		
Input Link 42: Data Delay		004088A8		
Input Link 43: Data Delay		004088AC		
Input Link 44: Data Delay		004088B0		
Input Link 45: Data Delay		004088B4		
Input Link 46: Data Delay		004088B8		
Input Link 47: Data Delay		004088BC		
			<b>Bit Value</b>	
<b>Bits[4:0]:</b> Data Delay Value			Delay in ns	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Input Link 48: Data Delay		004088C0	RW	5
Input Link 49: Data Delay		004088C4		
Input Link 50: Data Delay		004088C8		
Input Link 51: Data Delay		004088CC		
Input Link 52: Data Delay		004088D0		
Input Link 53: Data Delay		004088D4		
Input Link 54: Data Delay		004088D8		
Input Link 55: Data Delay		004088DC		
Input Link 56: Data Delay		004088E0		
Input Link 57: Data Delay		004088E4		
Input Link 58: Data Delay		004088E8		
Input Link 59: Data Delay		004088EC		
Input Link 60: Data Delay		004088F0		
Input Link 61: Data Delay		004088F4		
Input Link 62: Data Delay		004088F8		
Input Link 63: Data Delay		004088FC		
Input Link 64: Data Delay		00408900		
Input Link 65: Data Delay		00408904		
Input Link 66: Data Delay		00408908		
Input Link 67: Data Delay		0040890C		
Input Link 68: Data Delay		00408910		
Input Link 69: Data Delay		00408914		
Input Link 70: Data Delay		00408918		
Input Link 71: Data Delay		0040891C		
Input Link 72: Data Delay		00408920		
Input Link 73: Data Delay		00408924		
Input Link 74: Data Delay		00408928		
Input Link 75: Data Delay		0040892C		
Input Link 76: Data Delay		00408930		
Input Link 77: Data Delay		00408934		
Input Link 78: Data Delay		00408938		
Input Link 79: Data Delay		0040893C		
Input Link 80: Data Delay		00408940		
Input Link 81: Data Delay		00408944		
Input Link 82: Data Delay		00408948		
Input Link 83: Data Delay		0040894C		
Input Link 84: Data Delay		00408950		
Input Link 85: Data Delay		00408954		
Input Link 86: Data Delay		00408958		
Input Link 87: Data Delay		0040895C		
Input Link 88: Data Delay		00408960		
Input Link 89: Data Delay		00408964		
Input Link 90: Data Delay		00408968		
Input Link 91: Data Delay		0040896C		
Input Link 92: Data Delay		00408970		
Input Link 93: Data Delay		00408974		
Input Link 94: Data Delay		00408978		
Input Link 95: Data Delay		0040897C		
			<b>Bit Value</b>	
<b>Bits[4:0]:</b> Data Delay Value			Delay in ns	

## APPENDIX A: ROD and BOC FPGA Register Definitions

### 8.5 BPM Clock Phase and Vernier Registers

Description	REG ID	Address	Access	Width
BPM Clock Phase		00408980	RW	8
			Bit Value	
Bits[7:0]:			Delay	

Description	REG ID	Address	Access	Width
B-Reg Clock Phase		0040898C	RW	8
			Bit Value	
Bits[7:0]:			Delay	

Description	REG ID	Address	Access	Width
Vernier Clock Step Phase0		00408990	RW	5
This and the following register are in series, giving a delay of 0-50 nsec			Bit Value	
Bits[4:0]: Clock Delay Value			Delay in ns	

Description	REG ID	Address	Access	Width
Vernier Clock Step Phase1		00408994	RW	5
This and the previous register are in series, giving a delay of 0-50 nsec			Bit Value	
Bits[4:0]: Clock Delay Value			Delay in ns	

### 8.6 Strobe Delay Registers

Description	REG ID	Address	Access	Width
Strobe Delay 0		00408A00	RW	1
Strobe Delay 1		00408A10		
Strobe Delay 2		00408A20		
Strobe Delay 3		00408A30		
Strobe Delay 4		00408A40		
Strobe Delay 5		00408A50		
Strobe Delay 6		00408A60		
Strobe Delay 7		00408A70		
Strobe Delay 8		00408A80		
Strobe Delay 9		00408A90		
Strobe Delay 10		00408AA0		
Strobe Delay 11		00408AB0		
Strobe Delay 12		00408AC0		
Strobe Delay 13		00408AD0		
Strobe Delay 14		00408AE0		
Strobe Delay 15		00408AF0		
Strobe Delay 16		00408B00		
Strobe Delay 17		00408B10		
Strobe Delay 18		00408B20		
Strobe Delay 19		00408B30		
Strobe Delay 20		00408B40		
Strobe Delay 21		00408B50		
Strobe Delay 22		00408B60		
Strobe Delay 23		00408B70		
Strobe Delay 24		00408B80		
Strobe Delay 25		00408B90		
			Bit Value	
Adds a delay to the clock output from PHOS4 chip				
Bits[4:0]: Clock Delay Value			Delay in ns	

## APPENDIX A: ROD and BOC FPGA Register Definitions

### 8.7 FE Link Input RX DAC Threshold Registers

Description	REG ID	Address	Access	Width
Input Link 0: RX DAC Threshold		00408C00	RW	8
Input Link 1: RX DAC Threshold		00408C04		
Input Link 2: RX DAC Threshold		00408C08		
Input Link 3: RX DAC Threshold		00408C0C		
Input Link 4: RX DAC Threshold		00408C10		
Input Link 5: RX DAC Threshold		00408C14		
Input Link 6: RX DAC Threshold		00408C18		
Input Link 7: RX DAC Threshold		00408C1C		
Input Link 8: RX DAC Threshold		00408C20		
Input Link 9: RX DAC Threshold		00408C24		
Input Link 10: RX DAC Threshold		00408C28		
Input Link 11: RX DAC Threshold		00408C2C		
Input Link 12: RX DAC Threshold		00408C30		
Input Link 13: RX DAC Threshold		00408C34		
Input Link 14: RX DAC Threshold		00408C38		
Input Link 15: RX DAC Threshold		00408C3C		
Input Link 16: RX DAC Threshold		00408C40		
Input Link 17: RX DAC Threshold		00408C44		
Input Link 18: RX DAC Threshold		00408C48		
Input Link 19: RX DAC Threshold		00408C4C		
Input Link 20: RX DAC Threshold		00408C50		
Input Link 21: RX DAC Threshold		00408C54		
Input Link 22: RX DAC Threshold		00408C58		
Input Link 23: RX DAC Threshold		00408C5C		
Input Link 24: RX DAC Threshold		00408C60		
Input Link 25: RX DAC Threshold		00408C64		
Input Link 26: RX DAC Threshold		00408C68		
Input Link 27: RX DAC Threshold		00408C6C		
Input Link 28: RX DAC Threshold		00408C70		
Input Link 29: RX DAC Threshold		00408C74		
Input Link 30: RX DAC Threshold		00408C78		
Input Link 31: RX DAC Threshold		00408C7C		
Input Link 32: RX DAC Threshold		00408C80		
Input Link 33: RX DAC Threshold		00408C84		
Input Link 34: RX DAC Threshold		00408C88		
Input Link 35: RX DAC Threshold		00408C8C		
Input Link 36: RX DAC Threshold		00408C90		
Input Link 37: RX DAC Threshold		00408C94		
Input Link 38: RX DAC Threshold		00408C98		
Input Link 39: RX DAC Threshold		00408C9C		
Input Link 40: RX DAC Threshold		00408CA0		
Input Link 41: RX DAC Threshold		00408CA4		
Input Link 42: RX DAC Threshold		00408CA8		
Input Link 43: RX DAC Threshold		00408CAC		
Input Link 44: RX DAC Threshold		00408CB0		
Input Link 45: RX DAC Threshold		00408CB4		
Input Link 46: RX DAC Threshold		00408CB8		
Input Link 47: RX DAC Threshold		00408CBC		
			Bit Value	
				Value
Bits[7:0]: DAC Threshold setting				

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Input Link 48: RX DAC Threshold		00408CC0	RW	8
Input Link 49: RX DAC Threshold		00408CC4		
Input Link 50: RX DAC Threshold		00408CC8		
Input Link 51: RX DAC Threshold		00408CCC		
Input Link 52: RX DAC Threshold		00408CD0		
Input Link 53: RX DAC Threshold		00408CD4		
Input Link 54: RX DAC Threshold		00408CD8		
Input Link 55: RX DAC Threshold		00408CDC		
Input Link 56: RX DAC Threshold		00408CE0		
Input Link 57: RX DAC Threshold		00408CE4		
Input Link 58: RX DAC Threshold		00408CE8		
Input Link 59: RX DAC Threshold		00408CEC		
Input Link 60: RX DAC Threshold		00408CF0		
Input Link 61: RX DAC Threshold		00408CF4		
Input Link 62: RX DAC Threshold		00408CF8		
Input Link 63: RX DAC Threshold		00408CFC		
Input Link 64: RX DAC Threshold		00408D00		
Input Link 65: RX DAC Threshold		00408D04		
Input Link 66: RX DAC Threshold		00408D08		
Input Link 67: RX DAC Threshold		00408D0C		
Input Link 68: RX DAC Threshold		00408D10		
Input Link 69: RX DAC Threshold		00408D14		
Input Link 70: RX DAC Threshold		00408D18		
Input Link 71: RX DAC Threshold		00408D1C		
Input Link 72: RX DAC Threshold		00408D20		
Input Link 73: RX DAC Threshold		00408D24		
Input Link 74: RX DAC Threshold		00408D28		
Input Link 75: RX DAC Threshold		00408D2C		
Input Link 76: RX DAC Threshold		00408D30		
Input Link 77: RX DAC Threshold		00408D34		
Input Link 78: RX DAC Threshold		00408D38		
Input Link 79: RX DAC Threshold		00408D3C		
Input Link 80: RX DAC Threshold		00408D40		
Input Link 81: RX DAC Threshold		00408D44		
Input Link 82: RX DAC Threshold		00408D48		
Input Link 83: RX DAC Threshold		00408D4C		
Input Link 84: RX DAC Threshold		00408D50		
Input Link 85: RX DAC Threshold		00408D54		
Input Link 86: RX DAC Threshold		00408D58		
Input Link 87: RX DAC Threshold		00408D5C		
Input Link 88: RX DAC Threshold		00408D60		
Input Link 89: RX DAC Threshold		00408D64		
Input Link 90: RX DAC Threshold		00408D68		
Input Link 91: RX DAC Threshold		00408D6C		
Input Link 92: RX DAC Threshold		00408D70		
Input Link 93: RX DAC Threshold		00408D74		
Input Link 94: RX DAC Threshold		00408D78		
Input Link 95: RX DAC Threshold		00408D7C		
			<b>Bit Value</b>	
Bits[7:0]: DAC Threshold setting			Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

### 8.8 Monitoring ADC Setup Registers

Description	REG ID	Address	Access	Width
Monitoring ADC Setup (SCT & PIXEL series cards only) <b>Label: MON_SUP</b>		00408E00	W	8
Write to this register to set up the monitoring ADC. Data written is ignored.			<b>Bit Value</b>	
<b>Bits[7:0]:</b>			Value	

Description	REG ID	Address	Access	Width
Monitoring ADC Config (SCT & PIXEL series cards only) <b>Label: MON_FIG</b>		00408E04	W	8
Write to this register to set up the channel for the monitoring ADC to convert. Data written is the channel number.			<b>Bit Value</b>	
<b>Bits[7:0]: Channel Number</b>			Value	

Description	REG ID	Address	Access	Width
Monitoring ADC Convert (SCT & PIXEL series cards only) <b>Label: MON_CONV</b>		00408E08	W	8
Write to this register to instruct the monitoring ADC to do a conversion. Data written is ignored.			<b>Bit Value</b>	
<b>Bits[7:0]:</b>			Value	

Description	REG ID	Address	Access	Width
Spare Register (SCT & PIXEL series cards only) <b>Label: MON_SPARE</b>		00408E0C	TBD	8
TBD.			<b>Bit Value</b>	
<b>Bits[7:0]:</b>			TBD	

Description	REG ID	Address	Access	Width
Monitoring ADC Data LSB (SCT & PIXEL series cards only) <b>Label: MON_LSDAT</b>		00408E10	R	8
Lowest eight bits from ADC conversion are held in this register.			<b>Bit Value</b>	
<b>Bits[7:0]: Data bits 0-7</b>			Value	

Description	REG ID	Address	Access	Width
Monitoring ADC Data MSB (SCT & PIXEL series cards only) <b>Label: MON_MS DAT</b>		00408E14	R	2 or 4
Top bits from ADC conversion are held in this register. Numbers of bits depend on hardware revision number (low 5 bits of Hardware Information register). Hardware revision = 0 uses 2 bits Hardware revision = 1 uses 4 bits			<b>Bit Value</b>	
<b>Bits[1:0]: Data bits 9-8 OR Bits:[3:0] Data bits 11-8</b>			Value	

### 8.9 BOC Reset and Status and Miscellaneous Registers

Description	REG ID	Address	Access	Width
BOC Resets (Series cards only - see individual reset registers below for pre-production cards)		00408F00	RW	8
Write 1 followed by 0 into the relevant bit of this register to reset the BOC function and then release the reset.			<b>Bit Value</b>	
<b>Bits[0:2] Unused</b>			1	0
<b>Bits[3:3] BOC OK</b>			X	
<b>Bits[4:4] Vpin reset</b>			Preset	Release
<b>Bits[5:5] RX DAC Clear</b>			Reset	Release
<b>Bits[6:6] TX DAC Clear</b>			Reset	Release
<b>Bits[7:7] BPM Reset</b>			Reset	Release

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
BPM Reset (Pre-production cards only - see BOC Resets Register for Series cards)		00408F04	RW	1
Write 1 followed by 0 into this register to reset the BPM12 chips and then release the reset.			<b>Bit Value</b>	
			1	0
<b>Bits[0:0]</b>			Reset	Release

Description	REG ID	Address	Access	Width
TX DAC Clear (Pre-production cards only - see BOC Resets Register for Series cards)		00408F08	RW	1
Write 1 followed by 0 into this register to clear the TX DACs and release the clear signal.			<b>Bit Value</b>	
			1	0
<b>Bits[0:0]</b>			Clear	Release

Description	REG ID	Address	Access	Width
RX DAC Clear (Pre-production cards only - see BOC Resets Register for Series cards)		00408F0C	RW	1
Write 1 followed by 0 into this register to clear the RX DACs and release the clear signal.			<b>Bit Value</b>	
			1	0
<b>Bits[0:0]</b>			Clear	Release

Description	REG ID	Address	Access	Width
BOC Status (Pre-production cards - see below for Series cards)		00408F10	R	8
Status of the BOC			<b>Bit Value</b>	
			1	0
<b>Bit 0:</b> SW1 on BOC (not used)			0	
<b>Bit 1:</b> SW4 on BOC (on-board laser enable switch)			On	Off
<b>Bit 2:</b> SW5 on BOC (not used)			0	
<b>Bit 3:</b> SW6 on BOC (not used)			0	
<b>Bit 4:</b> Unused			0	
<b>Bit 5:</b> RODSENSE			!Sense	Sense
<b>Bit 6:</b> Local Laser Enable			Enabled	Interlock
<b>Bit 7:</b> Remote Laser Enable			Enabled	Interlock

Description	REG ID	Address	Access	Width
BOC Status (Series cards - see above for Pre-production cards).		00408F10	R	8
Status of the BOC			<b>Bit Value</b>	
			1	0
<b>Bit 0:</b> Unused			X	
<b>Bit 1:</b> BOC OK (latched)			OK	Not OK
<b>Bit 2:</b> Vb OK			OK	Not OK
<b>Bit 3:</b> Va OK			OK	Not OK
<b>Bit 4:</b> Err flag			Error	No error
<b>Bit 5:</b> RODSENSE			!Sense	Sense
<b>Bit 6:</b> Local Laser Enable			Enabled	Interlock
<b>Bit 7:</b> Remote Laser Enable			Enabled	Interlock

Description	REG ID	Address	Access	Width
RX Data Mode		00408F14	RW	3
Sets the data mode for the receiver side of the BOC. Normally set to 0 for SCT			<b>Value</b>	
<b>0:</b>			Normal SCT(B-reg)	
<b>1:</b>			SCT timing (B- & V-reg)	
<b>2:</b>			PIXEL LAYER 2 (40Mb/s)	
<b>3:</b>			PIXEL LAYER 1 & B (80Mb/s)	
<b>4:</b>			Reserved	
<b>5:</b>			Reserved	
<b>6:</b>			CLOCK as DATA	
<b>7:</b>			TRANSPARENT MODE	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Vernier Clock Fine Phase		00408F20	RW	8
Fine phase adjustment of the vernier clock			Value	
Bits[7:0]: DAC setting			Delay in 40ps steps	

Description	REG ID	Address	Access	Width
Clock Control (note variation between Rev C series BOC and other cards)		00408F28	RW	5
Control bits for the clock. Normally all bits are 0. The Half Clock Inhibit bit, if set, will stop the circuitry generating the 20MHz clock, even if the Half Clock bit is cleared (and hence the 20MHz clock is not in use).			Bit Value	
			1	0
Bit 0: Clock invert			Invert	Normal
Bit 1: Half Clock			Halve	Normal
Bit 2: Vernier bypass			Bypass	Normal
Bit 3: BPM bypass			Bypass	Normal
Bit 4: Phos4 fix (Series cards only)			Fix	Normal
Bit 5: Half Clock Inhibit (Rev C series cards only)			Inhibit	Enable

Description	REG ID	Address	Access	Width
Firmware revision		00408F40	R	8
Revision level of the firmware			Value	
Bits[7:0]: Revision level			Value	

Description	REG ID	Address	Access	Width
Hardware information		00408F44	R	8
Revision level of the hardware. The information returned in this byte now separately identifies the PCB version (bits 5-7) and the hardware revision for that PCB version (bits 0-4).			Value	
Bits[0:4] Hardware revision			Value	
Bits[7:5] PCB version			0 = pre-production 1 = series Rev A 2 = series Rev B 3 = series Rev C	

Description	REG ID	Address	Access	Width
Module type		00408F48	R	8
Module type designation			Value	
Bits[7:0]: Module type			Pre-production: 44 Series: 46	

Description	REG ID	Address	Access	Width
Manufacturer		00408F4C	R	8
Manufacturer identification			Value	
Bits[7:0]: Manufacturer			0xCB	

Description	REG ID	Address	Access	Width
Serial Number		00408F60	R	8
Module serial number - set by 2 HEX switches on the board			Value	
Bits[7:0]: Serial Number			Value	



# APPENDIX A: ROD and BOC FPGA Register Definitions

## 8.10 Monitoring ADC Tables and Conversion Information: SCT Version

Monitoring ADC (SCT series cards only): channel information				
Channel	Parameter		Formulae	
			Rev A	Rev B
0	PIN Current	Streams[0:11]	1	4
1	PIN Current	Streams[12:23]	1	4
2	PIN Current	Streams[24:35]	1	4
3	PIN Current	Streams[36:47]	1	4
4	PIN Current	Streams[48:59]	1	4
5	PIN Current	Streams[60:71]	1	4
6	PIN Current	Streams[72:83]	1	4
7	PIN Current	Streams[84:95]	1	4
8	PIN Voltage	Streams[0:47]	2	5
9	PIN Voltage	Streams[48:95]	2	5
10	Thermistor 1		3	6
11	Thermistor 2		3	6

Formulae to convert ADC reading to true value						
Board Revision	Number	Formula Form	Parameter Values		Range Max	Nominal Value
			A	B		
Rev A	1	A+B*Reading	41.52mA	-0.04051 mA/count	41.52 mA	
	2	A+B*Reading	0.0mV	11.106 mV/count	11.36 V	8.42V
	3	RTherm=A*((B/Reading)-1)	10000 Ohm	1023		10k Ohm@ 25C
Rev B	4	A+B*Reading	0.0mA	0.02383 mA/count	23.375 mA	
	5	A+B*Reading	0.0mV	14.494 mV/count	14.83 V	9.78V
	6	RTherm=A*((B/Reading)-1)	10000 Ohm	1023		10kOhm @25C

Converting RTherm to Temperature			
<b>Thermistor used:</b>	ATC Semitec 103KT1608 to VADC with 10k to ground		
<b>Steinhart-Hart Formula:</b>	$1/T(\text{Kelvin}) = C0 + C1*\ln(R\text{Therm}) + C3*(\ln(R\text{Therm}))^3$		
<b>Parameters optimized over 20-100C</b>	<b>Rev A</b>	C0	7.4717E-04
		C1	2.7726E-04
		C3	6.8388E-08
	<b>Rev B</b>	C4	7.4717E-04
		C5	2.7726E-04
		C6	6.8388E-08

## APPENDIX A: ROD and BOC FPGA Register Definitions

### 8.11 Monitoring ADC Tables and Conversion Information: PIXEL Version

Monitoring ADC (PIXEL series cards only): channel information				
Channel	Parameter		Formulae	
			Rev A	Rev B & C
0	PIN Current	Streams[0:11]	1	4
1	PIN Voltage	Streams[12:23]	1	4
2	PIN Voltage	Streams[24:35]	1	4
3	PIN Current	Streams[36:47]	1	4
4	PIN Current	Streams[48:59]	1	4
5	PIN Voltage	Streams[60:71]	1	4
6	PIN Voltage	Streams[72:83]	1	4
7	PIN Current	Streams[84:95]	1	4
8	PIN Voltage	Streams[0:47]	2	5
9	PIN Voltage	Streams[48:95]	2	5
10	Thermistor 1		3	6
11	Thermistor 2		3	6

Formulae to convert ADC reading to true value						
Board Revision	Number	Formula Form	Parameter Values		Range Max	Nominal Value
			K	M		
Rev A	1	K+M*Reading	41.52 mA	-10.147 uA/ct	41.52 mA	
	2	M*Reading	0.0 mV	2.777 mV/ct	11.36 V	8.42 V
	3	RTherm=K*((M/Reading)-1)	10000 Ohm	4095		10k @ 25C
Rev B & Rev C	4	K+M*Reading	-97 uA	5.958 uA/ct	24.375 mA	
	5	M*Reading	0.0mV	3.623 mV/ct	14.83 V	9.78V
	6	RTherm=K*((M/Reading)-1)	10000 Ohm	4095		10k @ 25C

Converting RTherm to Temperature			
Thermistor used:	ATC Semitec 103KT1608 to VADC with 10k to ground		
Steinhart-Hart Formula:	$1/T(\text{Kelvin}) = C0 + C1*\ln(\text{RTherm}) + C3*(\ln(\text{RTherm}))**3$		
Parameters optimized over 20-100C	Rev A	C0	7.4717E-04
		C1	2.7726E-04
		C3	6.8388E-08
	Rev B & C	C4	7.4717E-04
		C5	2.7726E-04
		C6	6.8388E-08

# APPENDIX A: ROD and BOC FPGA Register Definitions

## 9 ROD Slave DSP HPI Registers

Description	Address	Access	Width
Slave DSP 0: HPIC, Host Port Interface Control Register	00780000	RW	32
Slave DSP 1: HPIC, Host Port Interface Control Register	007A0000	RW	32
Slave DSP 2: HPIC, Host Port Interface Control Register	007C0000	RW	32
Slave DSP 3: HPIC, Host Port Interface Control Register	007E0000	RW	32
The HPIC register is normally the first register accessed to set configuration bits and initialize the interface. The HPIC is organized as a 32-bit register whose high half word and low half word contents are the same. On a host write, both half words must be identical. The lower half word is the write register, and the upper half word is the status register. No storage is allocated for the read-only reserved values. Only CPU writes to the lower half word affect HPIC values and HPI operation.		Bit Value	
		1	0
<b>Bit[0]:</b> HWOB - Read Only, see definition in bit 16		FHW->LSW	FHW->MSW
<b>Bit[1]:</b> DSPINT - Read Only, see definition in bit 17		INT	IDLE
<b>Bit[2]:</b> HINT - Read Only, see definition in bit 18		HINT=0	HINT=1
<b>Bit[3]:</b> HRDY - Read Only, see definition in bit 19		Ready	Busy
<b>Bit[4]:</b> FETCH - Read Only, see definition in bit 20		Request	Idle
<b>Bits[15:5]:</b> Reserved		Not Used	
<b>Bit[16]:</b> HWOB - If HWOB = 1, the first half word is least significant. If HWOB = 0, the first half word is most significant. HWOB affects both data and address transfers. Only the host can modify this bit. HWOB must be initialized before the first data or address register access.		FHW->LSW	FHW->MSW
<b>Bit[17]:</b> DSPINT - The host processor-to-CPU/DMA interrupt		INT	IDLE
<b>Bit[18]:</b> HINT - DSP-to-Host Interrupt. The inverted value of this bit determines the state of the CPU HINT output		HINT=0	HINT=1
<b>Bit[19]:</b> HRDY - Ready Signal to Host. If HRDY = 0, the internal bus is waiting for an HPI data access request to finish		Ready	Busy
<b>Bit[20]:</b> FETCH - Host Fetch Request. The value read by the host or CPU from this register field is always 0. The host writes a 1 to this bit to request a fetch into HPID of the word at the address pointed to by HPIA. The 1 is never actually written to this bit, however.		Fetch Request	Idle
<b>Bits[31:21]:</b> Reserved		Not Used	

Description	Address	Access	Width
Slave DSP 0: HPIA, Host Port Interface Address Register	00780004	RW	32
Slave DSP 1: HPIA, Host Port Interface Address Register	007A0004	RW	32
Slave DSP 2: HPIA, Host Port Interface Address Register	007C0004	RW	32
Slave DSP 3: HPIA, Host Port Interface Address Register	007E0004	RW	32
The HPIA contains the address of the memory accessed by the HPI at which the current access occurs. This address is a 30-bit word address, so the two LSBs are unaffected by HPIA writes and are always read as 0. The C62x/C67x HPIA register is only accessible by the host. It is not mapped to the DSP memory.		Bit Value	
<b>Bits[31: 0]:</b> HPIA		Value	

Description	Address	Access	Width
Slave DSP 0: HPID++, Host Port Interface Data Register w/Auto Inc	00780008	RW	32
Slave DSP 1: HPID++, Host Port Interface Data Register w/Auto Inc	007A0008	RW	32
Slave DSP 2: HPID++, Host Port Interface Data Register w/Auto Inc	007C0008	RW	32
Slave DSP 3: HPID++, Host Port Interface Data Register w/Auto Inc	007E0008	RW	32
The auto increment feature results in efficient sequential host accesses. For both HPID read and write accesses, this removes the need for the host to load incremented addresses into HPIA. For read accesses, the data pointed to by the next address is fetched immediately after the completion of the current read. For the C62x/C67x pre-fetching also occurs after a host write of FETCH = 1 to the HPIC register. If the next HPI access is an HPID read, then the data is not re-fetched and the pre-fetched data is sent to the host. Otherwise, the HPI must wait for the pre-fetch to finish.		Bit Value	
<b>Bits[31: 0]:</b> HPID++		Value	

Description	Address	Access	Width
Slave DSP 0: HPID, Host Port Interface Data Register	0078000C	RW	32
Slave DSP 1: HPID, Host Port Interface Data Register	007A000C	RW	32
Slave DSP 2: HPID, Host Port Interface Data Register	007C000C	RW	32
Slave DSP 3: HPID, Host Port Interface Data Register	007E000C	RW	32
A read or write cycle to the HPID no Auto Increment Register will access a register on the ROD at the specific address set in the HPIA register.		Bit Value	
<b>Bits[31: 0]:</b> HPID		Value	

## APPENDIX A: ROD and BOC FPGA Register Definitions

Description	REG ID	Address	Access	Width
Template:		0040	RW	32
			Bit Value	
			1	0
Bit [0] :			Over	Idle
Bit [1] :			Over	Idle
Bit [2] :			Over	Idle